دانشگاه صنعتی امیرکبیر

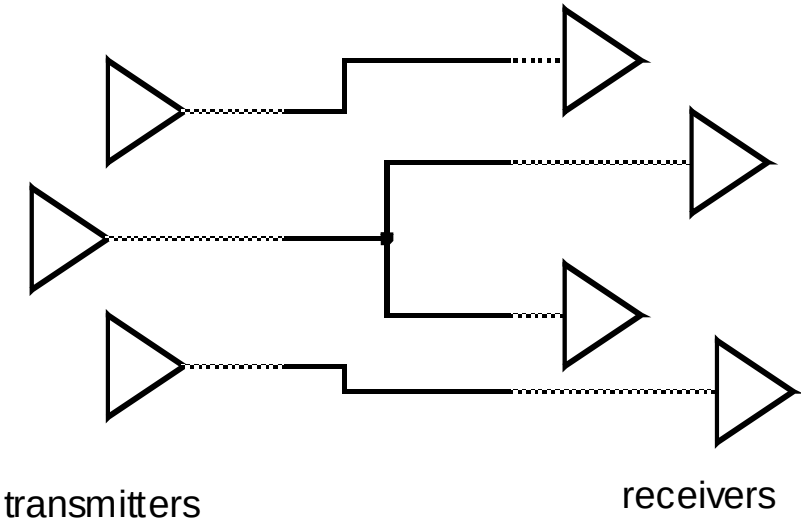
دانشکده مهندسی برق

طراحی مدارهای VLSI

فصل ششم: اتصالات میانی

مجید شالچیان

اتصالات در مدار های مجتمع



schematics

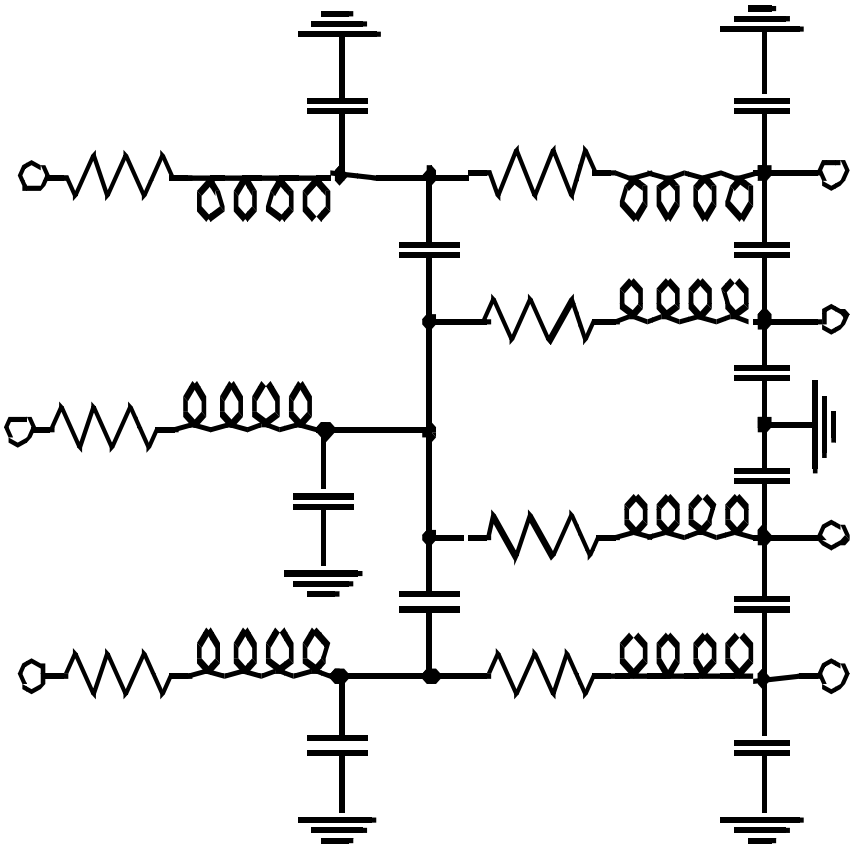
physical

مقدمه

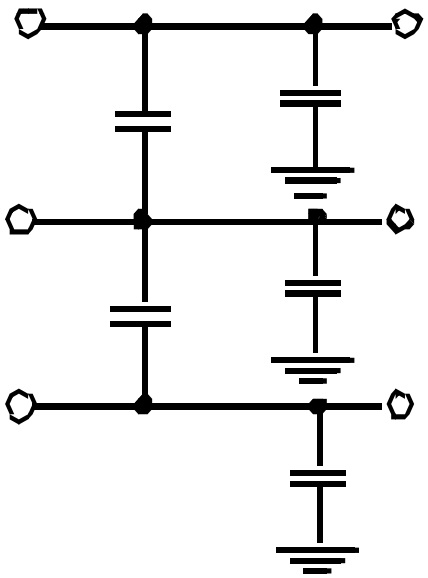
- **چندین لایه** Metal **با شکل های مختلف منجر به بروز اثرات خازنی، مقاومتی و سلفی در مدار های مجتمع می شوند.**
- **افزایش تاخیر و کاهش سرعت عملیاتی مدار ها**
- **افزایش مصرف انرژی و تلفات سیگنال**
- **ایجاد نویز و کاهش** reliability **مدار ها**

ارایه یک مدل کامل و دقیق از اتصالات پیچیده و در مدار های با تعداد المان زیاد غیر ممکن است.

(استفاده از تقریب های مهندسی)

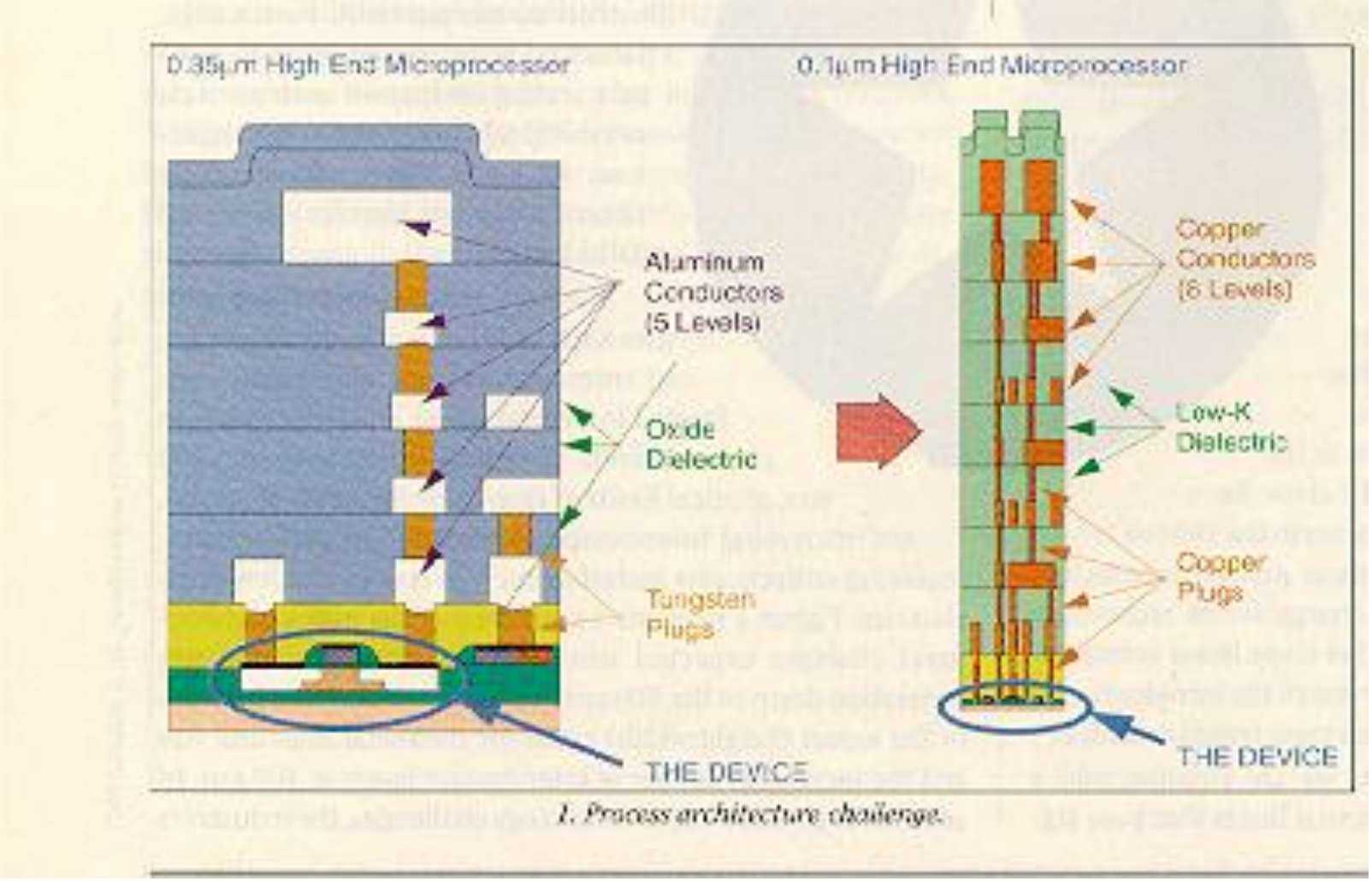


All-inclusive model



Capacitance-only

مهمتر شدن اثر اتصالات در تکنولوژی های جدید

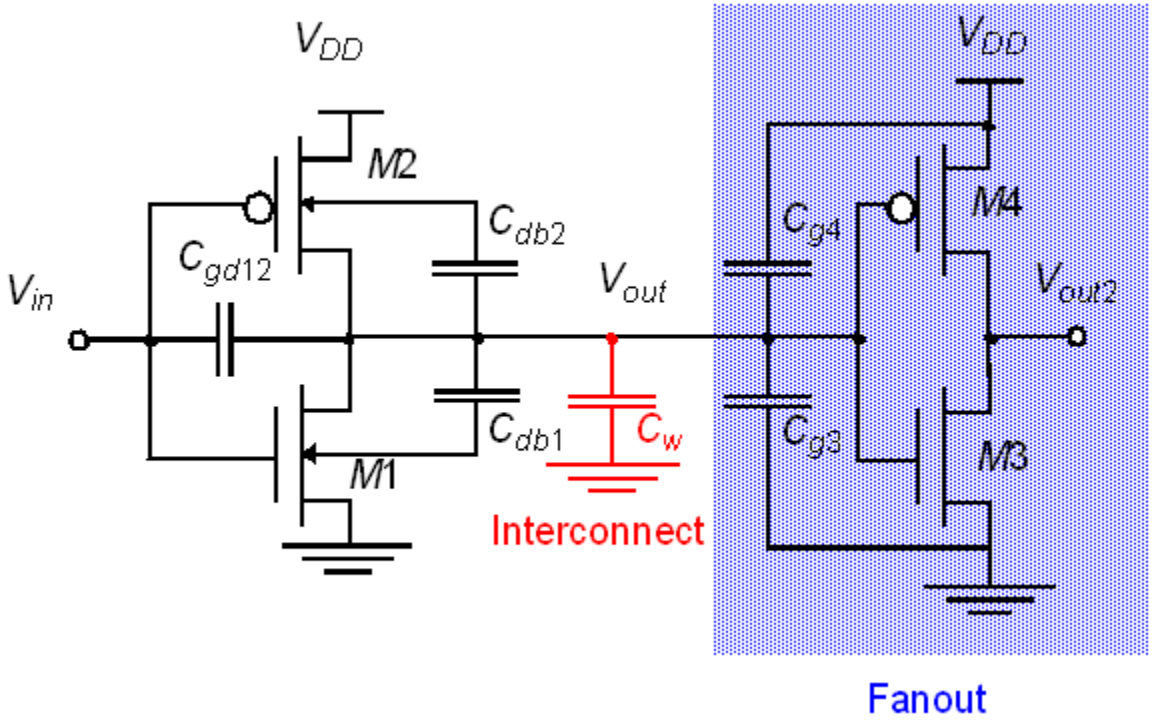


1. Process architecture challenge.

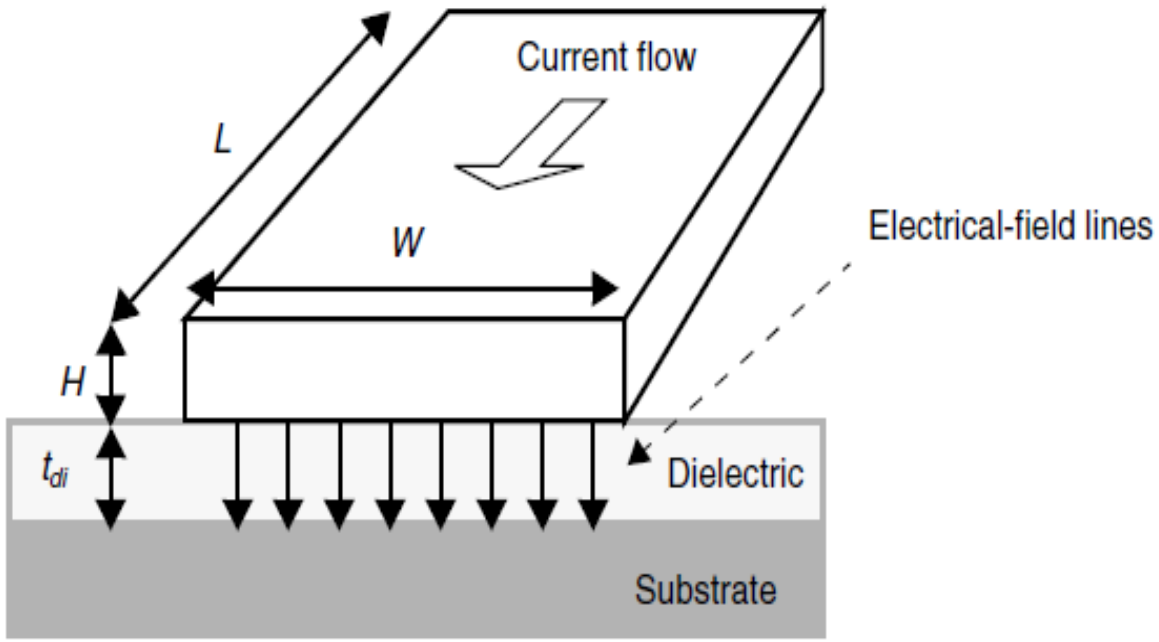
المان های اتصالات میانی

- خازن
  - خازن سیم تا زمین
  - خازن بین سیم ها
- مقاومت
- سلف

۱– خازن اتصالات میانی



خازن صفحه ای اتصال تا زمین



خازن اتصال تا زمین

permittivity constant (SiO_2= 3.9)

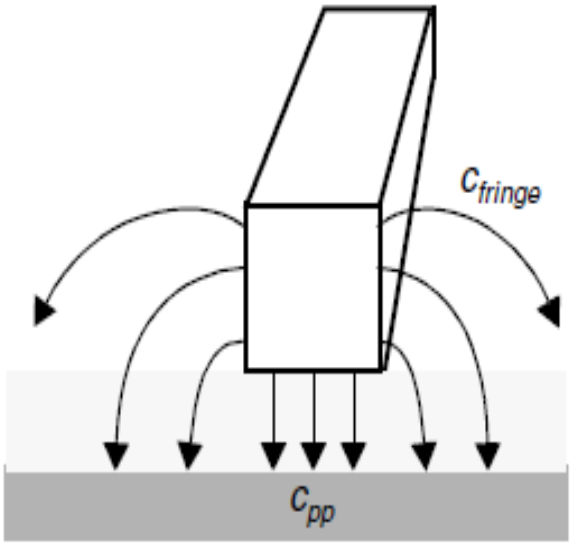
$C_{pp} = (\varepsilon_{di}/t_{di})\ WL$

ثابت گذر دهی

ε_0 ضریب گذر دهی خلا است که برابر است با 8.85×10^{-14} F/cm

Material	ε_{di}
Free space	1
Teflon AF	2.1
Aromatic thermosets (SiLK)	2.6 – 2.8
Polyimides (organic)	3.1 – 3.4
Fluorosilicate glass (FSG)	3.2 – 4.0
Silicon dioxide	3.9 – 4.5
Glass epoxy (PCBs)	5
Silicon nitride	7.5
Alumina (package)	9.5
Silicon	11.7

خازن های نشتی جانبی تا زمین



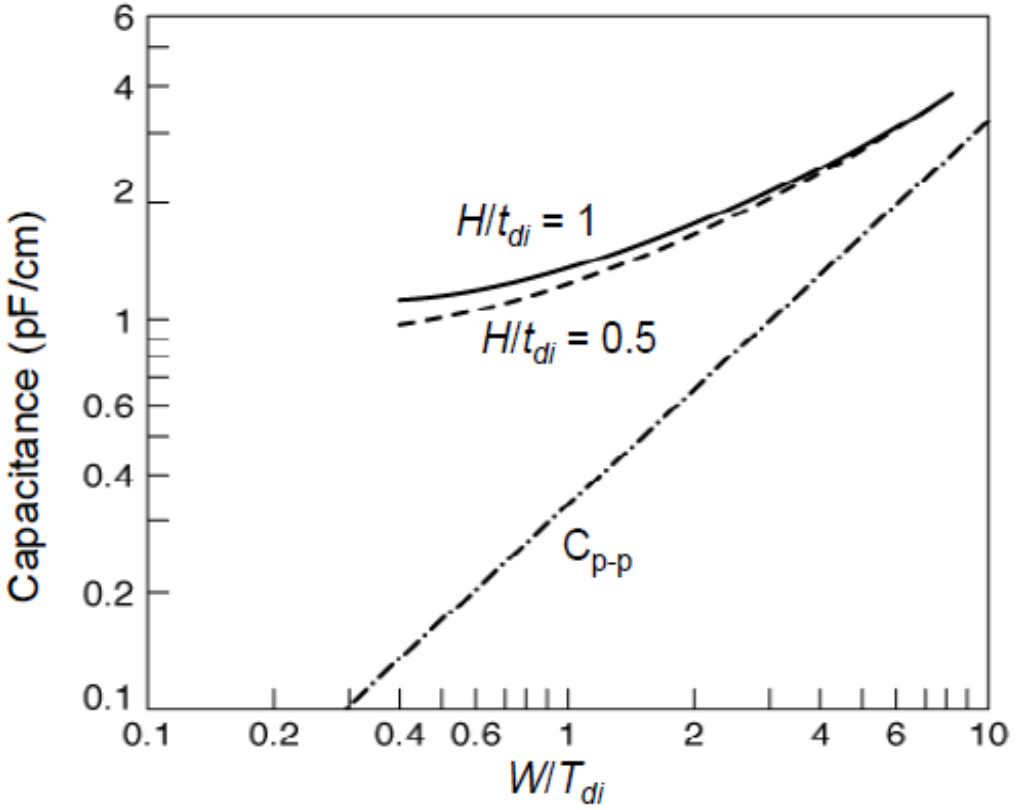
Fringing fields

$$C_{wire} = C_{pp} + C_{fringe} = \frac{w\varepsilon_{di}}{t_{di}} + \frac{2\pi\varepsilon_{di}}{\log(t_{di}/H)}$$

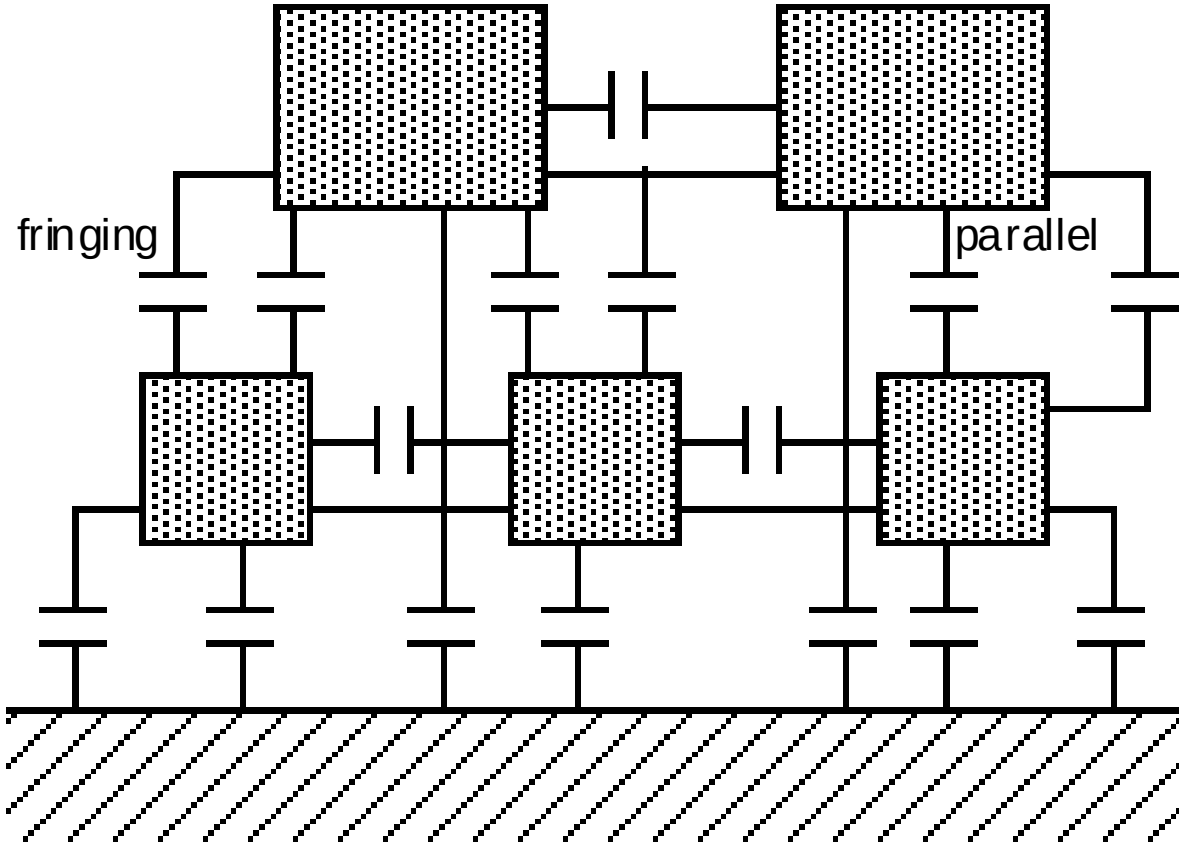
$$w = W - H/2$$

تاثیر نسبت ابعاد روی مقدار خازن

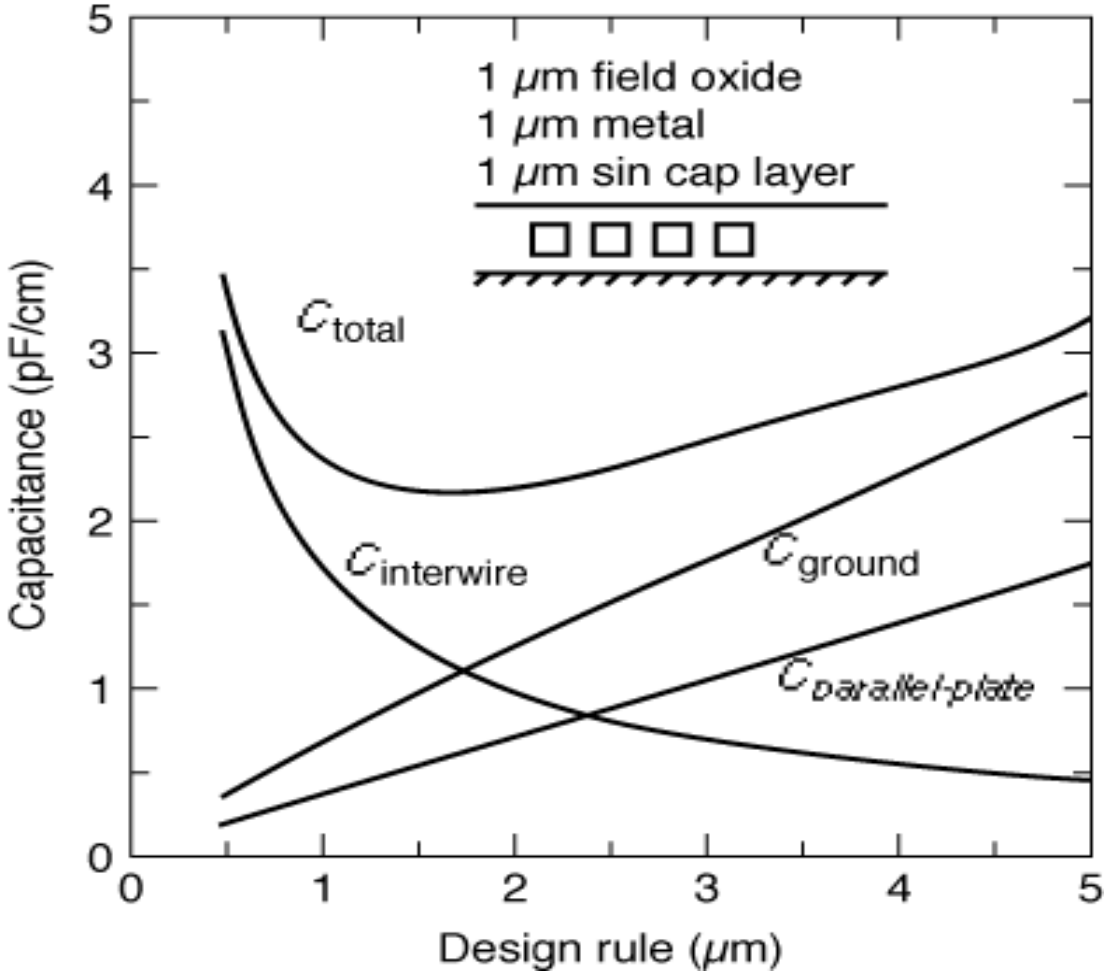
برای مقادیر بزرگ W/H ظرفیت خازن به خازن صفحه ای نزدیک می شود اما برای W/H های کمتر از 1.5 خازن fringe غالب می شود



خازن بین سیم ها



مقایسه نقش خازن ها



Insights

- For W/H < 1.5, the fringe component dominates the parallel-plate component. Fringing capacitance can increase the overall capacitance by a factor of 10 or more.
- When W < 1.75H interwire capacitance starts to dominate
- Interwire capacitance is more pronounced for wires in the higher interconnect layers (further from the substrate)
- Rules of thumb
  - Never run wires in diffusion
  - Use poly only for short runs
  - Shorter wires – lower R and C
  - Thinner wires – lower C but higher R
- Wire delay nearly proportional to L^2

Wiring Capacitances

	Field	Active	Poly	Al1	Al2	Al3	Al4
Poly	88	pp in aF/μm^2					
	54	fringe in aF/μm					
Al1	30	41	57				
	40	47	54				
Al2	13	15	17	36			
	25	27	29	45			
Al3	8.9	9.4	10	15	41		
	18	19	20	27	49		
Al4	6.5	6.8	7	8.9	15	35	
	14	15	15	18	27	45	
Al5	5.2	5.4	5.4	6.6	9.1	14	38
	12	12	12	14	19	27	52

	Poly	Al1	Al2	Al3	Al4	Al5
Interwire Cap	40	95	85	85	85	115

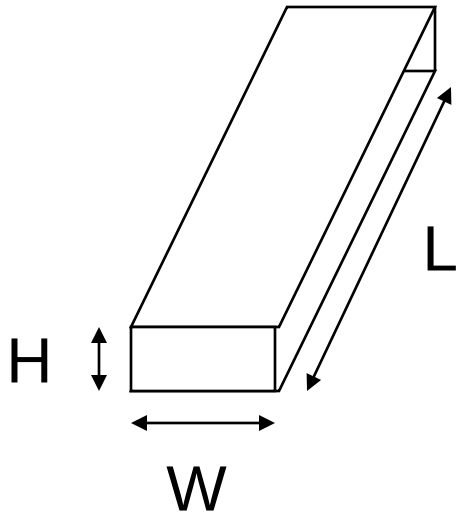
per unit wire length in aF/μm for minimally-spaced wires

Dealing with Capacitance

- Low capacitance (low-k) dielectrics (insulators) such as polymide or even air instead of SiO_2
  - family of materials that are low-k dielectrics
  - must also be suitable thermally and mechanically and
  - compatible with (copper) interconnect

- Copper interconnect allows wires to be thinner without increasing their resistance, thereby decreasing interwire capacitance

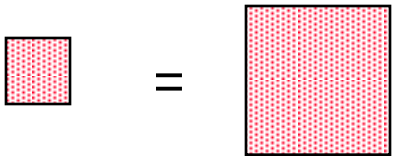
مقاومت اتصالات میانی



$$R = \frac{\rho L}{A} = \frac{\rho}{H} \frac{L}{W}$$

Sheet Resistance $R_{\square}$

$R_{1\square} = R_{2\square}$



Material	ρ(Ω-m)
Silver (Ag)	1.6×10^{-8}
Copper (Cu)	1.7×10^{-8}
Gold (Au)	2.2×10^{-8}
Aluminum (Al)	2.7×10^{-8}
Tungsten (W)	5.5×10^{-8}

Material	Sheet Res. (Ω/□)
n, p well diffusion	1000 to 1500
n+, p+ diffusion	50 to 150
n+, p+ diffusion with silicide	3 to 5
polysilicon	150 to 200
polysilicon with silicide	4 to 5
Aluminum	0.05 to 0.1

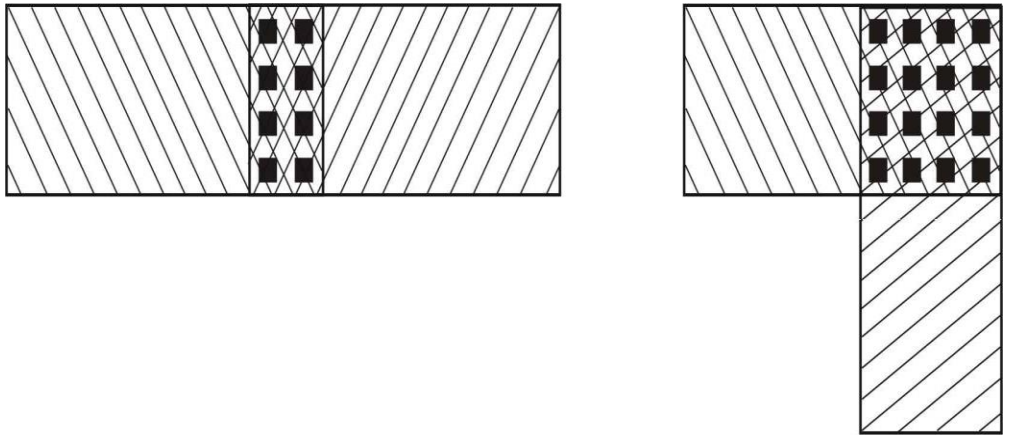
مقاومت صفحه ای لایه های مختلف

مشاهده می شود که آلومینیوم بهترین ماده برای سیم های طولانی است. از لایه نفوذ بهتر است استفاده نشود چون خازن پارازیت زیادی دارد و تاخیر آن بالا است. از پلی سیلیکان هم می توان در اتصالات محلی استفاده کرد.

Material	Sheet Res. (Ω/□)
n, p well diffusion	1000 to 1500
n+, p+ diffusion	50 to 150
n+, p+ diffusion with silicide	3 to 5
polysilicon	150 to 200
polysilicon with silicide	4 to 5
Aluminum	0.05 to 0.1

مقاومت CONTACT ها

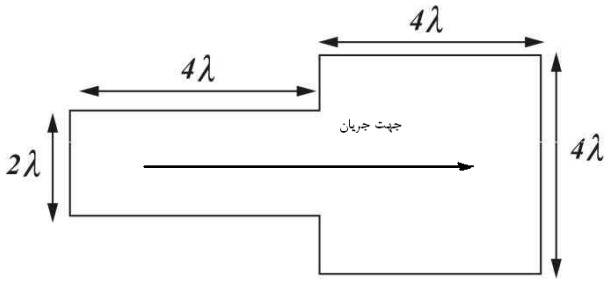
مقاومت contact ها بین فلز و نیمه هادی بین ۵ تا ۲۰ اهم و مقاومت Via بین فلـز و فلز بین ۱ تا ۵ اهم می باشد. برای تشکیل اتصال بین دو لایه با مقاومت کم بهتر اسـت چندین contact یا استفاده شوند چـون اگـر از یـک contact بـزرگ اسـتفاده شـود ازدحام جریان نزدیک لبه رخ می دهد. هنگامیکه جریان با زاویه قائمه حرکت کند بهتـر است از تعداد contact های بیشتری استفاده کنیم.



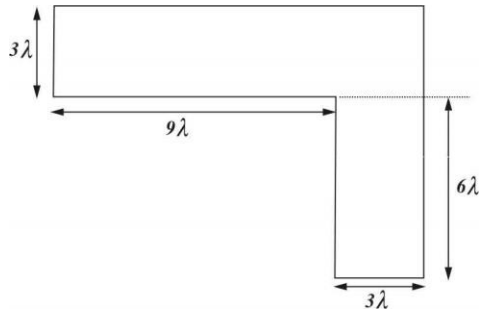
$R_{wire} = 0.075\ \Omega/\square \times (0.1 \times 10^6\ \mu m) / (1\ \mu m) = 7.5\ k\Omega$

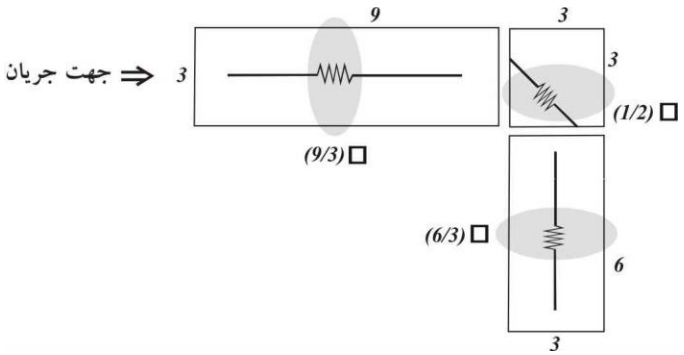
مثال

مثال ۴: مقاومت شکل زیر را بر حسب مقاومت صفحه ای Rs بدست آورید.



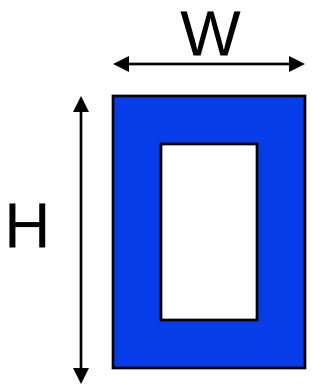
مثال ۵: مقاومت شکل زیر را حساب کنید (ناحیه نفوذ با مقاومت صفحه ای 7.6 اهم بر مربع)





Skin Effect

- At high frequency, currents tend to flow primarily on the surface of a conductor with the current density falling off exponentially with depth into the wire



$\delta = \sqrt{(\rho/(\pi f \mu))}$

where f is frequency

$\mu = 4\pi \times 10^{-7}$ H/m

$\delta = 2.6\ \mu m$ for Al at 1 GHz

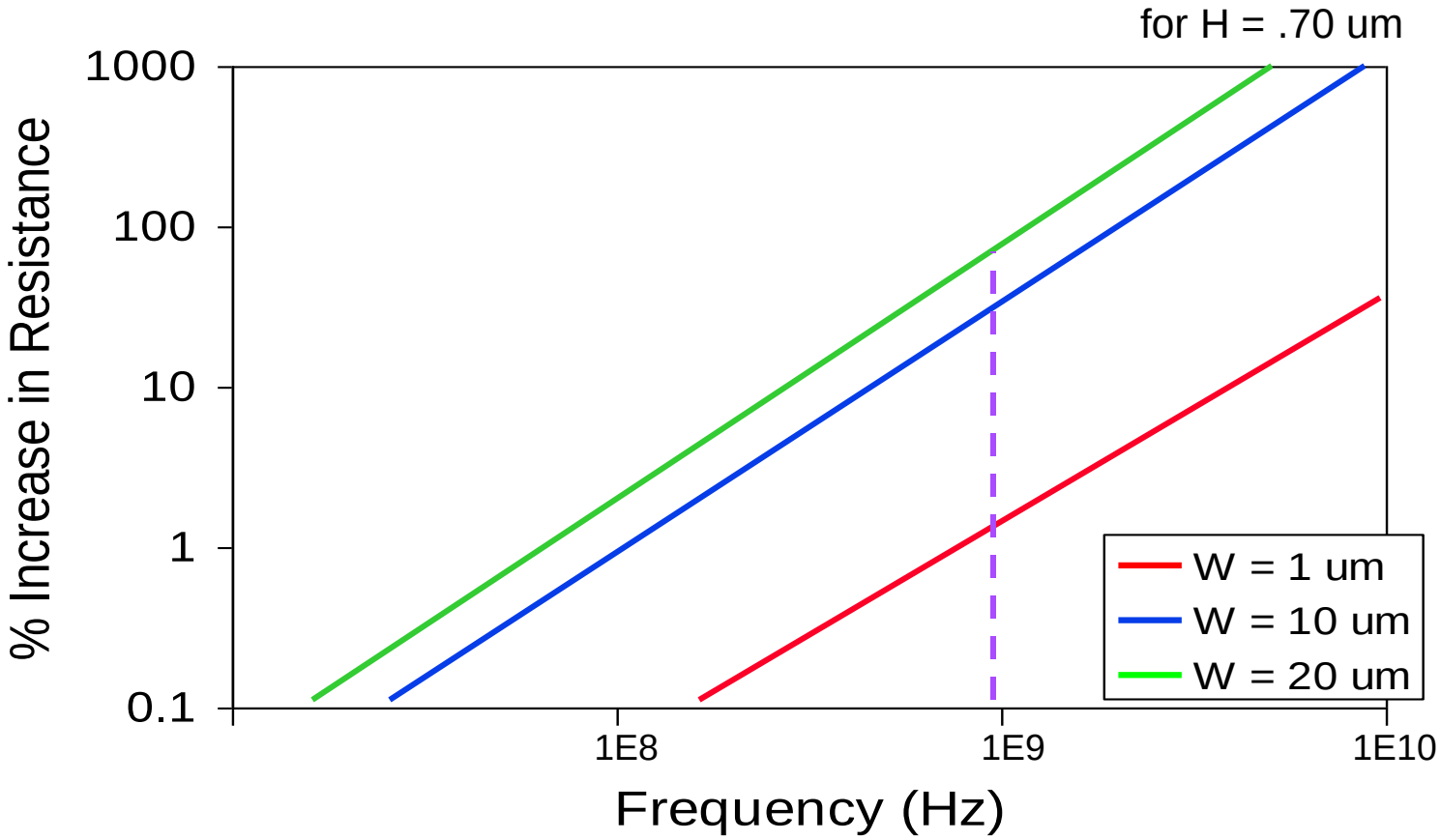
so the overall cross section is ~ $2(W+H)\delta$

- The onset of skin effect is at f_s - where the skin depth is equal to half the largest dimension of the wire.

$$f_s = 4\ \rho\ /\ (\pi\ \mu\ (\max(W,H))^2)$$

- An issue for high frequency, wide (tall) wires (i.e., clocks!)

Skin Effect for Different W's



- A 30% increase in resistance is observe for 20 μm Al wires at 1 GHz (versus only a 1% increase for 1 μm wires)

سلف اتصالات میانی

با توجه به معادله ماکسول از روی خازن می توان سلف را تخمین زد.

$$v = \frac{1}{\sqrt{lc}} = \frac{1}{\sqrt{\varepsilon\mu}} = \frac{c_0}{\sqrt{\varepsilon_r\mu_r}}$$

c_0 equals the speed of light (30 cm/nsec) in a vacuum

$$l = (3.9 \times 8.854 \times 10^{-12}) \times (4\,\pi\,10^{-7}) / C$$

برای تکنولوژی 0.25um و لایه Al1

$W = 0.4\ \mu m$: $c = 92$ aF/μm; $l = 0.47$ pH/μm
$W = 1\ \mu m$: $c = 110$ aF/μm; $l = 0.39$ pH/μm
$W = 10\ \mu m$: $c = 380$ aF/μm; $l = 0.11$ pH/μm

مقادیر سلف ها در مدار های فرکانس پایین تر از 1GHz عموما ناچیز و قابل صرفنظر هستند.

مقایسه مقدار سلف و مقاومت

Assuming a sheet resistance of 0.075 Ω/❑, we can also determine the resistance of the wire,

$$r = 0.075/W\ \Omega/\mu m$$

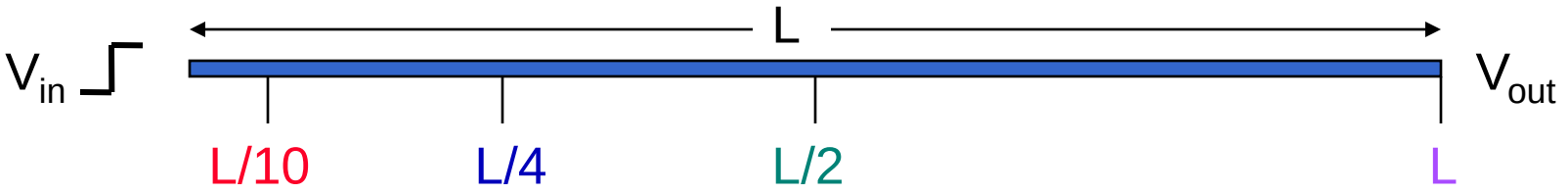
It is interesting to observe that the inductive part of the wire impedance becomes equal in value to the resistive component at a frequency of 27.5 GHz (for a 1 μm wide wire), as can be obtained from solving the following expression:

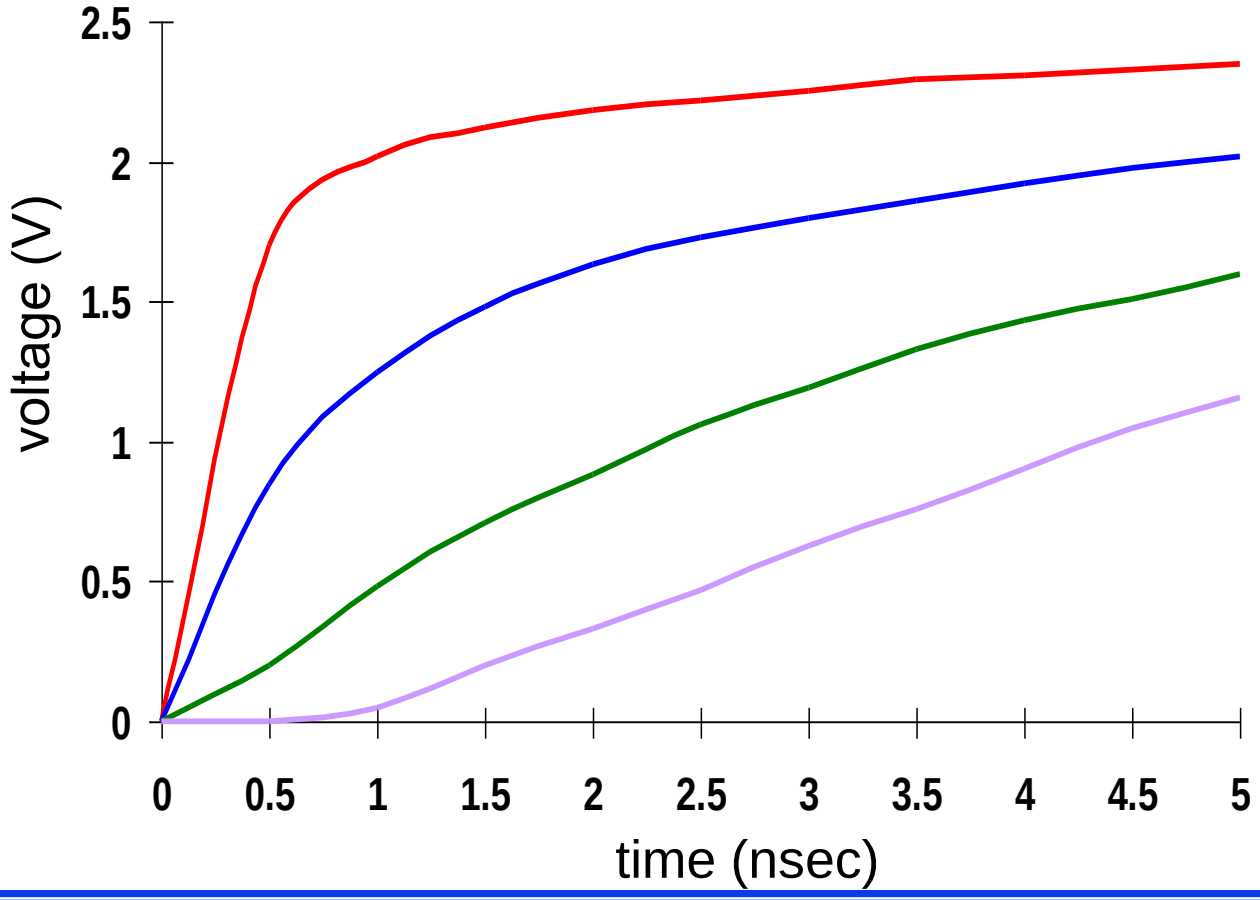
$$\omega l = 2\pi f l = r$$

For extra wide wires, this frequency reduces to approximately 11 GHz. For wires with a smaller capacitance and resistance (such as the thicker wires located at the upper interconnect layers), this frequency can become as low as 500 MHz, especially when better interconnect materials such as Copper are being used. Yet, these numbers indicate that inductance only becomes an issue in integrated circuits for frequencies that are well above 1 GHz.

تخمین تاخیر اتصالات میانی

Simulated Wire Delays





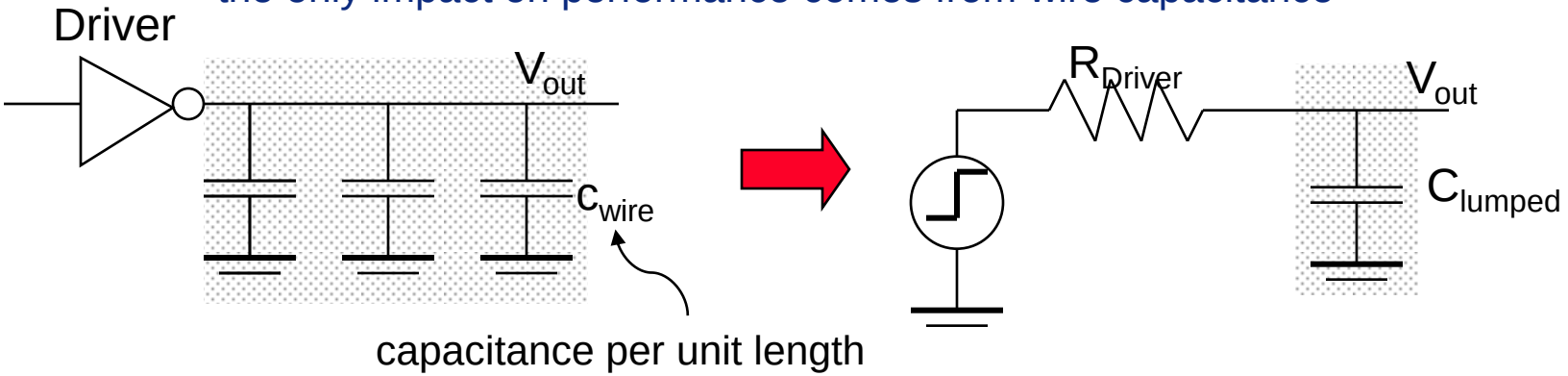
مدل های تاخیر

Ideal wire

- same voltage is present at every segment of the wire at every point in time - at equi-potential
- only holds for *very short* wires, i.e., interconnects between *very* nearest neighbor gates

Lumped C model

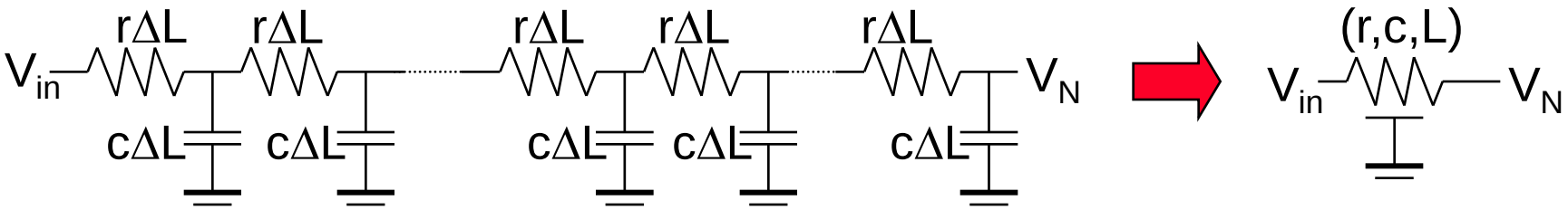
- when only a single parasitic component (C, R, or L) is dominant the different fractions are lumped into a single circuit element
  - When the resistive component is small and the switching frequency is low to medium, can consider only C; the wire itself does not introduce any delay; the only impact on performance comes from wire capacitance



- good for short wires; pessimistic and inaccurate for long wires

مدل های تاخیر (ادامه)

- Lumped RC model
  - total wire resistance is lumped into a single R and total capacitance into a single C
  - good for short wires; pessimistic and inaccurate for long wires
- Distributed RC model
  - circuit parasitics are distributed along the length, L, of the wire
    - c and r are the capacitance and resistance per unit length



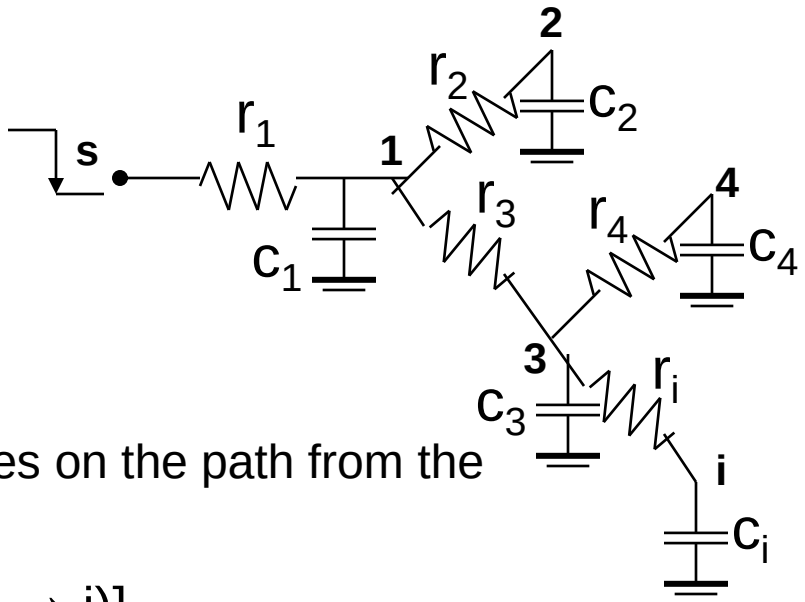
- Delay is determined using the Elmore delay equation

$$\tau_{Di} = \sum_{k=1}^{N} c_k r_{ik}$$

RC tree characteristics

تعریف درخت RC (مدل المور)

- A unique resistive path exists between the source node and any node of the network
  - Single input (source) node, s
  - All capacitors are between a node and GND
  - No resistive loops



- Path resistance (sum of the resistances on the path from the input node to node *i*)

$$r_{ii} = \sum_{j=1}^{i} r_j \Rightarrow (r_j \in [\text{path}(s \rightarrow i)]$$

- Shared path resistance (resistance shared along the paths from the input node to nodes *i* and *k*)

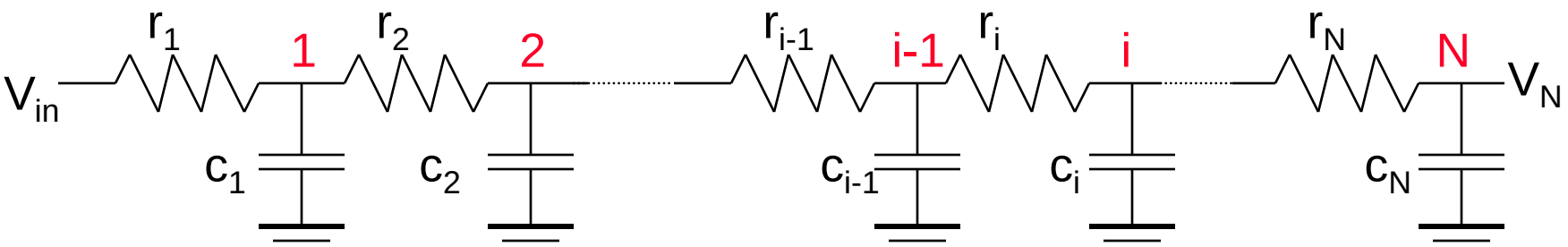
$$r_{ik} = \sum_{j=1}^{N} r_j \Rightarrow (r_j \in [\text{path}(s \rightarrow i) \cap \text{path}(s \rightarrow k)])$$

- A typical wire is a chain network with (simplified) Elmore delay of

$$\tau_{DN} = \sum_{i=1}^{N} c_i r_{ii}$$

فرمول تاخیر شبکه المور

$\tau_{D1}=c_1r_1 \qquad \tau_{D2}=c_1r_1 + c_2(r_1+r_2)$



$\tau_{Di}=c_1r_1+ c_2(r_1+r_2)+\ldots+c_i(r_1+r_2+\ldots+r_i)$

Elmore delay equation $\qquad \tau_{DN} = \sum c_i r_{ii} = \sum^{N} c_i \sum^{i} r_j$

$\tau_{Di}=c_1r_{eq}+ 2c_2r_{eq}+ 3c_3r_{eq}+\ldots+ ic_ir_{eq}$

کاربرد های فرمول المور

- Modeling the delay of a wire
- Modeling the delay of a series of pass transistors
- Modeling the delay of a pull-up and pull-down networks

Distributed RC Model for Simple Wires

- A length L RC wire can be modeled by N segments of length L/N
  - The resistance and capacitance of each segment are given by r L/N and c L/N

$$\tau_{DN} = (L/N)^2(cr+2cr+\ldots+Ncr) = (crL^2)\,(N(N+1))/(2N^2) = CR((N+1)/(2N))$$

where R (= rL) and C (= cL) are the total lumped resistance and capacitance of the wire

- For large N

$$\tau_{DN} = RC/2 = rcL^2/2$$

  - Delay of a wire is a quadratic function of its length, L
  - The delay is 1/2 of that predicted (by the lumped model)

Step Response Points

Voltage Range	Lumped RC	Distributed RC
$0 \rightarrow 50\%$ (t_p)	0.69 RC	0.38 RC
$10\% \rightarrow 90\%$ (t_r)	2.2 RC	0.9 RC

Time to reach the 50% point is $t = \ln(2)\tau = 0.69\tau$

Time to reach the 90% point is $t = \ln(9)\tau = 2.2\tau$

- Example: Consider a Al1 wire 10 cm long and 1 μm wide
  - Using a lumped C only model with a source resistance (R_{Driver}) of 10 kΩ and a total lumped capacitance (C_{lumped}) of 11 pF

$$t_{50\%} = 0.69 \times 10\ k\Omega \times 11pF = 76\ ns$$

$$t_{90\%} = 2.2 \times 10\ k\Omega \times 11pF = 242\ ns$$

  - Using a distributed RC model with c = 110 aF/μm and r = 0.075 Ω/μm

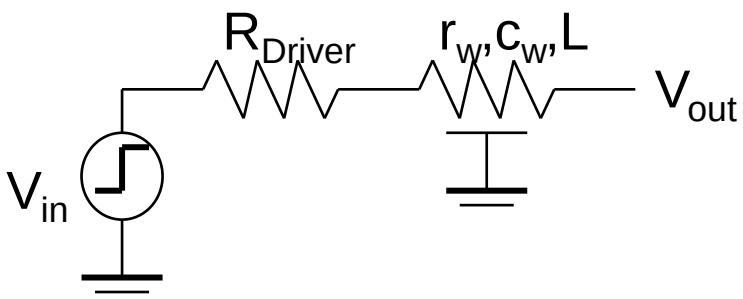
$$t_{50\%} = 0.38 \times (0.075\ \Omega/\mu m) \times (110\ aF/\mu m) \times (10^5\ \mu m)^2 = 31.4\ ns$$

$$t_{90\%} = 0.9 \times (0.075\ \Omega/\mu m) \times (110\ aF/\mu m) \times (10^5\ \mu m)^2 = 74.25\ ns$$

Poly: $t_{50\%} = 0.38 \times (150\ \Omega/\mu m) \times (88+2\times54\ aF/\mu m) \times (10^5\ \mu m)^2 = 112\ \mu s$

Al5: $t_{50\%} = 0.38 \times (0.0375\ \Omega/\mu m) \times (5.2+2\times12\ aF/\mu m) \times (10^5\ \mu m)^2 = 4.2\ ns$

Putting It All Together



- Total propagation delay consider driver and wire

$$\tau_D = R_{Driver}C_w + (R_wC_w)/2 = R_{Driver}C_w + 0.5r_wc_wL^2$$

and $t_p = 0.69\ R_{Driver}C_w + 0.38\ R_wC_w$

where $R_w = r_wL$ and $C_w = c_wL$

- The delay introduced by wire resistance becomes dominant when $(R_wC_w)/2 \geq R_{Driver}\ C_W$ (when $L \geq 2R_{Driver}/R_w$)
  - For an R_{Driver} = 1 kΩ driving an 1 μm wide Al1 wire, L_{crit} is 2.67 cm

Design Rules of Thumb

- rc delays should be considered when $t_{pRC} > t_{pgate}$ of the driving gate

$$L_{crit} > \sqrt{(t_{pgate}/0.38rc)}$$

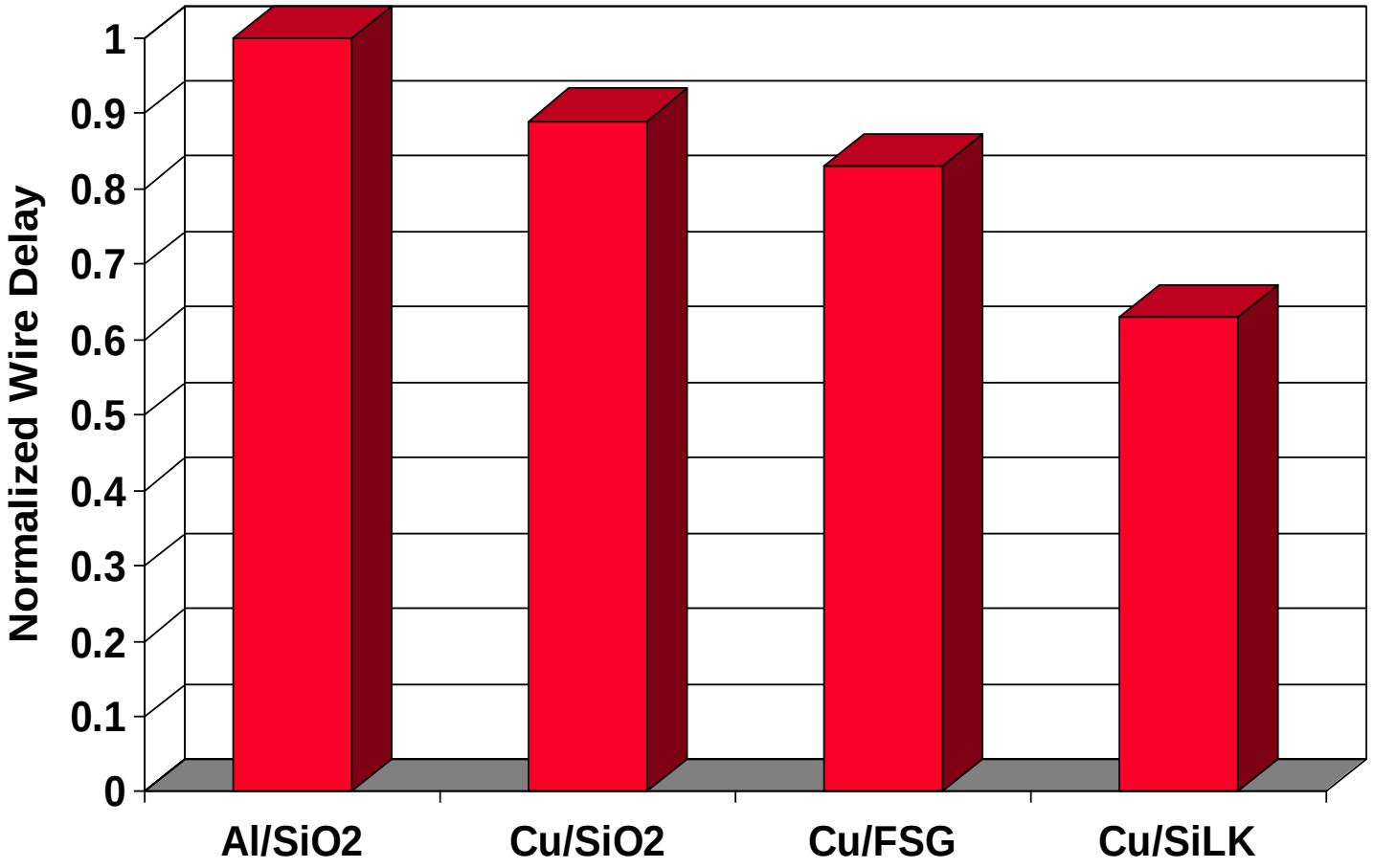
  - actual L_{crit} depends upon the size of the driving gate and the interconnect material

- rc delays should be considered when the rise (fall) time at the line input is smaller than RC, the rise (fall) time of the line

$$t_{rise} < RC$$

  - when not met, the change in the signal is slower than the propagation delay of the wire so a lumped C model suffices

Comparison of Wire Delays



جلسه آینده

- درس بعدی
  - مدار های منطقی ترتیبی