VLSI System Design

Department of Electrical Engineering
Amirkabir University of Technology (Tehran Polytechnic)
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Detailed Topics:

1. **Introduction to Digital Integrated Circuits**
   - 1.1. A Historical Perspective
   - 1.2. Design Issues in Digital Integrated Circuits
   - 1.3. Quality Metrics of a Digital Design
2. **CMOS Technology Processing and Layout**
   - 2.1. Manufacturing CMOS Integrated Circuits
   - 2.2. Design Rules
   - 2.3. Packaging Integrated Circuits
3. **MOS Modeling**
   - 3.1. The Threshold Voltage, Operation in Different Regions and I/V Characteristics
   - 3.2. Second-Order Effects: Body Effect, Channel Length Modulation
   - 3.3. Short-Channel Effects: Mobility Degradation, Velocity Saturation
   - 3.4. Parasitic Capacitances
   - 3.5. Models for Hand Analysis
   - 3.6. CMOS Latch-Up
   - 3.7. SPICE Models
   - 3.8. Technology Scaling
4. **Interconnects in CMOS Technology**
   - 4.1. Interconnect Parameters: Capacitance, Resistance, Inductance
   - 4.2. Electrical Wire Models: Lumped C Model, Lumped RC Model, Distributed RC Model
   - 4.3. Advanced Interconnect Techniques: Reduced Swing, Current Mode
   - 4.4. SPICE Wire Models
5. **The CMOS Inverter**
   - 5.1. The Static Behavior: Switching Threshold, Noise Margins, Robustness
   - 5.2. The Dynamic Behavior: Propagation Delay, Device Sizing for a Chain of Inverters, Optimal Buffer Design
   - 5.3. Power Dissipation: Dynamic, Switching Activity, Short-Circuit, Static or Leakage, Energy-Delay Product, Analyzing Power Consumption Using SPICE
   - 5.4. Impact of Technology Scaling
6. **Combinational CMOS Logic Gates**
   - 6.1. Combinational vs. Sequential Logic
   - 6.2. Static CMOS Logic Design: Complementary CMOS, Ratioed Logic, Pass Transistor Logic
   - 6.3. Dynamic CMOS Logic: Basic Principles, Speed and Power Dissipation, Issues in Dynamic Logic Design, Cascading Dynamic Gates, Domino Logic

7. **Sequential Logic Circuits**
   - 7.1. Static Latches and Registers
   - 7.2. Dynamic Latches and Registers
8. **Timing Issues in Digital Circuits**
   - 8.1. Timing Classification of Digital Systems
   - 8.2. Synchronous Interconnect and Design
   - 8.3. Clock Distribution Techniques
   - 8.4. Self-Time or Asynchronous Circuit Design
9. **Verilog RTL Modeling of Digital Systems**
10. **Arithmetic and Logic Building Blocks**
    - 10.1. The Adders: Binary Adder, Full Adder
    - 10.2. The Multiplier
    - 10.3. The Shifter: Barrel Shifter, Logarithmic Shifter
11. **Memory Design in CMOS**
    - 11.1. Classification, Architectures and Building Blocks
    - 11.2. The Memory Core: Read-Only Memories (ROMs), Nonvolatile Read-Write Memories, Read-Write Memories (RAM)
    - 11.3. Peripheral Circuitry: Address Decoders, Sense Amplifiers, Voltage References, Drivers & Buffers, Timing and Control
    - 11.4. SRAM Design
12. **Testing of Digital Systems**
    - 12.1. Introduction, Test Procedure
    - 12.2. Design for Testability
    - 12.3. Test Pattern Generation

References:

1. J. M. Rabaey, A. Chandrakasan, and B. Nicolic, *Digital Integrated Circuits: A Design Perspective*, New Jersey: Prentice Hall, 2003 (**Primary Text**).
2. K. W. Martin, *Digital Integrated Circuit Design*, New York: Oxford University Press, 2000.
3. N. H. E. Weste and David Harris, *CMOS VLSI Design: A Circuit and Systems Perspective*. Third Edition, Boston: Addison-Wesley, 2005.
4. Z. Navabi, *Verilog Digital System Design*, New York: McGraw-Hill, 1999.
5. Class Notes and Selected Publications.

Requirement:

Electronics II

Grading:

Homeworks and Design Projects: 30%

Midterm Exam: 30%

Final Exam: 40%