Data Converters

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Overall Topics:

1. **Fundamentals and Characterization of Data Converters (4 Lectures)**
2. **Switched-Capacitor Circuits (4 Lectures)**
3. **Nyquist-Rate D/A Converters (2 Lectures)**
4. **CMOS Comparators (2 Lectures)**
5. **Nyquist-Rate A/D Converters (7 Lectures)**
6. **Oversampling A/D Converters (6 Lectures)**
7. **Oversampling D/A Converters (3 Lectures)**
8. **Data Converter Testing (1 Lecture)**

Detailed Topics:

1. **Fundamentals and Characterization of Data Converters**
   - 1.1. Overall Block Diagram of A/D and D/A Converters
   - 1.2. Sampling in Time
     - 1.2.1. Ideal and Real Sampling
     - 1.2.2. Classes of Sampling: Nyquist-Rate, Oversampling, Undersampling
   - 1.3. Quantization in Amplitude: Transfer Function, Full-Scale Input, LSB, Gain of a Quantizer, Modeling of Quantization Error, Dynamic Range of an N-bit Quantizer
   - 1.4. D/A Converter Transfer Characteristic: Ideal D/A Converter, Ideal and Real Reconstruction, Signed Codes
   - 1.5. Performance Metrics
     - 1.5.1. Static: Monotonicity, Offset, Gain Error, DNL, INL
     - 1.5.2. Dynamic: SNR, SNDR, THD, SFDR, DR, ERB, Clock Jitter, Settling Time, Glitch, MTPR, ENOB, etc.
     - 1.5.3. Accuracy, Resolution, Converter Speed
   - 1.6. Simulation of Data Converters: Discrete Fourier Transform Basics, Windowing
   - 1.7. Data Converter Requirements for Communications and Other Applications
   - 1.8. State-of-the-Art Data Converters
2. **Switched-Capacitor Circuits**
   - 2.1. MOS Switch Design Techniques
     - 2.1.1. Basic MOS Switches
     - 2.1.2. Clock Feedthrough and Charge Injection
     - 2.1.3. Low-Voltage MOS Switch Design Techniques: Clock Boosting, Clock Bootstrapping
   - 2.2. Track and Hold Circuits: Charge Redistribution, Charge Conservation, Clock Generation, Flip-Around T/H

2.3. SC Difference Amplifiers
2.4. Switched-Capacitor Integrators
    2.4.1. SC Resistor Equivalent
    2.4.2. Parasitic Sensitive and Insensitive Architectures
    2.4.3. Finite DC gain
    2.4.4. Noise Analysis of an Integrator: Switches Noise or kT/C Noise, Opamp Noise, Correlated Double Sampling
2.5. Passive Charge Redistribution Networks
2.6. Switched-Capacitor Biquads

3. Nyquist-Rate D/A Converters

3.1. Reference Multiplication and Division: Voltage Division, Current Division, Charge Division
3.2. Binary-to-Thermometer Code Conversion
3.3. Decoder Based Architectures: Resistor String, Folded Resistor String, Singed Outputs
3.4. Binary-Weighted D/A Converters
    3.4.1. Binary-Weighted Resistor D/A Converters: R-2R Based Ladder
    3.4.2. Binary-Weighted Current-Steering
    3.4.3. Binary-Weighted Charge-Redistribution
3.5. Thermometer Coded D/A Converters: Resistive, Switched-Capacitor, Current-Steering
3.6. Hybrid or Segmented Architectures
3.7. A State-of-the-Art Design Example

4. CMOS Comparators

4.1. General Considerations and Performance Metrics
4.2. Multi-Stage Comparators
4.3. Latched Comparators
4.4. Design Techniques: Overdrive Test, Input-Referred Offset and Noise
4.5. A Survey on Latched Comparators, SR Latch
4.6. Offset Cancellation Techniques: Input Offset Cancellation, Output Offset Cancellation

5. Nyquist-Rate A/D Converters

5.1. Classes of Operation
5.2. Flash A/D Converters
    5.2.1. Overall Architecture
    5.2.2. Design Issues: Nonlinear Input Capacitive Loading, Resistor-String DC and AC Bowing, Signal and/or Clock Delay, Substrate and Power Supply Noise, Offset, Kickback Noise, Sparkles or Bubble Errors in Thermometer Code, Metastability
    5.2.3. A State-of-the-Art Design Example
5.3. Two-Step A/D Converters
    5.3.1. Basic Concept and Structure, Effect of Non-idealities, Accuracy Requirements, Digital Error Correction
    5.3.2. Two-Step Recycling and Subranging Architectures
5.4. Interpolating A/D Converters
5.5. Folding A/D Converters
    5.5.1. Basic Concept and Structure

5.5.2. CMOS Folder Realization and Accuracy Requirements

5.6. Folding and Interpolating A/D Converters

5.6.1. Architecture and Implementation Issues

5.6.2. A State-of-the-Art Implementation Example

5.7. Pipelined A/D Converters

5.7.1. Basic Block Diagram and Operation, General Analysis, Error Sources and Accuracy Requirements

5.7.2. Digital Calibration and/or Correction Techniques

5.7.3. Switched-Capacitor Implementation

5.7.4. Stage Scaling and Power Optimization

5.7.5. State-of-the-Art Implementation Examples

5.8. Integrating A/D Converters

5.9. Successive Approximation A/D Converters

5.10. Algorithmic A/D Converters

5.11. Time-Interleaved A/D Converters

5.12. Voltage to Frequency Converters

6. Oversampling A/D Converters

6.1. Basic Concepts, Oversampling

6.2. Feedback Modulators: Delta Modulation, Noise Shaping, Sigma-Delta Modulation

6.3. Sigma-Delta Modulators: First-Order, Error Compensation Model, High-Order Sigma-Delta Modulation

6.4. Realization of A Second-Order Sigma-Delta Modulator

6.4.1. Architecture, System Level Design

6.4.2. Switched-Capacitor Implementation

6.5. System Level Modeling of Circuit Non-idealities

6.5.1. Amplifier Finite and Nonlinear DC Gain

6.5.2. Amplifier Limited Output Swing

6.5.3. Finite Amplifier Bandwidth and Slew-Rate

6.5.4. Capacitance Mismatch

6.5.5. Clock Jitter

6.5.6. ADC Non-ideal Operation

6.5.7. DAC Non-ideal Operation

6.5.8. Shaping of Circuit Noise

6.6. High-Order Single-Stage ΣΔ Modulators: Distributed Feedback, Weighted Feedforward, Optimal NTF, System Level Design of a High-Order ΣΔ Modulator, A Design Example

6.7. Cascaded ΣΔ Modulators: General Architecture, Accuracy Requirements

6.8. Multi-Bit ΣΔ Modulators

6.8.1. DAC Realization

6.8.2. DAC Linearization Techniques: DEM Techniques, Calibration and Correction Techniques

6.9. Modulator Stability: Single-Bit Quantization, Multi-Bit Quantization

6.10. Bandpass and Quadrature ΣΔ A/D Conversion

6.11. Continuous-Time ΣΔ Modulators

6.12. Advanced Topics on ΣΔ Modulators

6.13. Decimation Filters

6.14. Design Examples and State-of-the-Art Implementations

7. Oversampling D/A Converters

7.1. Overall System

7.2. Digital ΣΔ Modulator Architectures and Implementation Issues

7.3. Interpolation Filters

7.4. Analog Post Processing

8. Data Converter Testing

8.1. Introduction, Test Board, Measurement Equipments

8.2. Test Considerations

References:

1. M. J. M. Pelgrom, *Analog-to-Digital Conversion*, Third Edition, Springer, 2017.
2. F. Maloberti, *Data Converters*, Springer-Verlag, The Netherlands, 2007.
3. S. Pavan, R. Schreier, and G. C. Temes, *Understanding Delta-Sigma Data Converters*, IEEE Press/Wiley, Second Edition, 2017.
4. B. Razavi, *Principles of Data Conversion System Design*, IEEE Press, 1995.
5. T. C. Carusone, D. A. Johns, and K. W. Martin, *Analog Integrated Circuit Design*, John Wiley & Sons, Second Edition, 2012.
6. R. J. van de Plassche, *CMOS Integrated Analog-to-Digital and Digital-to-Analog Converters*, Kluwer Academic Publishers, Second Edition, 2003.
7. J. M. de la Rosa, *Sigma-Delta Converters, Practical Design Guide*, Second Edition, IEEE Press/Wiley, 2018.
8. A. Rodriguez-Vazquez, F. Medeiro, and E. Janssens (Eds.), *CMOS Telecom Data Converters*, Kluwer Academic Publishers, 2003.
9. M. Gustavsson, J. Jacob Wikner, and N. N. Tan, *CMOS Data Converters for Communications*, Kluwer Academic Publishers, 2002.
10. S. R. Norsworthy, R. Schreier, and G. C. Temes (Eds.), *Delta-Sigma Data Converters*, IEEE Press, 1997.
11. B. Razavi, *Design of Analog CMOS Integrated Circuits*, McGraw-Hill, Second Edition, 2017.
12. W. Kester, *The Data Conversion Handbook*, Newnes, 2005.
13. Class Notes and Selected Publications.

Requirement:

Analog Integrated Circuits or Electronics III

Grading:

Homeworks: 10%

Design Projects: 25%

Midterm Exam: 30%

Final Exam: 35%