

Equalization-Based Digital Background Calibration Technique for Pipelined ADCs

Behzad Zeinali, Tohid Moosazadeh, Mohammad Yavari, *Member, IEEE*, and
Angel Rodriguez-Vazquez, *Member, IEEE*

Abstract—In this paper, we present a digital background calibration technique for pipelined analog-to-digital converters (ADCs). In this scheme, the capacitor mismatch, residue gain error, and amplifier nonlinearity are measured and then corrected in digital domain. It is based on the error estimation with nonprecision calibration signals in foreground mode, and an adaptive linear prediction structure is used to convert the foreground scheme to the background one. The proposed foreground technique utilizes the LMS algorithm to estimate the error coefficients without needing high-accuracy calibration signals. Several simulation results in the context of a 12-b 100-MS/s pipelined ADC are provided to verify the usefulness of the proposed calibration technique. Circuit-level simulation results show that the ADC achieves 28-dB signal-to-noise and distortion ratio and 41-dB spurious-free dynamic range improvement, respectively, compared with the noncalibrated ADC.

Index Terms—Adaptive linear prediction, digital background calibration, LMS algorithm, pipelined ADCs.

I. INTRODUCTION

PIPELINED analog-to-digital converters (ADCs) are the best candidate for medium to high resolutions between 10 and 16 bits and conversion rates between 10 and 250 MHz [1]–[4]. To achieve higher conversion rates, nanometer CMOS technologies are usually utilized where the intrinsic gain of transistors is very poor. On the other hand, in the pipelined ADCs, the resolution is mainly limited by the capacitor mismatch and limited and nonlinear DC gain in the amplifiers. Therefore, calibration techniques are needed to achieve both high speed and high resolution where they can also reduce the power consumption and analog circuits' complexity [1]–[4]. Moreover, digital calibrations are very interesting because digital circuits are almost fast and reliable in nanometer CMOS technologies.

The digital calibration algorithms are classified into two main foreground and background categories. The foreground calibration scheme interrupts the ADCs normal conversion whereas in background techniques, the normal operation of the

ADC is not interrupted. Nonetheless, in background schemes, the isolation of the calibration process from the normal operation of the ADC is an important issue [3].

The calibration techniques can also be categorized as the correlation-based [1]–[3], statistical-based [4], and equalization-based [5]–[7] approaches. Both the correlation- and statistical-based algorithms utilize the statistical properties of orthogonal pseudorandom calibration signals resulting in a very long convergence time. In equalization-based schemes, the errors are generally measured by calibration signals. But, the precision of these signals in nanometer CMOS technologies is an important issue. Several techniques have been proposed to alleviate this problem [5]–[7]. Nonetheless, they still need accurate analog elements or additional calibration cycles.

In this paper, a new equalization-based digital background calibration algorithm for pipelined ADCs is presented without needing any accurate calibration signal. It uses the adaptive LMS algorithm [8] to estimate the errors in foreground mode. To convert any foreground calibration scheme to a background one, different algorithms such as those presented in [9] and [10] can be used. In these techniques, some input samples are occasionally skipped to create time slots for calibration and then the missing input samples are digitally filled using a nonlinear digital interpolation filter. However, employing a nonlinear interpolation filter makes the maximum input signal frequency to be limited. Also, there is a large delay between the sampled input and its corresponding digital output due to using a relatively higher order finite-duration impulse response (FIR) filter. To alleviate these problems, a new digital background structure is proposed by using an adaptive linear predictor to fill the skipped input samples randomly.

The paper is organized as follows. In Section II, the structure of pipelined ADCs and their nonidealities are briefly reviewed. The proposed new calibration technique in foreground mode is presented in Section III. In Section IV, a new background calibration scheme is proposed. The ADC circuit implementation details are discussed in Section V. Section VI provides the circuit-level simulation results, and finally, Section VII concludes the paper.

II. PIPELINED ADC STRUCTURE

A. ADC Architecture

The general block diagram of pipelined ADCs includes several low-resolution stages to produce the digital output, D_{out} , where the final stage is usually a Flash ADC [6]. The

Manuscript received June 1, 2012; revised December 2, 2012; accepted January 13, 2013. Date of publication February 12, 2013; date of current version January 17, 2014.

B. Zeinali, T. Moosazadeh, and M. Yavari are with the Department of Electrical Engineering, Integrated Circuits Design Laboratory, Amirkabir University of Technology, Tehran 15914, Iran (e-mail: behzad_zeinali@aut.ac.ir; tmoosazadeh@aut.ac.ir; myavari@aut.ac.ir).

A. Rodriguez-Vazquez is with the Institute of Microelectronics of Seville, Centro Nacional de Microelectrónica, Universidad de Sevilla, Seville 41004, Spain (e-mail: angel@imse-cnm.csic.es).

Color versions of one or more of the figures in this paper are available online at <http://ieeexplore.ieee.org>.

Digital Object Identifier 10.1109/TVLSI.2013.2242208

stages (except the flash ADC) are composed of a sub-ADC and a multiplying digital-to-analog converter (MDAC). The sub-ADC compares the stage analog input with reference voltages and generates the corresponding stage digital output. The digital output is selected from $\{-1, 0, 1\}$ for 1.5-bit stages and $\{-1.5, -0.5, 0.5, 1.5\}$ for 2-bit back-end flash ADC. The front-end sample and hold amplifier (SHA) circuit is not generally utilized due to its additional noise and power consumption.

The capacitor non-flip-around (CNFA) MDAC structure is utilized in this paper instead of the mostly used capacitor flip-around (CFA) MDAC scheme for the ADC stages. This is because, in this scheme, the input signal and digital-to-analog converter (DAC) voltage exhibit the same errors and hence the capacitor mismatch and amplifier gain error are modeled in the same way [6]. Nonetheless, for more generality, all of the steps are also briefly explained for CFA MDAC structure.

The fully differential circuit implementation of a 1.5-bit/stage with CNFA structure is shown in Fig. 1 where V_{CMi} is the amplifier input common-mode voltage and C_P is the equivalent parasitic capacitance at the amplifier input. In sampling phase Φ_1 , the input signal V_{ini} is sampled in sampling capacitors C_S , while the amplifier output is connected to the output common-mode voltage V_{CMo} . In the next phase Φ_2 , the sampled input signal is transferred to the output by feedback capacitors C_F . In this phase, the DAC operation is also performed.

B. MDAC Modeling

In this section, the effects of capacitor mismatch and amplifier imperfections in the CNFA structure are modeled. In this model, the impact of error due to eliminating the front-end SHA, especially in the first stage, is neglected since it is compensated by time matching between the MDAC and sub-ADC paths [11]. The distortion introduced by a practical residue amplifier could be modeled as a memoryless and weakly nonlinear function of the amplifier's input voltage. So, it can be approximated accurately by its n first Taylor series coefficients where $n \leq 5$ is common [1], [2], although, in some previous reports, nonidealities greater than third order are neglected [6]. The following calculations are performed by considering nonlinearities up to fifth order while they can be easily extended for any arbitrary order.

The open-loop I–O static characteristics of a fully differential amplifier in the i th stage can be approximated by a fifth-order polynomial as [6]

$$V_{outi} \approx A \left(V_x + \gamma_1 V_x^3 + \gamma_2 V_x^5 \right) \quad (1)$$

where A and V_x are the amplifier DC gain and its input voltage, respectively, and γ_1 and γ_2 are the gain nonlinearity coefficients. When the amplifier is placed in a closed-loop configuration, by neglecting higher order harmonics, the inverse of (1) can be approximated by another fifth-order polynomial as

$$V_x \approx \rho_1 V_{outi} + \rho_3 V_{outi}^3 + \rho_5 V_{outi}^5 \quad (2)$$

$$\rho_1 = \frac{1}{A}, \quad \rho_3 = \frac{-\gamma_1}{A^3}, \quad \rho_5 = \frac{3\gamma_1^2 - \gamma_2}{A^5}. \quad (3)$$

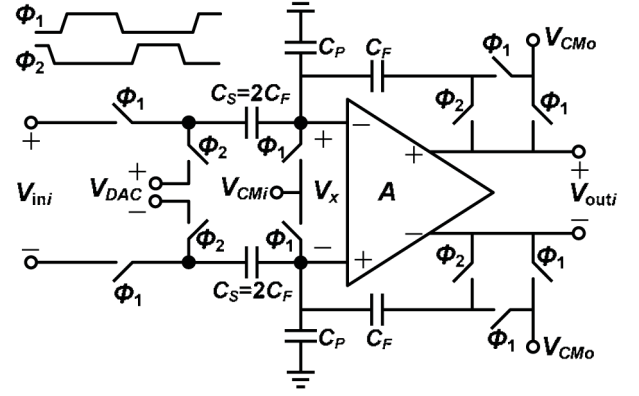


Fig. 1. Fully differential circuit implementation of a CNFA MDAC.

The I–O transfer function of the fully differential CNFA MDAC shown in Fig. 1 is given by

$$V_{ini}[n-1] - V_{DAC}[n] = \frac{C_F}{C_S} V_{outi}[n] - \left(\frac{C_S + C_F + C_P}{C_S} \right) V_x[n]. \quad (4)$$

By assuming $C_F/C_S = 0.5 + \varepsilon$ and substituting the relations (2) and (3) in (4), we have

$$V_{ri} = (0.5 + \varepsilon - k) V_{outi} + \frac{\gamma_1 k}{A^2} V_{outi}^3 + \frac{(3\gamma_1^2 - \gamma_2)k}{A^4} V_{outi}^5 \quad (5)$$

where k and V_{ri} are defined as $(1.5 + \varepsilon + C_F/C_S)/A$ and $V_{ini} - V_{DAC}$, respectively. But, a model as $V_{outi} = f(V_{ri})$ is more interesting, so the inverse of (5) is defined by another fifth-order polynomial as

$$V_{outi} \approx 2 \left[(1 - \alpha_1) V_{ri} - \alpha_3 V_{ri}^3 - \alpha_5 V_{ri}^5 \right] \quad (6)$$

where α_1 , α_3 , and α_5 are the MDAC imperfection coefficients. The error coefficients can be different in ADC's stages where their indexes associated with stage numbers are omitted in (6) for simplicity. Equation (6) indicates that in the calibration of the CNFA MDAC, the estimation of three different coefficients is required.

In CFA MDAC topology, there are two different paths and consequently two different errors for the input signal and sub-DAC output voltage. So, its modeling, such as relation (6), needs the estimation of 12 error coefficients. Nonetheless, as presented in [7], if V_{ini} is modeled as a function of V_{outi} and V_{DAC} , that is, $V_{ini} = g(V_{outi}, V_{DAC})$, the number of required error coefficients is significantly reduced. In this case, the capacitor mismatch is considered as $C_F = C(1 + \delta)$ and $C_S = C(1 - \delta)$ while the amplifier imperfection is modeled by (2). So, the sampled analog input is estimated as

$$V_{ini} = \frac{(1 - \delta)}{2} V_{DAC} + \left[\frac{(1 + \delta)}{2} - \rho_1 \right] V_{outi} - \rho_3 V_{outi}^3 - \rho_5 V_{outi}^5. \quad (7)$$

As seen from (7), the CFA MDAC needs the estimation of four coefficients while three coefficients are used in CNFA MDAC for the same error. So, in this paper, the CNFA MDAC structure is utilized to simplify the calibration process.

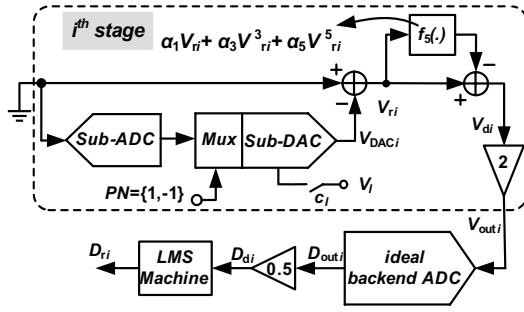


Fig. 2. i th stage in the calibration mode in ECS method.

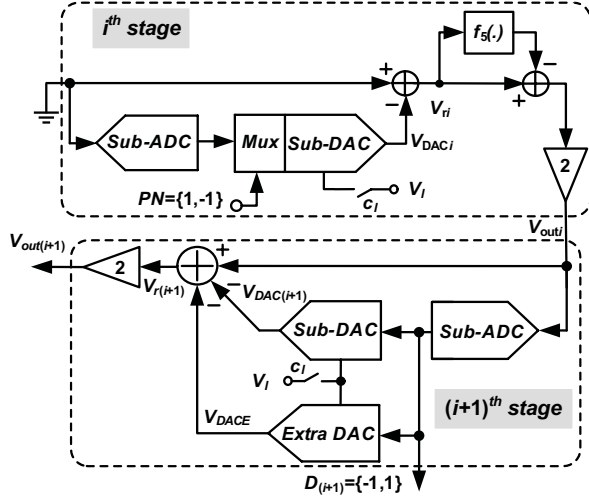


Fig. 3. Proposed error estimation method for calibration of i th stage implemented in CNFA MDAC structure.

III. CALIBRATION ALGORITHM IN FOREGROUND MODE

A. Error Estimation With Calibration Signals

To explain the error estimation with calibration signals (ECS) method as illustrated in Fig. 2, the ADC's i th stage is modeled by (6), and the calibrated back-end stages are lumped as an ideal ADC. If the calibration procedure begins from the final stages and moves to the first stages, this condition will be easily satisfied. In Fig. 2, V_{ri} is the residue voltage of the i th stage, V_{di} is its distorted value, and V_{out_i} is the stage analog output. Also, D_{ri} , D_{di} , and D_{out_i} are N vectors defined as their N -bit digital values, respectively, where N is the back-end ADC number of bits. Since the LMS algorithm is utilized to estimate the model parameters in relation (6), at least four independent equations are required [8]. According to Fig. 2, the stage's sub-DAC utilizes eight different voltage levels ($\pm V_l$ for $l = \{1, 2, 3, 4\}$) in the calibration mode. They are applied by independent control signals of PN and c_l . PN is a random two-level signal altering between -1 and 1 to select the sign of the calibration signals and c_l specifies the analog value of the calibration signals.

The accuracy of estimation improves with increasing the number of calibration voltages and their distances, since this decreases the minimum LMS error [8]. The main drawback of this method is that the calibration signals should be implemented at least with the back-end ADC accuracy. In conventional implementations, voltage levels with more

than 10-bit accuracy cannot be easily realized [7]. So, some methods are needed to alleviate the high accuracy requirement in calibration signals.

B. Proposed Calibration Method

In this section, the proposed method is described for 1.5-bit/stage with CNFA MDAC topology. Fig. 3 shows the proposed method for the calibration of i th stage named the error estimation with nonprecision calibration signals. The calibration process recursively works backward through pipelined stages. The procedure is explained for the state of $PN = -1$. So, firstly the input of the i th stage is connected to the ground and $PN = -1$ is injected. In this situation, $V_{DAC_i} = -(V_l + \varepsilon_l)$ for $l = \{1, 2, 3, 4\}$ where V_l is the desired voltage level and ε_l is a random error due to the fabrication process. By substituting $V_{ri} = -V_{DAC_i}$ in the MDAC model and assuming $V_l \gg \varepsilon_l$, the output of the i th stage will be

$$V_{out_i} \approx 2 \left[(1 - \alpha_1)(V_l + \varepsilon_l) - \alpha_3 V_l^3 - \alpha_5 V_l^5 \right]. \quad (8)$$

When $|V_l| > 0.125 V_{ref}$, the signal given by (8) is entered to the $(i + 1)$ th stage and generates the digital output of $D_{(i+1)} = 1$. In contrary to the conventional pipelined ADCs, the same V_l is utilized in the sub-DAC of the $(i + 1)$ th stage and hence we have $V_{DAC(i+1)} = (V_l + \varepsilon_l)$. Furthermore, as shown in Fig. 3, one additional voltage level, $V_{DACE} = (V_l + \varepsilon_l)$, is subtracted from the input of $(i + 1)$ th stage. So, the residue voltage of the $(i + 1)$ th stage will be

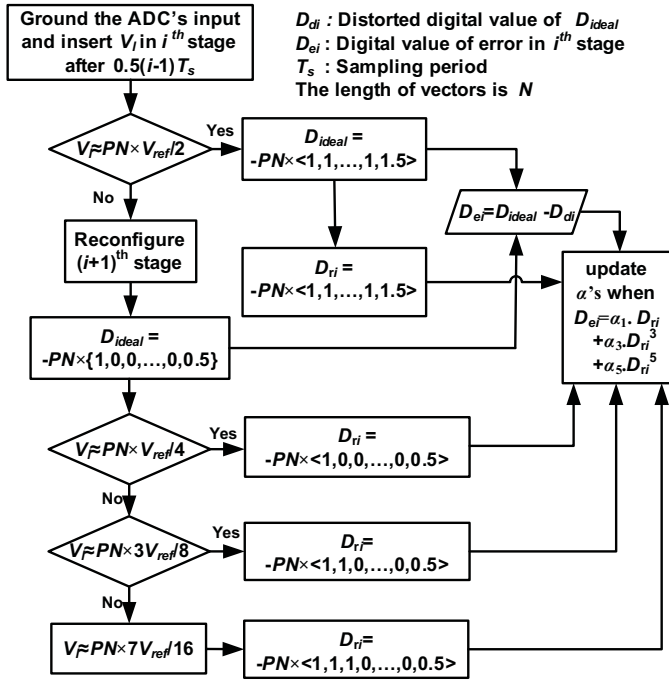
$$\begin{aligned} V_{r(i+1)} &= V_{out_i} - V_{DAC(i+1)} - V_{DACE} \\ &= -2 \left[\alpha_1 (V_l + \varepsilon_l) + \alpha_3 V_l^3 + \alpha_5 V_l^5 \right] \\ &\equiv -2(\alpha_1 \varepsilon_l + V_{ei}) \end{aligned} \quad (9)$$

where V_{ei} is the error due to the i th-stage nonidealities. In system level, subtracting the additional voltage level is equivalent to add an extra 1-bit DAC in the $(i + 1)$ th stage using the $(V_l + \varepsilon_l)$ voltage level. As seen in (9), the extra DAC output, V_{DACE} , would be subtracted from the $(i + 1)$ th-stage input in the sampling phase to attenuate ε_l by α_1 . So, by using this configuration, the effect of nonprecision calibration signals is significantly alleviated.

Next, an equation should be derived for D_{di} because according to Fig. 2, it is used in the LMS machine to estimate the value of D_{ri} . In an ideal ADC, V_{ei} , and consequently, its digital value D_{ei} , will be zero. So, according to (9), independent of the V_l value, the $(N - 1)$ -bit back-end ADC digitizes the value of $\alpha_1 \varepsilon_l$ which is negligible. In this situation, D_{di} is also denoted by D_{ideal} . It can be easily shown that D_{ideal} is equal to $\langle 1, 0 \dots 0, 0.5 \rangle$ where $\langle \cdot \rangle$ is defined as the bit alignment operation. It means that the $(i + 1)$ th and 2-bit flash stages generate digital outputs equal to 1 and 0.5, respectively, and the digital code produced in other stages is 0. On the other hand, in a nonideal ADC, the i th stage feeds a nonzero error into the back-end ADC resulting in D_{di} as

$$D_{di} = D_{ideal} - D_{ei} = D_{ideal} - \left(\alpha_1 D_{ri} + \alpha_3 D_{ri}^3 + \alpha_5 D_{ri}^5 \right). \quad (10)$$

In driving (10), this fact that $V_{ri} = -V_{DAC_i} = -V_l$ was used. In (10), D_{ideal} is independent of V_l while $\alpha_1 D_{ri} +$

Fig. 4. Proposed procedure for calibration of i th stage.

$\alpha_3 D_{ri}^3 + \alpha_5 D_{ri}^5$ depends on the value of V_i . So, the different independent equations can be achieved by changing the value of V_i where D_{ri} is altered and D_{ideal} is constant. For different values of V_i , D_{ideal} and D_{ri} are shown in Fig. 4. In this figure, the values of V_i are specified for different quantities of D_{ri} . For instance, in the case of $V_i = 3 V_{ref}/8$, the value of D_{ri} is equal to $\langle -1, -1, 0 \dots 0, -0.5 \rangle$ which is extracted from a conventional ADC. Also, it should be regarded that the DAC voltages from the $(i+2)$ th stage to the end are chosen between $\{-V_{ref}/2, 0, V_{ref}/2\}$ similar to the conventional pipelined ADCs. Therefore, in the i th-stage calibration, it is enough to add an extra 1-bit DAC in the $(i+1)$ th stage and use the same voltage levels in the i th and $(i+1)$ th stages.

For the circuit implementation of the proposed method, when the i th stage is under calibration, the MDAC of the $(i+1)$ th stage is reformed as in Fig. 5 where the fully differential circuit implementation of the extra 1-bit DAC is shown. During i th-stage calibration, an additional V_i is subtracted from the $(i+1)$ th-stage input in its sampling phase Φ_1 , and so it does not need a higher resolution DAC. As shown in Fig. 5, this extra DAC is implemented in the MDAC structure with only four additional switches. The switches turn on in Φ_2 phase and add some extra series resistance in the amplifying path and hence degrading the stage amplifier settling performance. Besides, such implementation needs that the amplifier input and output common-mode voltages to be the same.

For CFA MDAC, the relation (7) is utilized to model the i th stage, and the calibration procedure is performed in two steps. In the first step, the calibration signals of $|V_i| < V_{ref}/2$ are applied to the i th stage where the stage is configured as a multiply-by-two circuit. In other words, V_{DAC} is zero in (7) and the remained error coefficients can be estimated as

$$D_l = \left[\frac{(1+\delta)}{2} - \rho_1 \right] D_{ri} - \rho_3 D_{ri}^3 - \rho_5 D_{ri}^5 \quad (11)$$

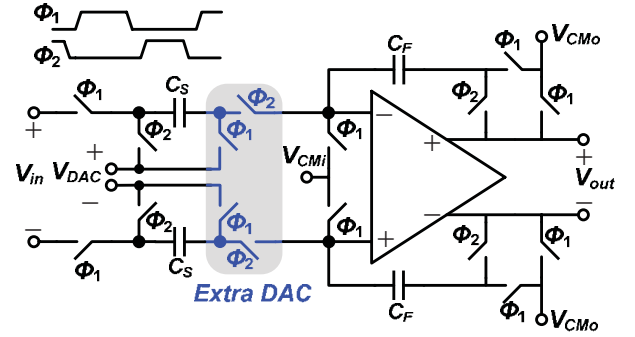


Fig. 5. Circuit implementation of extra 1-bit DAC in the CNFA MDAC structure.

where D_l is the digital equivalent of V_l . In this case, V_{DAC} in $(i+1)$ th and $(i+2)$ th stages is selected equal to V_l where the extra DAC voltages are subtracted through C_F and C_S capacitors in $(i+1)$ th stage and C_S capacitor in $(i+2)$ th stage. It could be easily proved that ϵ_l will be attenuated by ρ_1 . In the second step, the coefficient of V_{DAC} in (7) is estimated. In this case, V_{ini} is forced to zero and the calibration signal is applied through sub-DAC path. So, in this case, the estimation of error coefficient is similar to the CNFA structure.

For the case of n -bit stages, there are 2^n sampling units resulting in $(2^n - 1)$ different error coefficients in sub-DAC's path. Also, there are three error coefficients due to the amplifier nonidealities (by supposing a fifth-order modeling). However, to utilize the proposed method in multibit-per-stage case, the errors in sub-DAC should be firstly calibrated. So, using a linear DAC is a simple way and the best alternative is the dynamic element matching DAC [1], [2]. By using a linear DAC, the errors due to the amplifier nonidealities can be calibrated by the proposed method as well.

C. LMS-Based Coefficient Extraction

The LMS is a simple form of the steepest descent algorithm [8] where the correlation of error and input vector is replaced by a one-point sample multiplication. In this way, the parameters of (10) are estimated as

$$e(n) = D_{di}(n) - D_{ideal}(n) - \sum_{k=\{1,3,5\}} \alpha_k(n) D_{ri}^k(n)$$

$$\alpha_k(n+1) = \alpha_k(n) + \mu_k D_{ri}^k(n) e(n) \quad k = \{1, 3, 5\} \quad (12)$$

where n is the update index and μ 's are the update step sizes of the LMS algorithm in coefficient extraction. The same procedure can also be done in the case of (11) as follows:

$$\begin{aligned} \text{First step: } e_1(n) &= D_l(n) - \left[\frac{(1+\delta)}{2} - \rho_1 \right] D_{ri} \\ &+ \sum_{k=\{3,5\}} \rho_k(n) D_{ri}^k(n) \\ \alpha(n+1) &= \alpha(n) + \mu_\alpha D_{ri}(n) e_1(n) \\ \rho_k(n+1) &= \rho_k(n) + \mu_k D_{ri}^k(n) e_1(n) \quad k = \{3, 5\}. \end{aligned}$$

$$\text{Second step: } e_2(n) = \frac{\overbrace{(1-\delta)}^{\beta}}{2} D_l(n) + \alpha(n) D_{ri} - \sum_{k=\{3,5\}} \rho_k(n) D_{ri}^k(n)$$

$$\beta(n+1) = \beta(n) + \mu \beta D_l(n) e_2(n). \quad (13)$$

In [8], the acceptable interval for the update step sizes is calculated such that it guarantees the stability of LMS algorithm. Here, the update parameters are selected using the relation given in [8] and by considering the compromise between the convergence time and the steady-state error.

IV. BACKGROUND CALIBRATION METHOD

A. Conventional Background Structure

Tracking time-dependent variations in ADC performance requires the calibration process to work continuously. It means the background calibration is inevitable. There are several structures recommended to change the foreground methods to their corresponding background versions. The nonlinear interpolation method [6], [9], [10] suffers from the large delay between the sampled input and its corresponding digital output. Besides, this limits the maximum input signal frequency. The split structure [3] has the matching problem between the channels. The nested structure [12] needs extra power and area consumption in the reference ADC. Also, queue-based structures [13] suffer from the extra power consumption and silicon die area. In the following sections, a new method with prominent features is proposed to achieve an efficient background calibration scheme.

B. Digital Adaptive Prediction Structure

The linear prediction of a signal using an FIR filter is defined by

$$D_{\text{predicted}}(n) = \sum_{i=1}^L D_{\text{in}}(n-i) w_i \quad (14)$$

where L is the prediction order and w_i 's are the filter coefficients. Also, $D_{\text{predicted}}$ and D_{in} denote the predictor's output and input, respectively. In prediction concept, the n th sample of the input signal is predicted by previous L samples. The prediction error is defined as the difference between (14) and the n th sample of the input signal. When this error converges to the minimum value, the optimal value of the filter coefficients is achieved. There are several methods to estimate the optimal value of w_i 's [8]. One useful and common method is to use an adaptive algorithm.

Here, by using the adaptive linear prediction, a background calibration structure is proposed in digital domain as shown in Fig. 6. While the ADC works in the normal conversion mode, the predictor updates its weight vector to minimize the error between the input signal and the desired value. The input vector and the desired value at the n th sample are as follows:

$$\begin{aligned} D_{\text{in}}(n) &= [D_{\text{out}}(n-1), D_{\text{out}}(n-2), \dots, D_{\text{out}}(n-L)]^T \\ D_{\text{desired}}(n) &= D_{\text{out}}(n) \end{aligned} \quad (15)$$

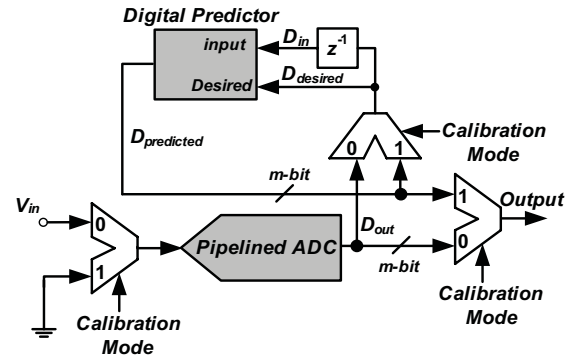


Fig. 6. Proposed background calibration by using the prediction structure.

where $D_{\text{out}}(n)$ is the ADC's output at the n th input sample and T denotes the transpose operation. When the ADC enters into the calibration mode, the predictor output is used as ADC's digital output and $D_{\text{desired}}(n) = D_{\text{predicted}}(n-1)$ in (15).

To validate the performance of the proposed predictor in different calibration conditions, several simulation scenarios are examined. The filter length and skipping rate are two effective parameters on the predictor performance. Moreover, the skipping rate affects the calibration process. As the skipping rate is increased, the calibration time is decreased, while the predictor performance is also decreased.

The MSE criterion between the output of the ideal ADC and the proposed background structure is utilized to evaluate the predictor performance. The MSE is defined as

$$\text{MSE} = \frac{1}{N} \sum_{n=1}^N |D_{\text{ideal}} - D_{\text{proposed}}|^2 \quad (16)$$

where D_{ideal} and D_{proposed} are the outputs of an ideal 12-bit ADC and the ADC calibrated by the proposed architecture, respectively. In Fig. 7, the MSE is sketched for different skipping rates and ADC analog input frequencies where the filter length is 64. By skipping 10% of input signal samples, the maximum predictor MSE is below -75 dB in the Nyquist band. The MSE of the adaptive linear predictor is also sketched for different filter lengths and analog input signal frequencies in Fig. 8. As is seen, an adequate performance in the whole of input frequency band is achieved by a filter length of 64. By this selection, the predictor has the maximum MSE of -70 dB for Nyquist frequency although a proper performance in the middle input frequency is also achieved by a lower filter length. As seen in Figs. 7 and 8, the proposed adaptive linear predictor used to convert the foreground calibration algorithm to a background scheme can recover the skipped samples in the Nyquist band with a proper performance. Furthermore, the behavior of the calibration routine for input frequencies in the second Nyquist zone is almost similar to the Nyquist band. Moreover, because of using the prediction algorithm in the background structure, no further latency will be added to the digital outputs of the calibrated pipelined ADC.

To evaluate the performance of the proposed background structure for other input signals, an autoregressive (AR) signal is utilized. The AR signal shown in Fig. 9(a) is obtained by filtering a white zero mean Gaussian random sequence

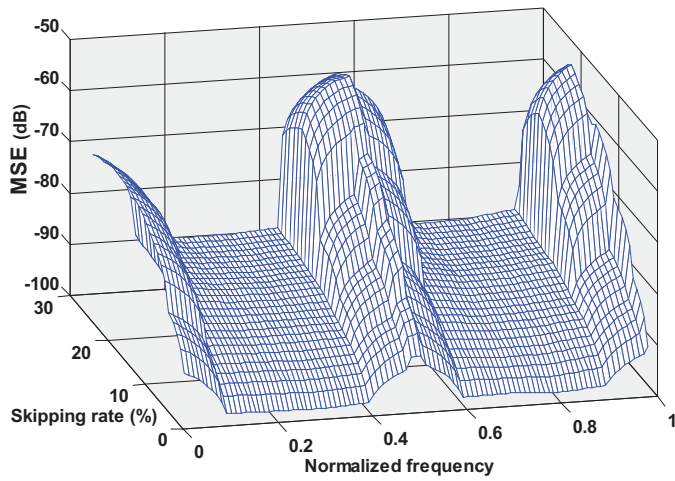


Fig. 7. MSE for different input signal frequencies and skipping rates of input samples.

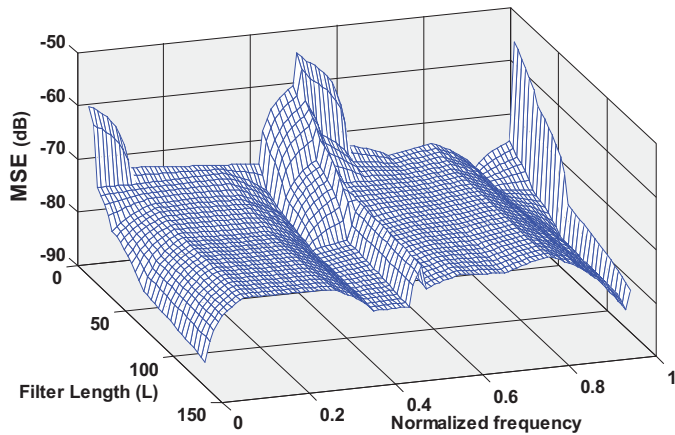


Fig. 8. MSE for different input signal frequencies and predictor lengths.

through a sixth-order all-pole system. Fig. 9(b) shows the predictor convergence behavior by considering the MSE criterion defined as the difference between the input signal and the predictor output. Also, the performance of the background calibrated ADC is evaluated by using the MSE that is equal to -53 dB for a 10% skipping rate. The MSE can be improved by reducing the skipping rate but with an increased convergence time.

V. CIRCUIT IMPLEMENTATION

To prove the usefulness of the proposed calibration algorithm, a prototype 12-bit 100-MS/s pipelined ADC is designed in a 90-nm CMOS technology with 1.2-V power supply. The ADC input SHA is eliminated by time matching between the first-stage MDAC and sub-ADC paths [11].

A. Amplifiers and Comparators

A two-stage Miller-compensated operational amplifier, shown in Fig. 10(a), comprising of two simple common-source stages is used to realize the MDACs. The cross-coupled loads are used in the first stage to improve the amplifier DC gain as well as to establish the common-mode voltage at

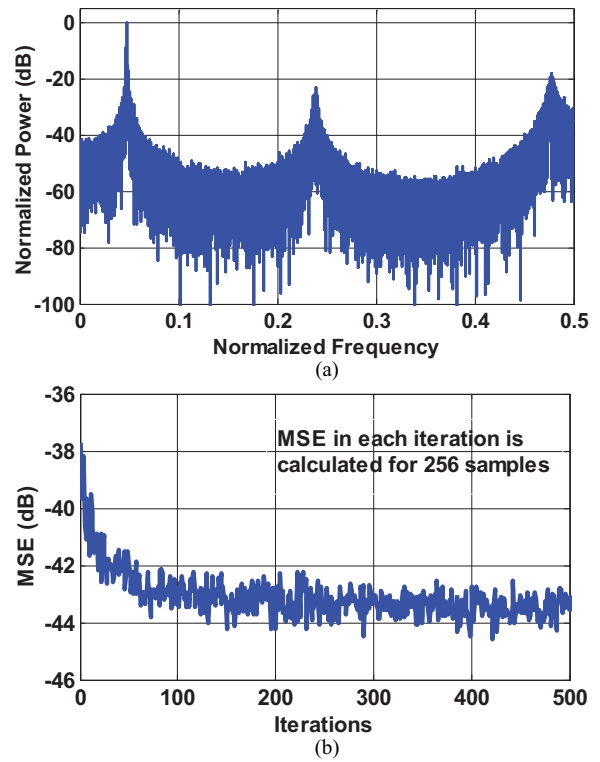


Fig. 9. (a) Spectrum of the AR input signal. (b) Predictor MSE.

the first-stage output. A simple switched-capacitor common-mode feedback circuit is used to control the second-stage common-mode voltage. In sampling phase, both the first and second stages of the amplifier are reset. Minimum channel length devices are used in amplifying transistors to achieve higher bandwidth larger than 1.5 GHz in the first-stage MDAC. However, this limits the DC gain to only 38 dB. To reduce the power consumption and die area, the capacitors, amplifier devices, and bias currents are scaled down in the next stages.

The time-matching requirement without the input SHA needs fast regenerative comparators in the first stage to ensure that the first MDAC has enough time for settling. A simple dynamic latch [14] shown in Fig. 10(b) is employed with a designed regeneration time less than 0.25 ns to realize the sub-ADCs.

B. Reformed Decoder for Stage Sub-ADC

Another important point in the circuit implementation is the time to produce the DAC voltage sign. In conventional MDAC structure, the stage digital output is produced at the beginning of the amplification phase, so, the DAC voltage sign is distinguished in this phase. However, in the proposed structure shown in Fig. 5, the circuit needs the DAC voltage sign in the sampling phase when it is in the calibration mode. So, the sub-ADC structure has been altered to eliminate this problem. As mentioned in Section III, in the calibration of the i th stage when PN is equal to -1 , the digital output of the $(i + 1)$ th stage must be 1 in order to the extra 1-bit DAC to alleviate the destructive effect of nonprecision calibration signals. Also, in $PN = 1$, the digital output must be -1 . So,

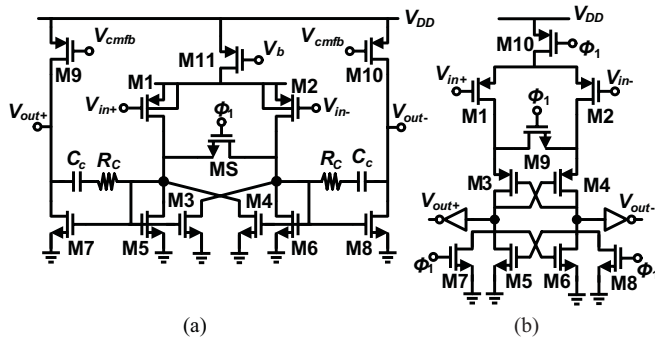


Fig. 10. (a) Amplifier architecture. (b) Dynamic latch.

with this information, we can produce the digital output of the $(i + 1)$ th stage without comparators. Hence, the decoder at the output of the stage sub-ADCs is reconstructed as Fig. 11. In this figure, Q_i and Q_{ib} are the comparator outputs and d_i is used as the multiplexer input in the sub-ADC configuration. When the $(i + 1)$ th stage is in the calibration mode ($C_{i+1} = 1$), the PN is injected to the sub-DAC input. Also, when the i th stage is in its calibration mode ($C_i = 1$), this configuration can produce the proper digital output in the $(i + 1)$ th stage.

Another point in circuit implementation is the necessity of shift in controller signals coming from the under calibration stage to its next stage. Due to a half-cycle difference between two consecutive stages, the calibration signals coming from the previous stage should also be shifted by a half-cycle.

C. Digital Implementation of the Predictor

To prove the adequate performance of the proposed adaptive linear prediction, it was implemented in MATLAB with fixed-point precision. To update the lattice filter coefficients, the Affine Projection Algorithm (APA) is utilized. The APA is based on affine subspace projections and it is a useful family of adaptive algorithms to speed up the convergence of the LMS algorithm especially for the colored signals. Whereas the LMS-type filter updates the weights based only on the current input vector, the APA updates the weights on the basis of the last N input vectors where N is the affine order. The recursive algorithm called pseudo APA with Gauss-Seidel recursion (GS-PAP) is utilized to simplify the implementation [15]. The computational complexity of the GS-PAP algorithm is almost $2L + 14N$ per sample, whereas LMSs complexity is $2L$ per sample. The further computational complexity is neglected against GS-PAP's improvements [15], especially in higher values of L , where in the interpolation concept, a filter length of 122 is necessary [6].

Fig. 12 shows the implementation of the proposed digital background calibration scheme with fixed-point precision. This implementation is compatible with an ADC with 14-bit as the number of digital output comprised of twelve 1.5-bit/stage structure and one 2-bit flash ADC as the 13th stage. The first six stages are calibrated only for the achievement of 12-bit resolution. Since only 7-bit accuracy is considered in the calibration signals, the proposed error estimation method with nonprecision calibration signals is applied to the

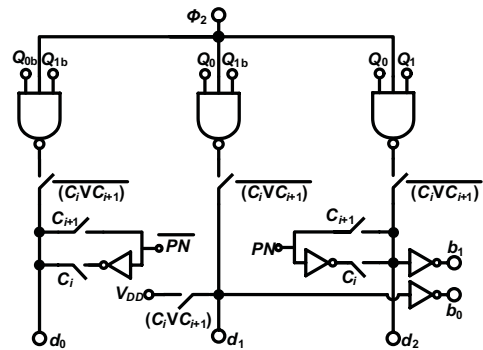


Fig. 11. Decoder used in the $(i + 1)$ th stage sub-ADC.

first four stages, and the other two stages utilize the ECS technique.

In Fig. 12, the precision of each signal is specified by two digits. The first digit is the number of bits required to define each signal without overload and the second one is the number of bits for fractional points. The difference of these two digits is used for the sign and integer parts of a signal. In this implementation of GS-PAP algorithm, $28L + 42N + 78$ bit memory is utilized. This figure also shows the maximum number of bits used at the output of GS algorithm. Although, in the middle frequencies, all the 22-bit will not be used, in frequencies near DC or Nyquist band, this number of bits is necessary. Because, in these cases, the approximation of the autocorrelation matrix needs more bits to suppress the overload in the calculation procedure. In Fig. 12, \underline{b} is defined as an N vector with only 1 in the first index and 0 in other indexes. Also, μ is the update step size of the GS-PAP algorithm.

Compared with the previous implemented or synthesized algorithms, the digital hardware cost comprising gate count and its overhead for power consumption could be approximately estimated in 90-nm digital CMOS technology. In this paper, the additional digital circuits are the 64-tap digital filter block for data prediction, the LMS machine to compute the error coefficients, and the blocks realizing third- and fifth-order functions. On the other hand, a 122-tap filter is implemented in [6] for nonlinear interpolation where the gate-level synthesis of the logic for the combiner block, the nonlinear interpolation filter, and the calibration engine indicates a complexity of 17-K, 2.3-K, and 53-K gates, respectively. Also, the reported power consumption of the combiner block, interpolation filter, and calibration engine are 7.3, 1.15, and 1.8 mW, respectively, at 200 MHz. It is worth mentioning that the nonlinear interpolation algorithm utilized in [6] uses approximately the same digital hardware as used in the proposed approach. But, the digital engine in [6] is not used in every cycle. To reduce the digital hardware in the proposed calibration technique, the LMS algorithm can also be used instead of the GS-PAP one, but, with an increased convergence time and hence a degraded performance.

VI. SIMULATION RESULTS

The proposed background calibration method is evaluated in the context of a 1.5-bit/stage pipelined ADC with

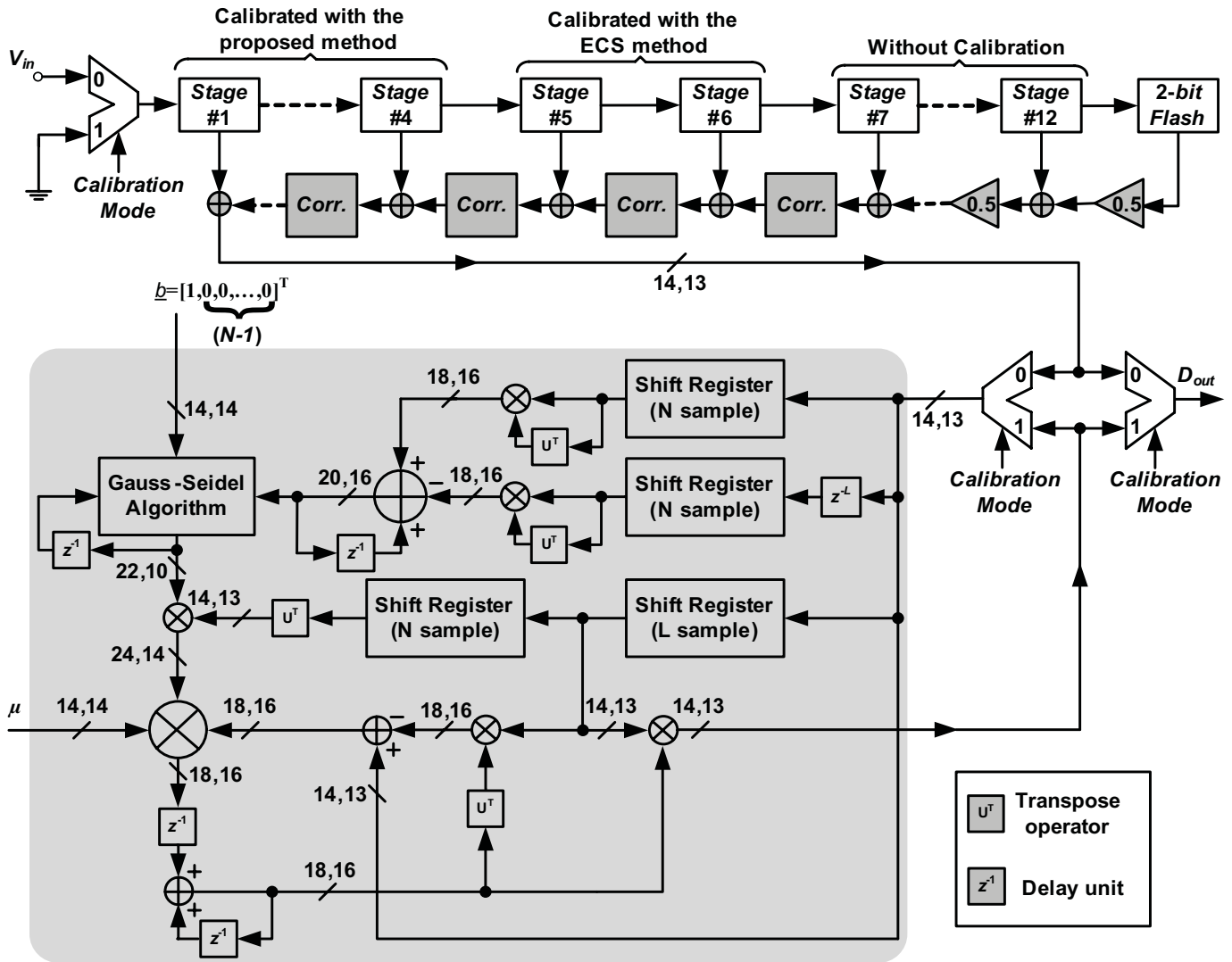


Fig. 12. Digital implementation of the predictor with fixed-point elements.

12-bit resolution. The ADC has been simulated in a standard 90-nm CMOS technology with 1.2-V power supply and 100-MS/s sampling rate. It has twelve 1.5-bit stages with a 2-bit back-end flash ADC. To have a view on the value of error parameters, they are obtained for ADC's first stage from the transistor-level simulations as $\alpha_1 = -0.04$, $\alpha_3 = -0.11$, and $\alpha_5 = -0.22$. In this paper, in order to further relax the required analog circuits' specifications and to better show the ability of the proposed calibration algorithm, the simulation results are reported by considering a fifth-order nonlinearity in the operational amplifiers. In practical implementations, the calibration can be also performed by considering a third-order nonlinearity and the proper design of amplifiers as well.

As mentioned before, the calibration algorithm is applied only to the first six stages. In fact, the proposed error estimation method with nonprecision calibration signals is applied to the first four stages, and the other two stages use the ECS algorithm. The calibration procedure is commenced from the sixth stage and goes back to the first stage. This is because the proposed calibration algorithm is performed by assuming an ideal back-end ADC in the calibration of the i th stage. The

accuracy of the calibration signals is limited to 7-bit where they can be easily implemented by the conventional resistive ladder. The analog circuits are simulated in HSPICE where the calibration process is implemented with MATLAB platform.

It is worth mentioning that the design example is intended for 12-bit resolution while the accuracy of the calibration signals is limited to 7-bit. By considering the fact that 1-bit lower resolution is needed in every later stage, so, in the fifth stage, 7-bit resolution is needed and this can be achieved with the ECS technique. Therefore, instead of the proposed technique, the ECS approach is employed in the fifth and sixth stages in order not to use the extra DAC which is used in the proposed calibration technique.

The output power spectral density (PSD) of the simulated ADC without calibration and with ECS calibration method is shown in Fig. 13(a) and (b), respectively. The simulated PSD using the proposed calibration algorithm is depicted in Fig. 14. The SNDR and SFDR are 40 and 42 dB, respectively, in noncalibrated ADC, and they are improved to 56 and 58 dB, respectively, by using the ECS calibration method in the first six stages. The SNDR and SFDR values are improved to 68

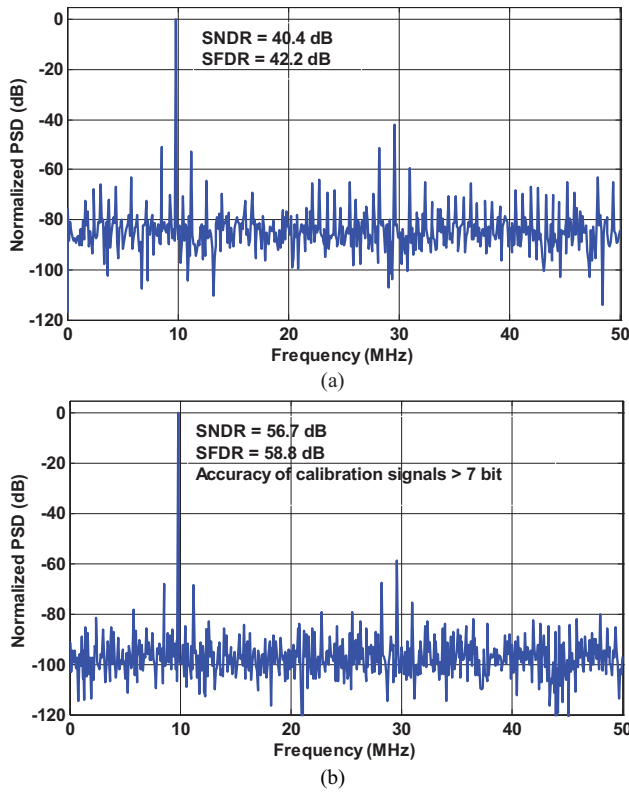


Fig. 13. PSD of ADC's digital output (a) before calibration and (b) with ECS calibration technique in the first six stages.

and 83 dB, respectively, by applying the proposed calibration method.

Figs. 15 and 16 plot the simulated DNL and INL before and after the calibration, respectively, at a sampling frequency of 100 MHz. The noncalibrated ADC has a maximum INL of ± 50 LSB, while after calibration, the maximum INL is ± 2.2 LSB. Also, the maximum DNL falls into $+0.9$ LSB after the calibration while before the calibration there are several missing codes.

The ADC performance in the Nyquist band is evaluated by plotting the SNDR and SFDR for several input signal frequencies in Figs. 17 and 18, respectively. As seen, by using the proposed calibration algorithm, the values of SNDR and SFDR are considerably improved in whole of the input signal frequency band compared with the noncalibrated or calibrated ADCs by using the ECS method. It is worth to mention that because the equalization-based algorithms estimate the error coefficients independent of the input signal, the values of both SNDR and SFDR decrease when the input signal frequency is increased.

Figs. 19 and 20 show the convergence behavior of the linear error coefficient (α_1) and error in ADC's first stage corrected by the ECS method and the proposed error estimation with nonprecision calibration signals algorithm, respectively. As seen, due to large errors in calibration signals, the convergence process in the ECS method has no proper situation, and the accuracy of estimation is limited to 7-bit. However, the proposed method has considerably better convergence behavior, and the accuracy of estimation is improved to 12 bits while the accuracy of calibration signals is only 7-bit. This means that

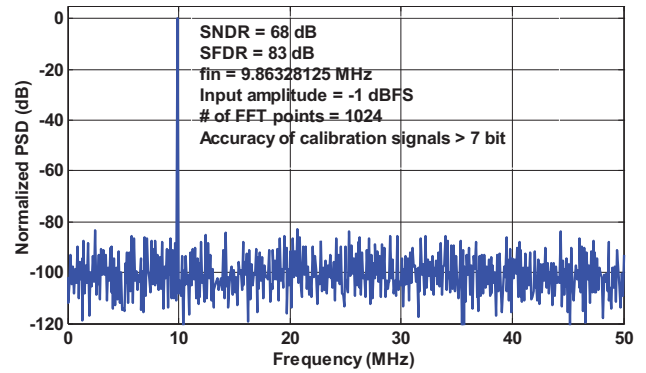


Fig. 14. PSD of ADC's digital output with the proposed calibration technique.

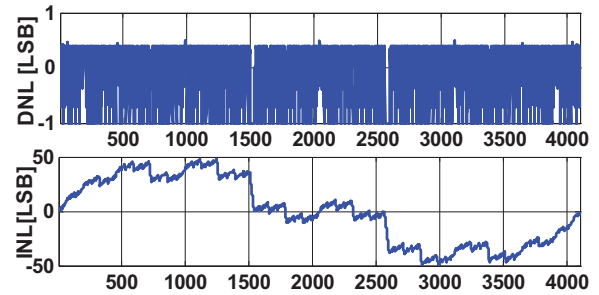


Fig. 15. Simulated INL and DNL before the calibration.

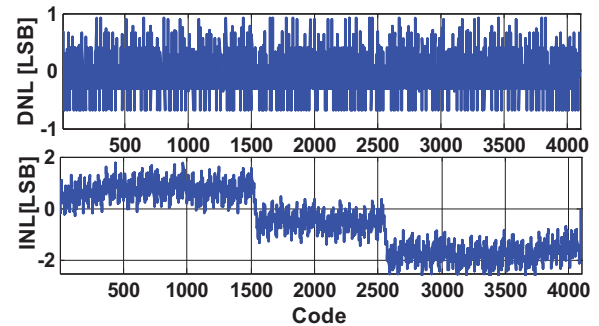


Fig. 16. Simulated INL and DNL after using the proposed calibration.

the accuracy of calibration in the ECS technique is limited by the calibration signals, while the proposed calibration method improves that beyond the accuracy of calibration signals.

For the calibration of each stage in the background structure, one frame with 2^{13} samples is defined where 2^{10} of them are only utilized for the estimation of the error coefficients, and the other frame samples are not skipped but are used in the normal conversion process. In fact, the foreground calibration process also need only upto 2^{10} samples (with $\mu_1 = 1/128$, $\mu_3 = 1/4096$, and $\mu_5 = 1/8192$). Hence, the total calibration time for background calibrated ADC or the start-up delay is equal to $491.52 \mu s$ with 100-MHz sampling rate. Also, it should be regarded that after the calibration of all stages, the calibration process is restarted from the sixth stage.

Beside the simulation results, a quantitative analysis is provided to estimate the convergence time for different types

TABLE I
PERFORMANCE COMPARISON OF THE SIMULATED ADC

Ref.	Process	Resolution	V_{DD} (V)	f_s (MS/s)	INL (LSB)	DNL (LSB)	SFDR (dB)	SNDR (dB)	SFDR Improvement (dB)	SNDR Improvement (dB)	Analog Power (mW)	Convergence Iterations (N_{ci})	FoM (pJ/conv. step)
This paper	90 nm	12-bit	1.2	100	2.2	0.9	83	68	41	28	48	6×2^{13}	0.23
[2]	90 nm	14-bit	1.2	100	3.6	0.54	88	69.9	42	27	93	3×2^{32}	0.37
[5]	0.25 μm	12-bit	2.5	80	+0.24	+0.09	84.5	72.6	32.2	22.5	340	—	1.22
[6]	90 nm	12-bit	1.2	200	+1.3	+0.59	—	62	—	32	348	2^{14}	1.25
[7]	90 nm	10-bit	1.2	500	1	0.4	—	56	—	27	55	14×2^{15}	0.31
[12]	0.35 μm	12-bit	3.3	20	0.75	0.42	80	70.2	12	7.9	191	2^{21}	3.61
[17]	90 nm	14-bit	1.2	100	1.3	0.9	90	73	—	—	250	2^{10}	0.68
[18]	0.35 μm	12-bit	3.3	20	0.2	0.27	84.4	72.5	31.9	31.2	56.3	5×2^{12}	0.78
[19]	0.18 μm	10-bit	1.8	100	0.95	0.48	70.4	56.2	—	—	31	—	0.76

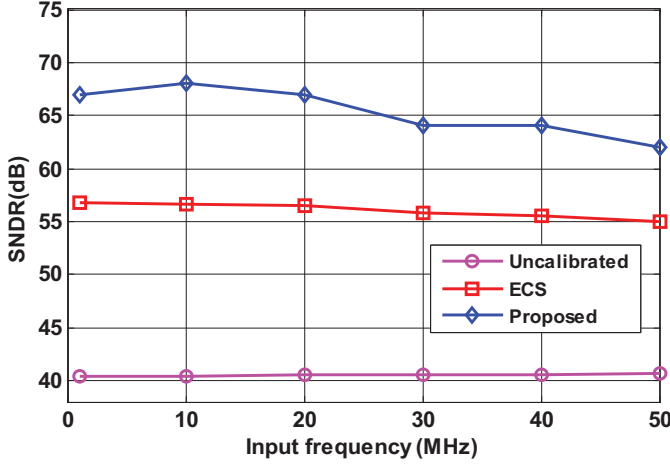


Fig. 17. SNDR versus input signal frequency.

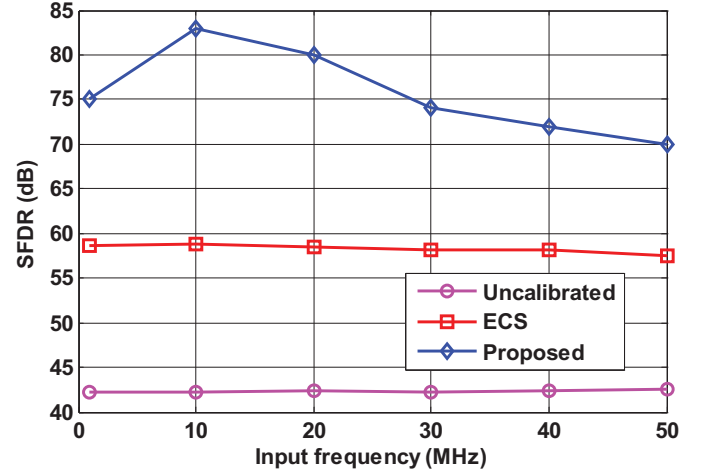


Fig. 18. SFDR versus input signal frequency.

of input signals. The predictor's optimal MSE is defined as

$$\varepsilon_L = \min \left(E \left\{ |e_p(n)|^2 \right\} \right) \quad (17)$$

where $e_p(n)$ is the prediction error at the n th sample. When the predictor input signal $D_{in}(n)$ is a wide-sense stationary process with a power spectrum density of $S_{DD}(e^{j\omega})$ and is nonzero for all ω , ε_L will be the mean square value of the error of an optimal L th-order predictor which satisfies the following relation [16]:

$$\varepsilon_L = \exp \left(\frac{1}{2\pi} \int_0^{2\pi} L n^{S_{DD}(e^{j\omega})} d\omega \right). \quad (18)$$

In deriving this relation, the prediction error was assumed to be white. This condition is well satisfied when the predictor length L is large enough. On the other hand, if the skipping rate is halved, the MSE is degraded around 3 dB. Hence, the convergence iterations (N_{ci}) of the total calibration process for an arbitrary input signal with the PSD of $S_{DD}(e^{j\omega})$ is obtained as

$$N_{ci} = \underbrace{6 \times 2^{10}}_{\text{foreground cal.}} \times \underbrace{2^{\left(\frac{\varepsilon_L - \varepsilon_{ideal}}{3}\right)}}_{\text{background cal.}} \quad (19)$$

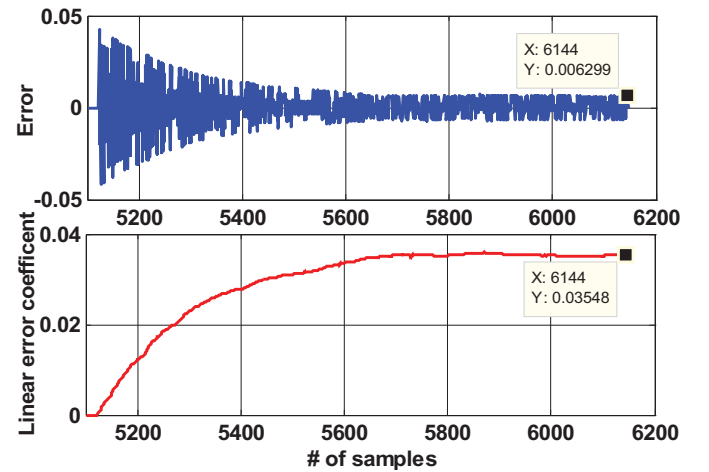


Fig. 19. Convergence of a_1 and error in first stage calibrated by ECS method.

where ε_{ideal} is the desired MSE for background calibrated ADC. For instance, ε_L is equal to -42 dB for the signal shown in Fig. 9. For an ε_{ideal} of -69 dB, the convergence time will be equal to 31.45728 ms with 100-MHz sampling rate.

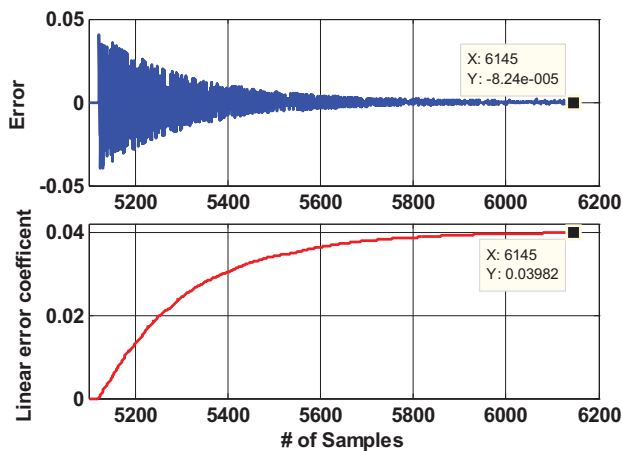


Fig. 20. Convergence of α_1 and error in first stage calibrated by the proposed method.

The simulated pipelined ADC is compared with several recently reported ADCs in Table I where the figure of merit (FoM) mentioned in [1] is also utilized for comparison. The designed ADC achieves the lowest FoM although this comparison is not completely fair since the simulation results reported here are compared with the measurement results. Nonetheless, it should be regarded that the designed circuits are only utilized to prove the efficiency of the proposed calibration method. To have a practical prototype, it will be power efficient to optimize both the analog circuits and the calibration algorithm complexity.

VII. CONCLUSION

In this paper, a digital background calibration technique for pipelined ADCs was proposed to measure and cancel the capacitor mismatch, residue gain error, and operational amplifier's nonlinearity. The main achievement of this technique is the error correction independent of the accuracy of calibration signals. Moreover, a new method was proposed to isolate the calibration process from the ADC's normal operation without limiting the ADC input signal bandwidth and adding any extra latency. The proposed methods were applied to a 1.5-bit/stage 12-bit pipelined ADC designed in a standard 90-nm CMOS technology with 1.2-V power supply and 100-MS/s sampling rate. By using these techniques, both the ADC's SNDR and SFDR were significantly improved when verifying the usefulness of the proposed calibration technique.

REFERENCES

- [1] A. Panigada and I. Galton, "Digital background correction of harmonic distortion in pipelined ADCs," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 53, no. 9, pp. 1885–1895, Sep. 2006.
- [2] A. Panigada and I. Galton, "A 130 mW 100 MS/s pipelined ADC with 69 dB SNDR enabled by digital harmonic distortion correction," *IEEE J. Solid-State Circuits*, vol. 44, no. 12, pp. 3314–3328, Dec. 2009.
- [3] J. Li and U. Moon, "Background calibration techniques for multi-stage pipelined ADCs with digital redundancy," *IEEE Trans. Circuits Syst. II, Reg. Papers*, vol. 50, no. 9, pp. 531–538, Sep. 2003.
- [4] B. Murmann and B. E. Boser, "Digital domain measurement and cancellation of residue amplifier nonlinearity in pipelined ADCs," *IEEE Trans. Instrum. Meas.*, vol. 56, no. 6, pp. 2504–2514, Dec. 2007.
- [5] C. R. Grace, P. J. Hurst, and S. H. Lewis, "A 12-bit 80-MSample/s pipelined ADC with bootstrapped digital calibration," *IEEE J. Solid-State Circuits*, vol. 40, no. 5, pp. 1038–1046, May 2005.

- [6] B. D. Sahoo and B. Razavi, "A 12-bit 200-MHz CMOS ADC," *IEEE J. Solid-State Circuits*, vol. 44, no. 9, pp. 2366–2380, Sep. 2009.
- [7] A. Verma and B. Razavi, "A 10-bit 500-MS/s 55-mW CMOS ADC," *IEEE J. Solid-State Circuits*, vol. 44, no. 11, pp. 3039–3050, Nov. 2009.
- [8] S. S. Haykin, *Adaptive Filter Theory*, 3rd ed. Upper Saddle River, NJ, USA: Prentice-Hall, 1996.
- [9] U. Moon and B. Song, "Background digital calibration techniques for pipelined ADCs," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 44, no. 2, pp. 102–109, Feb. 1997.
- [10] R. G. Massolini, G. Cesura, and R. Castello, "A fully digital fast convergence algorithm for nonlinearity correction in multistage ADC," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 53, no. 5, pp. 389–393, May 2006.
- [11] D. Y. Chang, "Design Techniques for a Pipelined ADC Without Using a front-end sample-and-hold amplifier," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 51, no. 11, pp. 2123–2132, Apr. 2004.
- [12] H. Wang, X. Wang, P. J. Hurst, and S. H. Lewis, "Nested digital background calibration of a 12-bit pipelined ADC without an input SHA," *IEEE J. Solid-State Circuits*, vol. 44, no. 10, pp. 2780–2789, Oct. 2009.
- [13] O. Erdogan, P. Hurst, and S. Lewis, "A 12-b digital-background-calibrated algorithmic ADC With-90-dB THD," *IEEE J. Solid-State Circuits*, vol. 34, no. 12, pp. 1812–1820, Dec. 1999.
- [14] L. Sumanen, M. Waltari, V. Hakkarainen, and K. Halonen, "CMOS dynamic comparators for pipeline A/D converters," in *Proc. Int. Symp. Circuits Syst.*, vol. 5, May 2002, pp. 157–160.
- [15] H. Sheikhzadeh, K. R. L. Whyte, and R. L. Brennan, "Partial update subband implementation of complex pseudo-affine projection algorithm on oversampled filterbanks," in *Proc. IEEE Int. Conf. Acoust. Speech Signal Process.*, vol. 4, Jan. 2005, pp. 373–376.
- [16] P. P. Vaidyanathan, *The Theory of Linear Prediction*, San Mateo, CA, USA: Morgan & Claypool, 2008.
- [17] H. Van de Vel, B. A. J. Buter, H. van der Ploeg, M. Vertregt, G. J. G. M. Geelen, and E. J. F. Paulus, "A 1.2–V 250-mW 14-b 100-MS/s digitally calibrated pipeline ADC in 90-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 44, no. 4, pp. 1047–1056, Apr. 2009.
- [18] J. Yuan, S. W. Fung, K. Y. Chan, and R. Xu, "A 12-bit 20 MS/s 56.3 mW pipelined ADC with interpolation-based nonlinear calibration," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 59, no. 3, pp. 555–565, Mar. 2012.
- [19] M.-Y. Kim, J. Kim, T. Lee, and C. Kim, "10-bit 100-MS/s pipelined ADC using input-swapped opamp sharing and self-calibrated V/I converter," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 19, no. 8, pp. 1438–1447, Aug. 2011.



Behzad Zeinali received the B.Sc. and M.Sc. degrees in electrical engineering from the Amirkabir University of Technology, Tehran, Iran, in 2009 and 2012, respectively.

He has been a Research Assistant with the IC Laboratory, Amirkabir University of Technology, since 2008, where he worked on the digital calibration of pipelined ADCs and design of CMOS tunable filters. His current research interests include mixed-signal integrated circuits and systems, including data converters and digital calibration techniques.



Tohid Moosazadeh received the B.Sc. and M.Sc. degrees in electrical engineering from Urmia University, Urmia, Iran, and Amirkabir University of Technology, Tehran, Iran, in 2007 and 2010, respectively, where he is currently pursuing the Ph.D. degree with the Department of Electrical Engineering.

His current research interests include analog and mixed-signal circuits and systems, digital calibration of pipelined ADCs, and opamp-less pipelined ADCs.



Mohammad Yavari (S'01–M'08) received the B.Sc., M.Sc., and Ph.D. degrees in electrical engineering from the University of Tehran, Tehran, Iran, in 1999, 2001, and 2006, respectively.

He has been an Assistant Professor with the Department of Electrical Engineering, Amirkabir University of Technology, Tehran, since 2006, where he founded the Integrated Circuits Design Laboratory, in 2007. He spent several research periods with the Institute of Microelectronics of Seville (IMSE-CNM), Seville, Spain. He was with Niktek, from May 2004 to April 2005 and October 2006 to May 2007, as a Principal Design Engineer, where he was involved in the design of high-resolution A/D and D/A converters for professional digital audio applications. He is the author or co-author of more than 100 peer-reviewed papers in international and national journals and conference proceedings on analog integrated circuits. His current research interests include analog and mixed-signal integrated circuits and signal processing, data converters, and CMOS RFIC design for wireless communications.

Dr. Yavari was a recipient of the Best Student Research Award of the University of Tehran in 2004.



Ángel Rodríguez-Vázquez (F'96) received the Ph.D. degree in physics-electronics from the University of Seville, Seville, Spain, in 1983.

He is a Full Professor of electronics with the University of Seville and a Researcher with the Institute of Microelectronics of Seville/CNM-CSIC (IMSE-CNM/CSIC), Seville. He is the President and the responsible for long term R&D of Innovaciones Microelectrónicas S.L. (AnaFocus). He has been looking for the balance between long term research and innovative industrial developments. He started a research unit on High-Performance Analog and Mixed-Signal VLSI Circuits of the Institute of Microelectronics of Seville/CNM-CSIC, Seville. He headed this unit until 2004, for more than 15 years, in the course of which he educated three generations of Ph.D.'s who are currently working at academia and at industry. He conducted pioneering R&D activities on bioinspired

microelectronics, including vision chips and neuro-fuzzy interpolators and controllers. He was a pioneer in the application of chaotic dynamics to instrumentation and communications, and his team completed the design and prototyping of the first, world-wide, integrated circuits with controllable chaotic behavior and the design and prototyping of the first world-wide chaos-based communication MoDem chips. His team made significant contributions to the area of structured analog and mixed signal design and the area of data converter design, including the elaboration of advanced teaching materials on this topic for different industrial courses and the production of two widely quoted books on the design of high performance CMOS sigma-delta converters. An estimated 30 high-performance mixed-signal chips were successfully designed by his research unit at IMSECNM/ CSIC until 2001 in the framework of different R&D programs and contracts. These include three generations of vision chips for high-speed applications, analog front-ends for XDSL MoDems, ADCs for wireless communications, ADCs for automotive sensors, chaotic signals generators, complete MoDems for power-line communications, etc. Many of these chips were state-of-the-art in their respective fields. Some of them have entered mass production. He founded Innovaciones Microelectrónicas S.L. (AnaFocus) in 2001. This company started operation after raising venture capital in January 2004. He served as the AnaFocus CEO until June 2009, a period in which the company grew from two employees until 50 employees and reached the threshold of maturity as a worldwide company specialized in the design and production of smart CMOS imagers and vision systems-on-chip. Since June 2009, he has been back to conduce long term research activities in the areas of vision systems using 3-D integration technologies and medical electronics. He has authored and edited over ten books, 46 chapters in contributed books, including original tutorials on chaotic integrated circuits, design of data converters and design of chips for vision, and 450 articles in peer-review specialized publications. He has presented many invited plenary lectures at different international conferences. His research work over 4900 citations and he has a h-index of 37 according to Google Scholar.

Dr. Rodríguez-Vázquez was a recipient of a number of international awards for his research work, including the IEEE Guillemin-Cauer Best Paper Award, the IEEE ECCTD Best Paper Award, and the IEEE ISCAS Best Demo-Paper Award, and was elected a fellow of the IEEE for his contributions to the design of chaos-based communication chips and neurofuzzy chips. He served as an Editor, an Associate Editor, and a Guest Editor for different IEEE and non-IEEE journals. He is in the committee of many international journals and conferences and has chaired different international IEEE and SPIE conferences.