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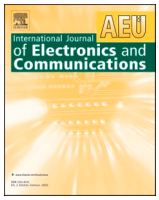

Regular paper

An improved PVT-Robust floating inverter dynamic amplifier for noise-shaping SAR ADCs

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ABSTRACT

The floating inverter dynamic amplifier (FIDA) is a power-efficient, open-loop, and dynamic amplifier without requiring any output common-mode feedback (CMFB) circuit. It is appropriate for low-power applications. However, its gain is not robust over process, voltage, and temperature (PVT) variations. In this work, a simple, low power, and low noise method is proposed to solve this problem. The proposed method controls the amplification time window of the FIDA to be proportional to its time constant. Based on the FIDA gain formula, this technique stabilizes the gain over PVT changes. The proposed PVT-robust FIDA is designed at the circuit level using 0.18 μm TSMC CMOS technology with Cadence Virtuoso tool. According to the post-layout simulation results of a sample design, the gain of the amplifier is 29.4 with 51.3 μW power consumption from a 1.2 V supply voltage. The maximum gain variation over PVT changes is reduced from 49.6% to 9.8% using the proposed gain calibration technique.

1. Introduction

Dynamic amplifiers (DAMPs) are one of the key components in recent noise-shaping (NS) successive approximation register (SAR) analog-to-digital converters (ADCs). The DAMPs are used in the NS loop filters to amplify the residue voltage and compensate for residue attenuation [1–3]. The NS-SAR ADCs are power-efficient for high-resolution applications when low-power, low-noise, and process, voltage, and temperature (PVT) robust DAMPs are utilized instead of conventional static amplifiers. However, the input voltages of the required DAMPs are small, and hence, their linearity is not critical in NS-SAR ADCs.

The DAMPs are utilized in both closed-loop and open-loop forms. The closed-loop DAMPs are PVT robust. However, they are power consuming and have large input-referred noise [4–8]. Therefore, they are not suitable for low-power applications. The open-loop DAMPs are low-power and low-noise structures. But, their gain is sensitive to the PVT variations [9–18]. So, they can be utilized in low-power applications provided that a gain calibration scheme is employed.

The conventional dynamic amplifier for NS-SAR ADCs has been presented in [9]. It is a power-efficient structure. However, it encounters a strict trade-off between gain and speed of the operation. Moreover, its gain depends on PVT conditions, and hence, it needs a gain calibration scheme. Also, it requires an output common-mode voltage detector to maintain its output common-mode voltages almost constant. In [10], an open-loop dynamic amplifier based on two cascaded integrators has been proposed, which is low power and low noise. However, it needs an output common-mode detector. Furthermore, its gain is sensitive to PVT variations. In [11], a charge-steering amplifier comprised of two clocked differential pairs has been proposed. It is low power, but its gain is low and also sensitive to PVT variations. In [12], a complementary charge-steering amplifier is suggested with a high gain as squared of [11]. Nevertheless, its gain is PVT variant. In [13,14], a PVT stabilized DAMP is presented by employing an additional circuit to control the clock of the conventional DAMP. However, it needs an output CMFB circuit and has a low gain. An open-loop dynamic ring amplifier using cascaded inverters is proposed in [15]. It is a power-efficient and high-speed structure. However, its design considerations are complicated to be stable. In [16], a two-stage clocked amplifier is reported to balance the trade-off between speed and gain. It includes of a differential pair with an active current-mirror load as the first stage and a common-source amplifier as the second stage to realize a Gm-R amplifier. Its gain is sensitive to PVT variations and devices mismatch. So, it needs the gain calibration and offset cancelation circuits to control the gain. In [17,18],

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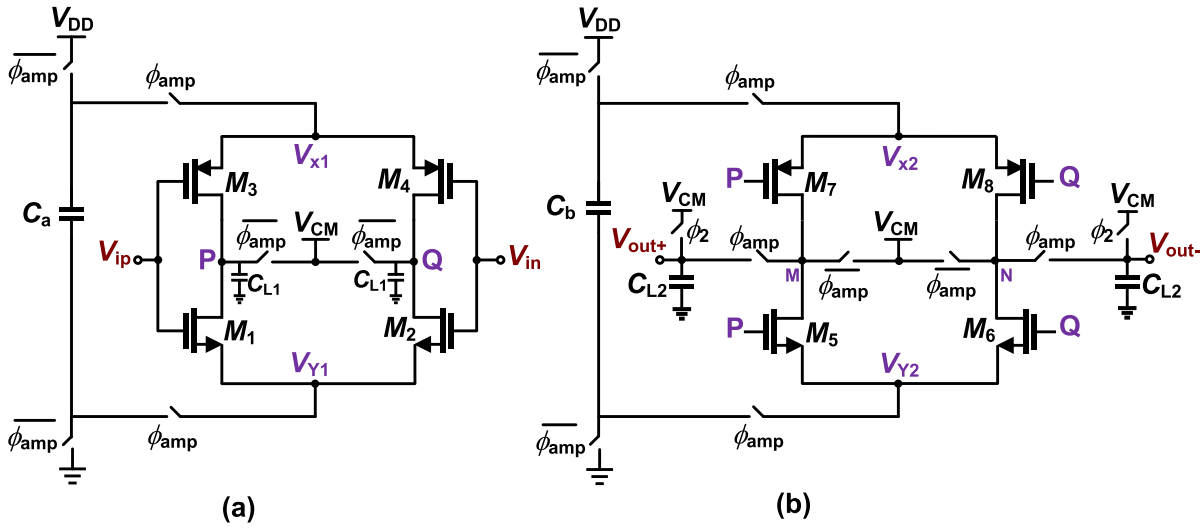


Fig. 1. The two-stage FIDA schematic, (a) first stage and (b) second stage.

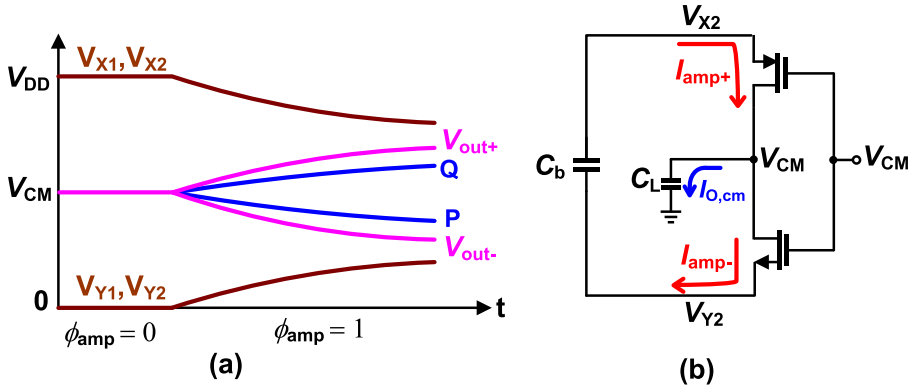


Fig. 2. (a) Operation of the FIDA, and (b) common-mode equivalent circuit of the output stage of the FIDA.

the temperature compensation techniques are used to stabilize the gain over the temperature changes. However, the effects of the voltage and process variations on the gain have been remained unchanged. In [19], an inverter based DAMP with a linearization technique is reported which is suitable for high speed pipeline ADCs. Since its gain is PVT variant, it uses a foreground calibration scheme for ADC to resolve the gain error issue.

In [20–24], the floating inverter dynamic amplifier (FIDA) is used by utilizing dynamic bias and current reuse schemes to improve the gain and reduce the noise. It has a wide input common-mode range without needing any CMFB circuit against many other published DAMPs. Nonetheless, its gain is sensitive to the PVT variations. In [25], a dynamic amplifier is proposed with a cascode input transistor pairs, which are set in linear region to increase the input and output voltage swings of the amplifier. Also, it uses an automatic calibration scheme including of clamping the drain voltage of input transistors to a reference voltage to have a PVT robust gain. In [26], the FIDA has been used as a residue amplifier in a NS-SAR ADC with limited amplification time window. Actually, it uses manual tuning of the reservoir capacitors to get PVT robust FIDA gain. However, this method requires one step manual capacitors tuning before starting the amplification phase.

This paper proposes a novel technique to stabilize the FIDA gain against PVT variations. We propose a circuit to adjust the amplification time window of the FIDA to control the gain in PVT changes. An auxiliary FIDA is used as a reference amplifier to control the gain of the main FIDA. A constant input voltage is applied to the auxiliary FIDA to achieve nearly constant output voltage. By comparing the output voltage of the auxiliary FIDA with a constant reference voltage, its gain is also controlled. After that, the amplification time window of the main FIDA is considered to be the same as the auxiliary one. So, according to the gain formula, the FIDA gain is kept nearly constant over PVT variations. This technique does not need any additional tuning reservoir capacitors as opposed to [27]. Also, this technique is low-power without requiring any manual user adjustment.

The rest of the paper is arranged as follows. In Section 2, the structure of the proposed PVT-robust FIDA is presented. In Section 3, the circuit-level post-layout simulation results of the proposed dynamic amplifier are reported. Finally, Section 4 concludes the paper.

2. Proposed PVT-Robust floating inverter dynamic amplifier structure

2.1. The floating inverter dynamic amplifier

Fig. 1 shows a two-stage floating inverter dynamic amplifier circuit to achieve high gain for NS-SAR ADCs like [3,16,26]. From Fig. 1, every stage comprises of an inverter pair, a storage capacitor, and some switches which are controlled by the amplification clock of ϕ_{amp}. When $\phi_{amp} = 0$, the amplifier turns off and the circuit is in reset mode. In this mode, the C_a and C_b storage capacitors are charged to V_{DD}. Also, voltage nodes of P, Q, M, and N are reset to the common-mode voltage of V_{CM}. However, when $\phi_{amp} = 1$, the amplifier turns on and enters into the amplification mode. In this mode, the nodes of P, Q, M, and N are disconnected from V_{CM}. The C_a and C_b storage capacitors are utilized as

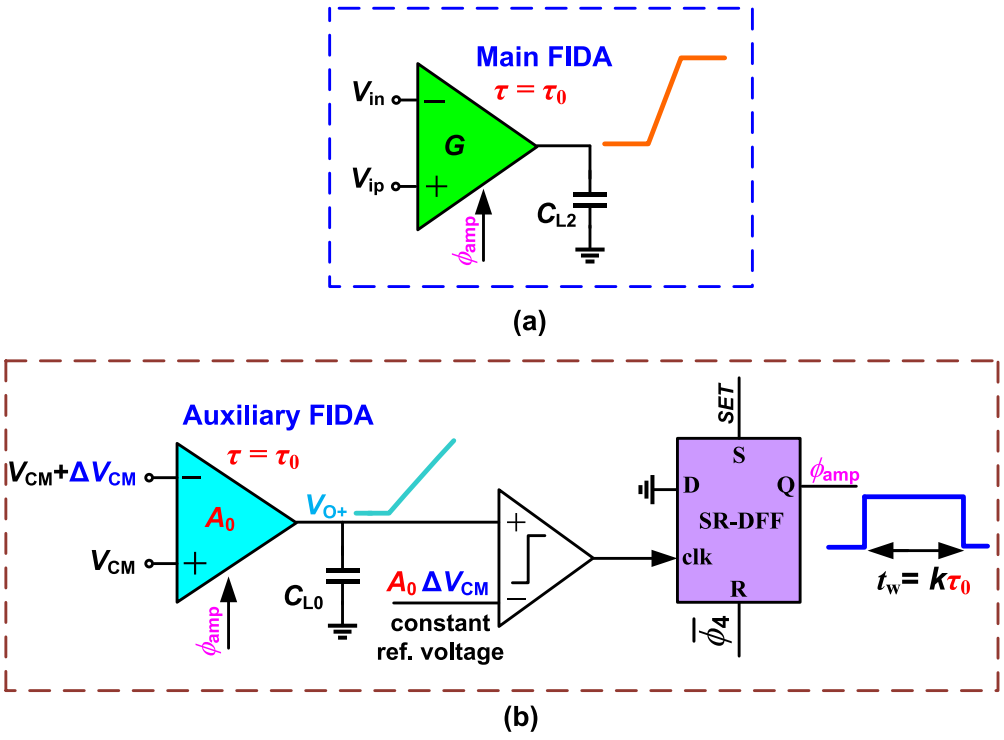


Fig. 3. Overall structure of the (a) main FIDA, and (b) proposed amplification time control circuit.

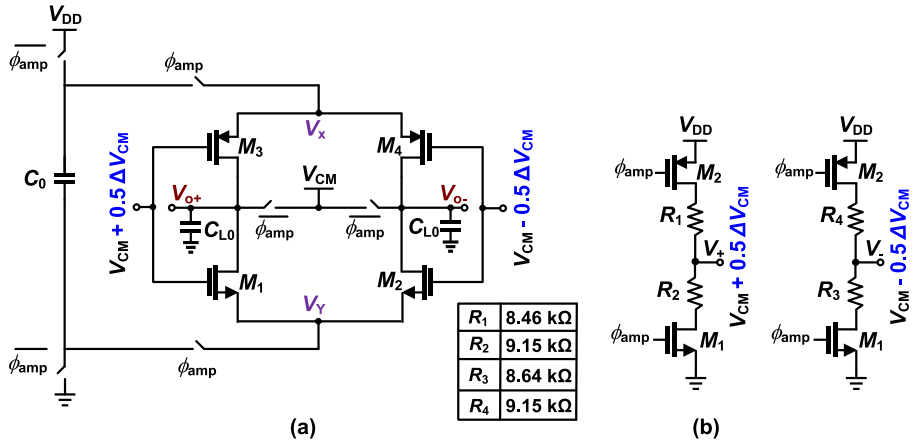


Fig. 4. (a) The auxiliary FIDA schematic and (b) dynamic resistor divider bias circuit.

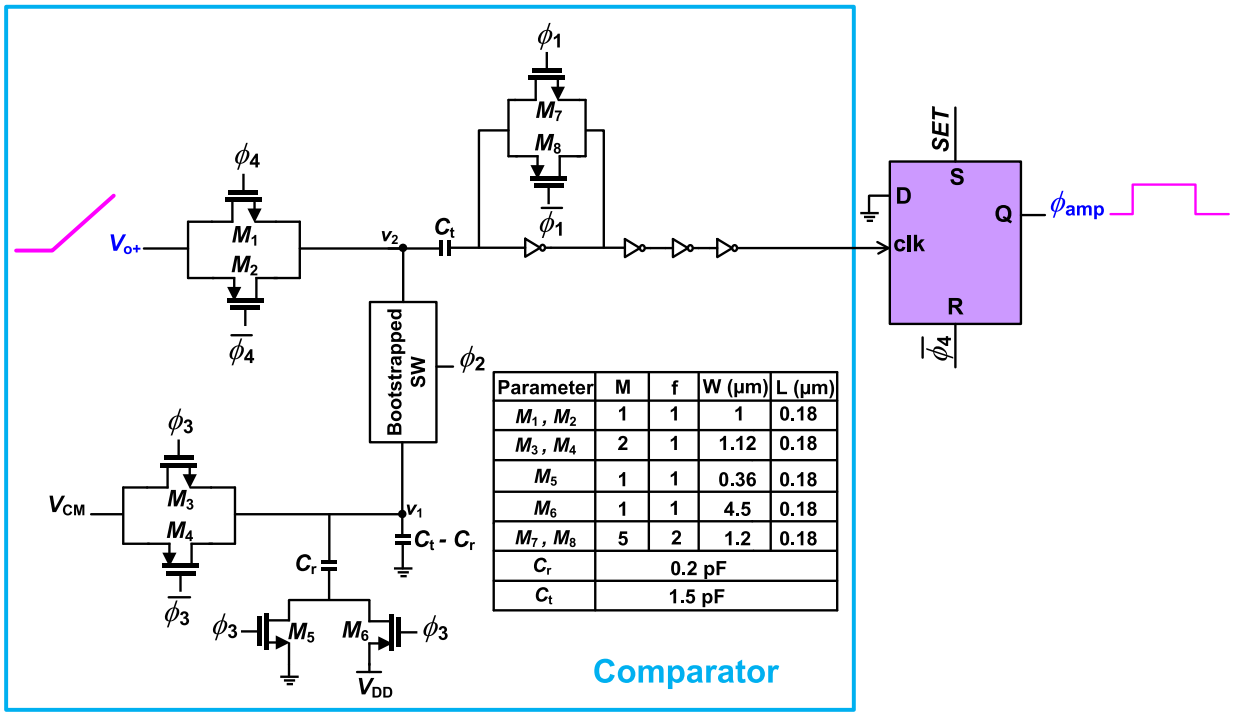
the power supply in the inverter pairs resulting in discharging C_a and C_b capacitors as shown in Fig. 2(a) [20,21].

As mentioned in Section 1, the FIDA has attractive features like low power consumption, wide input common-mode voltage range, and intrinsically constant output common-mode voltage without needing any CMFB circuit. These properties have made the FIDA the as a right choice for NS-SAR ADC applications in recent years. The common-mode equivalent circuit of the output stage of the FIDA is shown in Fig. 2(b). As depicted in Fig. 2(b), the constant output common-mode voltage of the FIDA is obtained due to the equal input and output currents of the storage capacitor ($I_{amp+} = I_{amp-}$). So, it results in zero common-mode current passing through the load capacitor ($I_{O,cm} = 0$) [6]. The inverter based amplifiers without the floating capacitor require a CMFB circuit as in [27].

However, the FIDA gain is sensitive to the PVT variations, and hence, its gain is not robust in PVT conditions. As mentioned in Section 1, recently, some researchers have tried to solve this issue by using FIDA in the closed-loop form [6,7,8] or in an open-loop form with a long amplification time window [22]. Also, in our recent work, we used the manual tuning of the storage capacitors to make the open-loop FIDA gain relaxed to PVT variations [26]. However, these solutions have some problems such as large input-referred noise, low speed [22], or they are not user friendly [26]. So, in this work, a new technique is proposed to make a PVT-robust FIDA without the problems of the previously reported solutions.

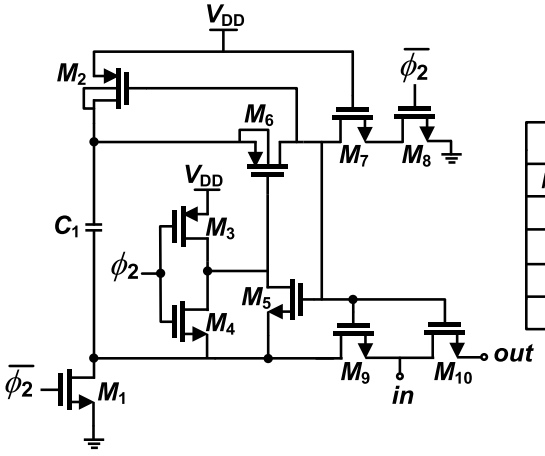
2.2. Overall structure of the proposed PVT-Robust FIDA

In this sub-section, the idea of the proposed gain calibration method is firstly explained. Then, the operation of the proposed FIDA structure will be described. In Fig. 1, at the beginning of the amplification phase, the M_1-M_8 transistors of the FIDA work at the proximity of the weak-



Parameter	M	f	W (μm)	L (μm)
M_1, M_2	1	1	1	0.18
M_3, M_4	2	1	1.12	0.18
M_5	1	1	0.36	0.18
M_6	1	1	4.5	0.18
M_7, M_8	5	2	1.2	0.18
C_r	0.2 pF			
C_t	1.5 pF			

Fig. 5. Schematic of the comparator and following SR-D-FF.



Parameter	M	f	W (μm)	L (μm)
M_1, M_4, $M_{7\text{-}9}$	1	1	0.22	0.18
M_2, M_3	1	1	0.54	0.18
M_6	1	1	0.36	0.18
M_{10}	2	1	1.5	0.18
C_1	0.2 pF			

Fig. 6. Schematic of the bootstrapping switch [28].

inversion region. As the absolute value of their gate-source voltage decreases along the amplification phase, they further go into the deep subthreshold region. For simplicity, we assume that the FIDA input transistors are always in the weak-inversion region when they are on [20]. Therefore, the gain of the two-stage FIDA in Fig. 1 is given by [22]:

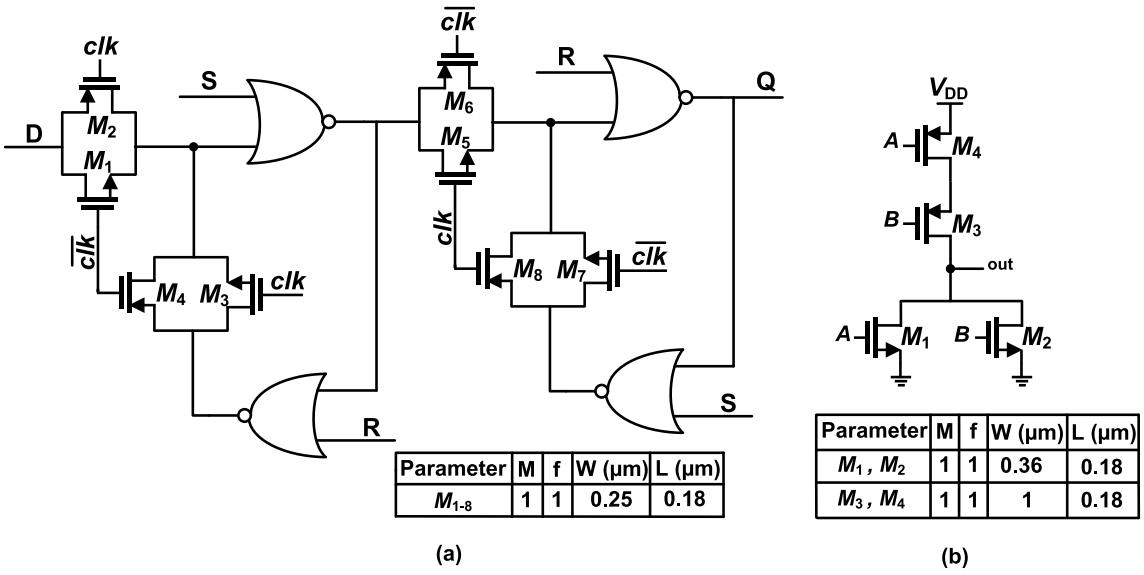
$$G(t_w) \approx \frac{\alpha_1 C_a}{C_{L1}} \ln\left(1+\frac{t_w}{\tau_1}\right).\frac{\alpha_2 C_b}{C_{L2}} \ln\left(1+\frac{t_w}{\tau_2}\right) \tag{1}$$

where t_w, C_a and C_b are the amplification time window and storage capacitors, respectively. Also, C_{L1} and C_{L2} are the load capacitors of the FIDA stages. $\alpha_{1,2}$ are fitting constants and $\tau_{1,2}$ are the initial discharge time constants of two stages of the FIDA in the amplification phase. $\tau_{1,2}$ are given by

$$\tau_1 = \frac{2n\,.\,U_T\,.\,C_a}{I_{amp1}(0^+)} \qquad \tau_2 = \frac{2n\,.\,U_T\,.\,C_b}{I_{amp2}(0^+)} \tag{2}$$

where U_T, n, and $I_{amp1,2}$ (0^+) are the thermal voltage, weak-inversion slope factor, and initial current of the FIDA stages, respectively [22]. From (1), the fitting factor and the capacitor ratio parts are almost PVT robust. However, the initial time constants of two stages, $\tau_{1,2}$, are not stable in PVT conditions. Therefore, it is clear that if we choose a fixed amplification time window, t_w, then, the only sources of the FIDA gain instability will be $\tau_{1,2}$. However, instead of a constant amplification time window, t_w, we assume t_w proportional to τ_i as

$$\frac{t_w}{\tau_{1,2}} = k_{1,2} \quad \Rightarrow \quad t_w = k_{1,2}.\,\tau_{1,2} \tag{3}$$



Parameter	M	f	W (μm)	L (μm)
$M_{1\text{-}8}$	1	1	0.25	0.18

Parameter	M	f	W (μm)	L (μm)
M_1, M_2	1	1	0.36	0.18
M_3, M_4	1	1	1	0.18

Fig. 7. Schematic of the (a) SR-D-FF [29], and (b) NOR gates.

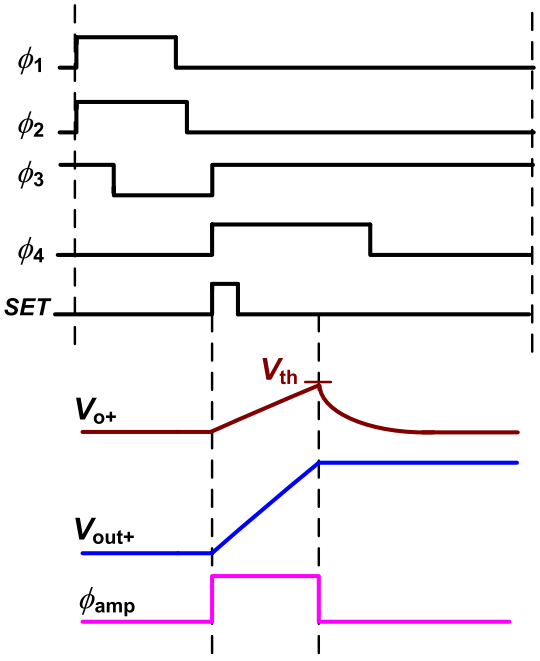


Fig. 8. Timing diagram of the comparator and SR-D-FF.

where $k_{1,2}$ are constant factors over PVT variations to achieve a PVT robust gain. Therefore, we design a clock control circuit to adjust the amplification clock.

The overall structure of the proposed circuit is illustrated in Fig. 3. Fig. 3(a) shows the main FIDA block. As depicted in Fig. 3(b), we use a single-stage FIDA as an auxiliary one with an initial time constant of τ_0 and a small gain of A_0. Its input differential voltage is assumed to be a constant voltage of ΔV_{CM} and its input common-mode voltage is V_{CM}. Therefore, its output differential voltage is constant about A_0xΔV_{CM}. However, to achieve a PVT robust gain of A_0 for the auxiliary FIDA, we compare its output with a constant threshold voltage of A_0xΔV_{CM}. So, when its output crosses the A_0xΔV_{CM} value, the comparator output will be "High" and trigs the Set-Reset D-Flip Flop (SR-D-FF) clock. Then, the output of the SR-D-FF drops which results in $\phi_{amp} = 0$. Since ϕ_{amp} is the clock of the auxiliary FIDA, it is turned off. So, in this circuit, the amplification time window of the auxiliary FIDA is automatically controlled over PVT conditions to keep its gain constant equal to A_0. The amplification time window of the auxiliary FIDA is calculated as.

$$\begin{cases} t_{aux} = \left[\exp\left(\frac{A_0 C_{L0}}{\alpha_0 C_0}\right) - 1\right] . \tau_0 \\ if \ \left[\exp\left(\frac{A_0 C_{L0}}{\alpha_0 C_0}\right) - 1\right] = k_0 \end{cases} \Rightarrow t_{aux} = k_0 . \tau_0 \quad (4)$$

The auxiliary amplification time window (t_{aux}) is proportional to its initial time constant (τ_0). As mentioned above, we assume the same amplification time window for both auxiliary and main FIDAs. So, from the relations (3) and (4), we have.

$$k_{1,2} . \tau_{1,2} = k_0 . \tau_0 \Rightarrow \tau_{1,2} = \frac{k_0}{k_{1,2}} . \tau_0 \quad (5)$$

For design simplicity, we choose the constant coefficient of $k_0/k_{1,2} = 1$ resulting in $\tau_{1,2} = \tau_0$. Therefore, we design the main two-stage FIDA to have the same initial time constant as the auxiliary FIDA in both stages ($\tau_1 = \tau_2 = \tau_0$). So, from the relation (2), we have.

$$\frac{C_a}{I_{amp1}(0^+)} = \frac{C_b}{I_{amp2}(0^+)} = \frac{C_0}{I_{amp0}(0^+)} \quad (6)$$

Furthermore, from the relations (1) and (4), the main FIDA gain relation can be calculated as.

$$G(t_w) = \frac{\alpha^2 C_a C_b}{C_{L1} C_{L2}} \left[\ln\left(1 + \frac{t_w}{\tau_0}\right)\right]^2 = \frac{\alpha^2 C_a C_b}{C_{L1} C_{L2}} \left[\ln\left(1 + \left[\exp\left(\frac{A_0 C_{L0}}{\alpha_0 C_0}\right) - 1\right]\right)\right]^2 \quad (7)$$

As mentioned before, α and A_0 are robust over PVT changes. Also, the capacitor ratios are stable over PVT conditions. So, the overall gain relation in (7) is also PVT robust.

From the relation (6), to implement this condition, there are different options for C_a, C_b, and C_0 capacitors value and initial currents. However, in this work, for design convenience, we choose the same capacitances and initial currents for the main and auxiliary FIDAs as below.

$$\begin{cases} C_a = C_b = C_0 \\ I_{amp1}(0^+) = I_{amp2}(0^+) = I_{amp0}(0^+) \end{cases} \quad (8)$$

Therefore, we consider the transistors size of the two stages of the

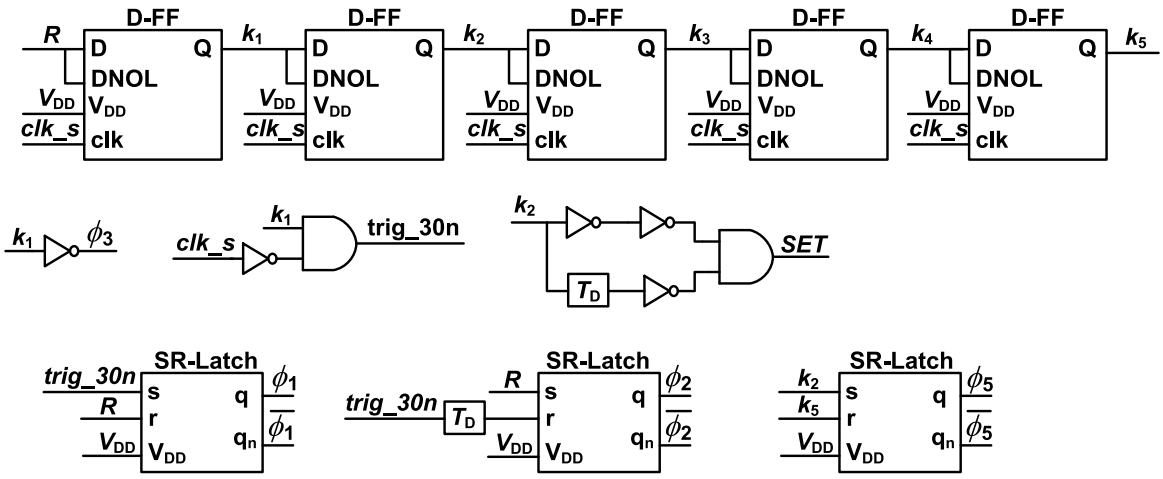
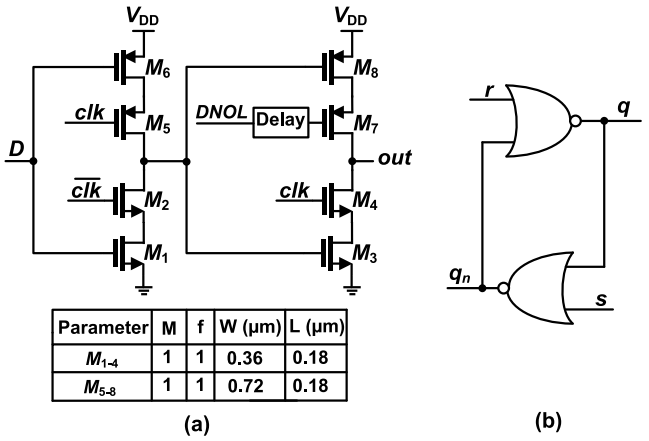


Fig. 9. Schematic of the clock generator.



Parameter	M	f	W (μm)	L (μm)
$M_{1\text{-}4}$	1	1	0.36	0.18
$M_{5\text{-}8}$	1	1	0.72	0.18

Fig. 10. Schematic of the (a) D-FF [31], and (b) SR-Latch.

main FIDA the same as the corresponding transistors of the auxiliary FIDA. Also, the storage capacitors of both FIDAs will be chosen the same. Then, we achieve equal initial currents resulting in equal initial time constants in both amplifiers. So, from the relations (7), and (8), the main FIDA gain is obtained as.

$$G(t_w) = \frac{\alpha^2 C_0^2}{C_{L1}C_{L2}}\left[\ln\left(1+\frac{t_w}{\tau_0}\right)\right]^2 = \frac{\alpha^2 C_0^2}{C_{L1}C_{L2}}\left[\ln\left(1+\left[\exp\left(\frac{A_0 C_{L0}}{\alpha_0 C_0}\right)-1\right]\right)\right]^2 \quad (9)$$

From the relation (9), by keeping A_0 constant over PVT variations, the main FIDA gain (G) will be also nearly constant because all other parameters and parameter ratios in (9) are stable in PVT conditions.

2.3. The proposed PVT-Robust FIDA circuit

The main FIDA schematic is depicted in Fig. 1. As mentioned above, in this work, we use a two-stage FIDA to achieve a gain about 30 as a sample design for applications like NS-SAR ADCs [1,16,26]. As shown in Fig. 4(a), the auxiliary FIDA is considered with a small gain around 4.7. So, a single-stage FIDA [20,21] is selected to realize it. Fig. 4(b) shows the resistor divider bias circuit and its resistance values to create the constant positive and negative input voltages of the auxiliary FIDA. It is a dynamic bias circuit and only turns on at the amplification phase (ϕ_{amp}) to be power efficient. The constant positive and negative output voltages of the resistor dividers are given by.

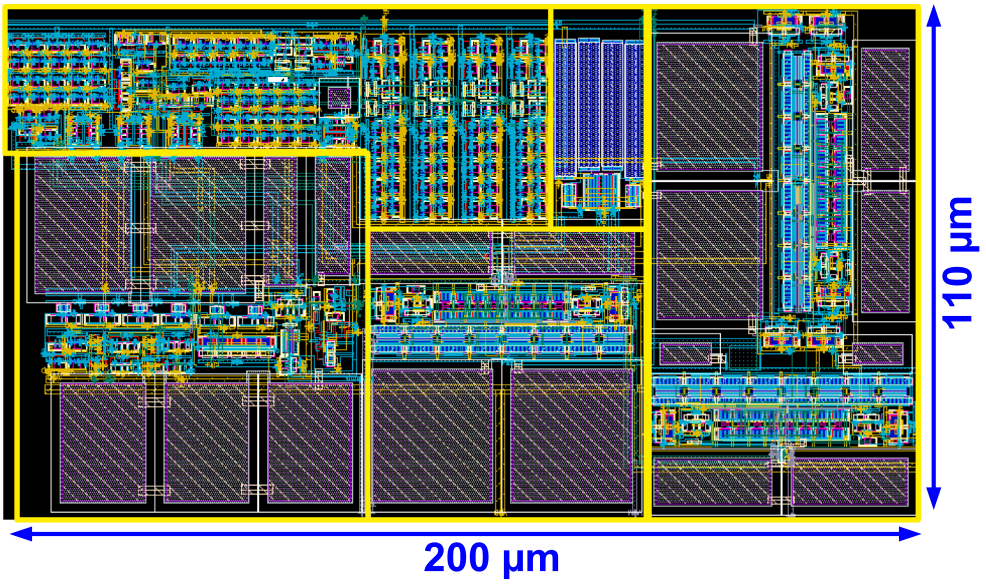


Fig. 11. Layout of the proposed PVT-robust FIDA.

Table 1
Simulated main FIDA parameter sizes.

Parameter	M	f	W (μm)	L (μm)
M_1, M_2	8	6	1.5	0.36
M_3, M_4	8	2	1.5	0.36
M_5, M_6	8	6	1.5	0.36
M_7, M_8	8	2	1.5	0.36
C_a, C_b	0.55 pF			

Table 2
Simulated auxiliary FIDA parameter sizes.

Parameter	M	f	W (μm)	L (μm)
M_1, M_2	8	6	1.5	0.36
M_3, M_4	8	2	1.5	0.36
C_0	0.55 pF			

$$\begin{aligned} V_+ &= V_{CM} + 0.5\Delta V_{CM} = \frac{R_{on1} + R_2}{R_{on1} + R_2 + R_1 + R_{on2}} V_{DD} \\ V_- &= V_{CM} - 0.5\Delta V_{CM} = \frac{R_{on1} + R_3}{R_{on1} + R_3 + R_4 + R_{on2}} V_{DD} \end{aligned} \tag{10}$$

where V_+ and V_- are the output voltages of the resistor dividers. R_{on1} and R_{on2} are the on-resistance values of M_1 and M_2 switches, respectively. ΔV_{CM} is a small constant differential voltage. From the relation (10), we have

$$\begin{aligned} & V_+ + V_- = V_{DD} \Rightarrow \quad V_- = V_{DD} - V_+ \\ \Rightarrow & \frac{R_{on1} + R_3}{R_{on1} + R_3 + R_4 + R_{on2}} V_{DD} = V_{DD} - \frac{R_{on1} + R_2}{R_{on1} + R_2 + R_1 + R_{on2}} V_{DD} \end{aligned} \tag{11}$$

After simplifying (11), the relation between R_1 and R_3 resistance values is calculated as below.

$$\begin{aligned} & if \;\; R_2 = R_4 \Rightarrow \\ R_1 &= \left(\frac{R_2 + R_{on1}}{R_2 + R_{on2}}\right) R_3 - (R_{on2} - R_{on1}) \left(1 + \frac{R_{on1}}{R_2 + R_{on2}}\right) \end{aligned} \tag{12}$$

According to the relation (12), when $R_{on1} = R_{on2}$, then $R_1 = R_3$. However, In Fig. 4(b), according to the detailed transient simulations, the on-resistance values of M_1 and M_2 switches are a little different and $R_{on2} > R_{on1}$. So, from the relation (12), R_1 and R_3 resistance values should be a little different, too, to achieve a symmetrical ΔV_{CM}.

The resistor ratios are PVT robust. Owing to the V_{DD} voltage variations, the comparator threshold voltage of $A_0 \times \Delta V_{CM}$ is also designed to be depending on V_{DD}. Therefore, the auxiliary FIDA input and the comparator threshold voltage will follow each other in PVT conditions as well.

The schematic of the comparator with the following SR-D-FF is illustrated in Fig. 5. The comparator is implemented with some cascaded inverters and switched-capacitor circuits [13]. The comparator is a dynamic power-efficient one which is appropriate for this work. The transmission gate and bootstrapping switches as shown in Fig. 6 [28] are employed here. As shown in Fig. 7, a low-power SR-D-FF based on transmission gates is utilized [29]. Another option to implement the dynamic comparator is the Strong-Arm latch structure. However, it needs a master clock with a high frequency (for example $f \geq 500$ MHz) to achieve enough accuracy in comparison with the ramp signal. Using this high frequency clock results in large kickback noise and increases the power consumption. So, the comparator of Fig. 5 is preferred in this work.

The comparator operation is briefly explained here. As shown in the timing diagram of Fig. 8, when the auxiliary FIDA is in the reset mode, $\phi_4 = 0$, the comparator is disconnected from the auxiliary FIDA. Meanwhile, $\phi_1 = \phi_2 = \phi_3 = 1$. The first inverter in the comparator is designed to be in the auto-zeroing configuration [13]. At this time, all the capacitors of the comparator sample the V_{CM}. After that, ϕ_3 drops and the bottom-plate of the capacitor C_r is connected from ground to V_{DD}. It results in increasing V_1 and V_2 node voltages by about a fraction of the V_{DD}. After settling of these node voltages, ϕ_1 and ϕ_2 will drop, and hence, the threshold voltage of the comparator is given by.

$$V_{th} = V_{CM} + \frac{C_r}{2C_t} V_{DD} \tag{13}$$

The threshold voltage of the comparator should be equal to $A_0 x \Delta V_{CM}$. According to the relation (13), the comparator threshold voltage variation over PVT just depends on V_{DD} because the capacitor ratio factor is PVT robust.

When SR-D-FF sets the $\phi_{amp} = 1$, the auxiliary and main FIDA turn on. So, the auxiliary FIDA output starts ramping. Meanwhile, $\phi_4 = 1$, and the auxiliary FIDA output is connected to the comparator input. When the ramp signal crosses the V_{th} value, the clock of SR-D-FF becomes high, and the amplification clock (ϕ_{amp}) is low. Then, the main and auxiliary FIDAs stop the amplification. The time window between the rising and falling edges of the ϕ_{amp} defines the amplification time window. When ϕ_{amp} becomes low, the auxiliary FIDA outputs are reset to V_{CM}. However, according to Fig. 1, the main FIDA output voltages remain constant. The load capacitors are disconnected from its output nodes to save its output voltage. Actually, in NS-SAR ADCs, the amplifier output voltage will be used in the next clock cycles, and hence, it should be saved in the reset phase as well.

2.4. Noise analysis

In this work, a clock control circuit is proposed to improve the PVT robustness of the main FIDA. The noise of the clock control circuit creates jitter at the amplification time (t_w), which results in the added input-referred noise in the main FIDA. The noise of the proposed clock control circuit includes the noise current of the auxiliary FIDA and the comparator input-referred noise. Using the similar noise analysis of [30], it can be proved that the input-referred noise of the main FIDA due to the clock jitter is obtained as.

$$\overline{V_{in,\,mainj}^2} = \frac{V_{in}^2}{(\Delta V_{CM})^2} \cdot \left(\frac{\tau_0}{\alpha_0 C_0}\right)^2 \left[\frac{4kT\gamma g_m}{t_w} + \left(\frac{C_{L0}}{t_w}\right)^2 \overline{V_{n,\,comp}^2}\right] \tag{14}$$

where g_m is the transconductance of the input transistors in the auxiliary

Table 3
Performance summary of the main FIDA before and after using the proposed gain calibration technique in worst-case PVT situations.

Parameter	FF @ 85 °C V_{DD} = 1.2 V	FF @ −40 °C V_{DD} = 1.3 V	FS @ 27 °C V_{DD} = 1.2 V	TT @ 27 °C V_{DD} = 1.2 V	SF @ 27 °C V_{DD} = 1.2 V	SS @ 85 °C V_{DD} = 1.1 V	SS @ −40 °C V_{DD} = 1.2 V
Gain (before cal.)	41.1	38	31.1	29.4	29.8	19.2	14.8
Gain var. (before cal.)	+39.8 %	+29.2 %	+5.7 %	–	+1.3 %	−34.7 %	−49.6 %
t_w (before cal.) (ns)	22	22	22	22	22	22	22
Gain (after cal.)	32	31	29.6	29.4	29.19	27.3	26.5
Gain var. (after cal.)	+8.8 %	+5.4 %	+0.6 %	–	−0.6 %	−7.1 %	−9.8 %
t_w (after cal.) (ns)	14.8	19.3	23.33	23.68	24.08	31.4	33.9
Power dissipation (μW)	98	62.5	46.14	51.3	56.2	43	40.6

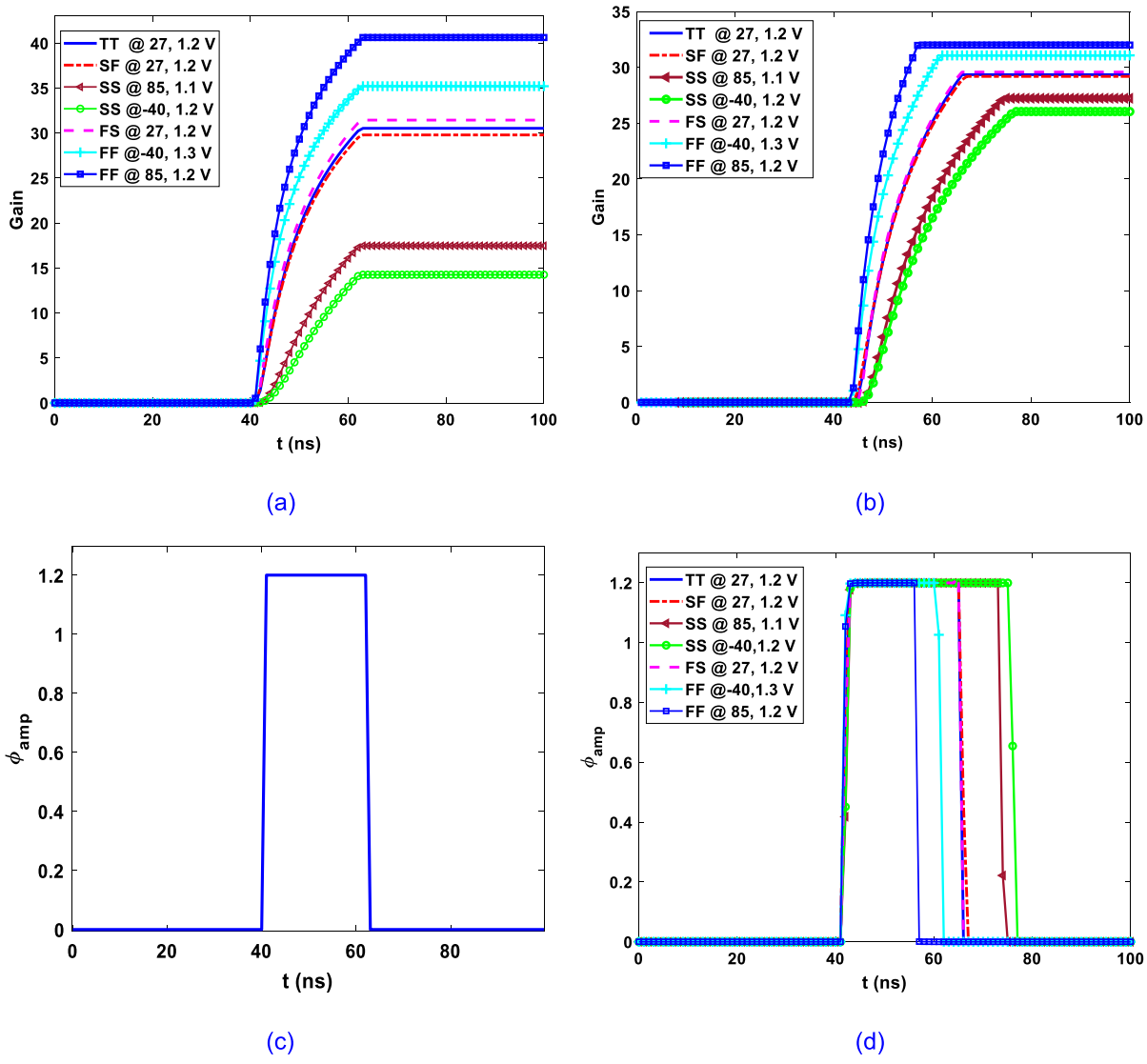


Fig. 12. Transient post-layout simulation results of the main FIDA gain (a) before and (b) after calibration in PVT corners, and the amplification clock phase (c) before and (d) after calibration.

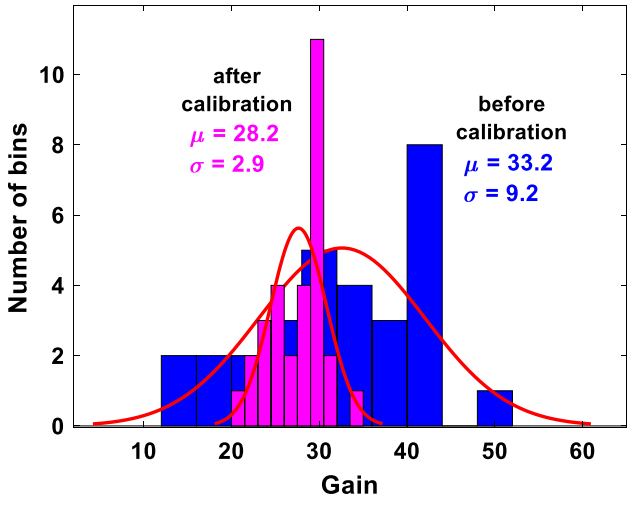


Fig. 13. Monte Carlo simulation results of FIDA gain before and after using the proposed gain calibration technique ($N = 30$).

FIDA, k is the Boltzmann's constant, and γ is the thermal noise excess factor of the MOS transistors. From the relation (14), to decrease the input-referred noise of the main FIDA due to the clock jitter, we should increase the auxiliary FIDA input voltage (ΔV_{CM}) or the amplification time (t_w). However, t_w depends on the speed specification of the main FIDA. Instead, we can increase the ΔV_{CM} while considering the auxiliary FIDA linearity. Increasing C_0 or decreasing τ_0 are the other ways to reduce the noise, although, they should be designed to achieve a power-efficient FIDA with a desired gain.

2.5. Clock generator

In this work, we use a master clock of 50 MHz to construct the clock phases of the switched-capacitor comparator as shown in Fig. 8. This master clock (*clk_s*) is chosen the same as the SAR ADC conversion clock frequency of [26] for compatibility purposes. Also, we use the reset signal of the SAR ADC (*R*) in this clock generator. We use a simple and low-power clock divider of [31], which is consisted of an array of dynamic D-FFs to create non-overlapping clock phases. Utilizing these non-overlapping clock phases accompanied by some logic gates, we implemented the clock generator circuit as depicted in Fig. 9 to realize the required clock phases of Fig. 8. The schematic of the D-FF and SR-Latch

Table 4
Performance comparison of the proposed PVT-robust FIDA with several similar state-of-the-art works.

Reference	Process (nm)	V_{DD} (V)	DAMP architecture	Max gain variation in PVT (%)	Area (mm^2)	Power (μW)	Gain	CMFB free	Method for PVT robustness
ISCAS'11 [9]*	90	1.2	Conventional	–	–	1050	15.5	NO	Calibration
JSSC'14 [11]	65	1	2-stage charge-steering	< 4 %	–	1000	10	NO	Calibration
TCAS-II'17 [12]	180	1.8	4-stage charge-steering	–	0.06	62	315	NO	Calibration
JSSC'17 [13]	65	1.3	PVT robust conventional	–	0.013	1100	5	NO	Using VTC
TCAS-II'18 [4]	130	1.2	Closed-loop class-AB RA	–	–	480	32	NO	Closed-loop DA
TCAS-II'19 [15]	65	1.2	PVT robust conventional	< 23.5 %	0.05	930	16	NO	Using VTC
JSSC'19 [5]	28	1	Gm-R based RA	–	–	3520	8	NO	Complete settled DA
TCAS-I'20 [16]	65	1	Gm-R based CAMP	< 10 %	–	–	30	NO	Complete settled DA
JSSC'21 [22]	65	1.1	Open-loop FIDA	< 10 %	–	23	16	YES	One-time tuning of C_{RES}
TCAS-II'23 [25]	40	1.1	Single-stage cascoded DA	< 3.8 %	0.0017	1150	16	NO	Clamping drain voltage
This Work*	180	1.2	PVT-robust FIDA	< 9.8 %	0.022	51.3	29.4	YES	Clock controlling circuit

* Post-layout simulation results.
RA = Ring-amplifier; CAMP = Clocked amplifier; FIB-DA = Floating inverter-based dynamic amplifier;
C_{RES} = Reservoir or storage capacitor.

of the clock generator are represented in Fig. 10.

3. Circuit level post-layout simulation results

To study the efficiency of the proposed PVT-robust FIDA, a sample design has been realized in 0.18-μm TSMC CMOS technology using Cadence Virtuoso. For TSMC 180 nm process, the nominal power supply voltage is 1.8 V. However, a smaller power supply voltage is highly preferred to reduce the power consumption and increase the device lifetime owing to the reduced device stress when all the other required design performance parameters can be satisfied as well. So, in this design, we used $V_{DD} = 1.2$ V to evaluate the performance of the proposed PVT-robust FIDA in comparison with the conventional one.

The metal–insulator-metal (MIM) capacitors are used to implement the capacitors. Fig. 11 shows the layout of the improved PVT-robust FIDA. As shown in Fig. 11, its active die area is 110 μm × 200 μm. We did not use finger insertion and we place the main and auxiliary FIDAs separated in the layout design to avoid complexity and coupling effects of two amplifier tracks on each other.

The total power consumption of the structure is 51.3 μW where 7.7 μW is dissipated in the clock generator, 5 μW is consumed by the FIDAs, 27.6 μW is consumed by the clock control circuit, and 11 μW is dissipated in the dynamic resistor dividers. The resistor divider power consumption can be highly reduced by choosing higher resistance values using PMOS transistors. The auxiliary FIDA only consumes 2 μW power from 51.3 μW total power dissipation. So, the auxiliary FIDA power consumption is <4% of the total power consumption which is negligible. The power overhead of the proposed gain calibration method is about 48 μW which is lower than many other published works [4,5,9,11,12,13,25]. The target gain of the main FIDA is about 30 in this work, which is appropriate for NS-SAR ADCs like [1,16,26]. The post-layout simulated device parameters of the main and auxiliary FIDAs are summarized in Tables 1 and 2, respectively.

To determine the performance of the proposed PVT-robust FIDA, the behavior of the main FIDA before and after using the proposed gain calibration technique is evaluated. The results of the post-layout circuit-level simulations in Cadence Virtuoso are summarized in Table 3. In these simulations, we assumed $\Delta V_{CM} = 40$ mV. As shown in Table 3, before using the clock control circuit, the FIDA gain is unstable over PVT variations with a constant amplification time window of 22 ns. However, after using the proposed technique, the gain of the FIDA will be almost robust over PVT changes. As presented in Table 3, the maximum gain variation over PVT changes is reduced from 49.6% to 9.8% when the proposed method is utilized. It means that the maximum gain variation of the FIDA after using the proposed technique is considerably reduced. Fig. 12 shows the transient post-layout simulation results of the main FIDA gain and amplification clock phase (ϕ_{amp}), before and after using the proposed gain calibration scheme. In Fig. 12, for better presentation and comparison, we have not illustrated the gain in dB as it is usual in DAMP references like [1,6,12,16,17], and [21].

The simulated input-referred noise of the main FIDA is about $V_n = 63$ μV_{rms} which is not significant. In this design, a large $\Delta V_{CM} = 40$ mV is selected to minimize the auxiliary FIDA noise and offset effects which are about 60 μV_{rms} and 4.5 mV, respectively. Also, a large ramp signal amplitude (input signal of the comparator) about 200 mV is chosen to minimize the comparator offset (<10 mV) and noise (<100 μV_{rms}) effects. So, these non-idealities are not critical in this work.

The effect of the device mismatches and process variations on the main FIDA gain has been evaluated by running Monte Carlo simulations with $N = 30$ runs using Cadence Virtuoso circuit simulator tool at normal environmental condition of TT @ 27 °C and $V_{DD} = 1.2$ V. The Monte Carlo simulation results of the FIDA gain before and after using the proposed technique is shown in Fig. 13. According to these results, the FIDA gain sensitivity to the device mismatches and process changes is substantially reduced. As shown in Fig. 13, the standard deviation reduction of the FIDA gain is about 70%.

A comparison performance summary is reported in Table 4. This work presents a power efficient and simple technique to improve PVT gain robustness compared to [4,5,9,11,13,15]. It is not a noisy method unlike [4,5]. The required active die area is less than [12,15]. Furthermore, it has lower maximum gain variation over PVT changes compared to [15,16,22]. Therefore, the resulting final gain is almost robust in various PVT conditions. It makes the proposed PVT-robust FIDA as a suitable choice for different low-power applications. The proposed gain calibration technique does not add any noticeable thermal noise to the FIDA input. Also, it does not need any additional storage capacitors for tuning opposed to [22,26]. From the simulation results, the proposed PVT-robust FIDA achieves a robust gain of 29.4 with an overall power consumption of 51.3 μW. The maximum gain variation is lower than 9.8% which is comparable with the recent state-of-the-art works.

4. Conclusion

This paper presents a novel method to reduce the FIDA gain variations in PVT corners. In the proposed technique, the amplification time window of the main FIDA is adjusted to be proportional to its time constant. Based on the FIDA gain formula, this method makes the FIDA gain to be nearly robust over PVT changes. The proposed method is simple, low power and low noise. Using this technique, the closed-loop FIDA structure, the storage capacitor tuning, and complicated power

consuming calibration schemes are not needed anymore. The proposed PVT-robust FIDA is designed at the circuit level using 0.18 μm TSMC CMOS process. Using this technique, the maximum FIDA gain variation over PVT changes has been significantly reduced from 49.6% to 9.8%. The FIDA gain sensitivity to the device mismatches and process variations is also reduced about 3-times after the calibration. The gain of the amplifier is 29.4 with 51.3 μW power consumption from a 1.2 V supply voltage. The power consumption of the proposed technique is lower than many other state-of-the-art calibration schemes. So, it is well-suitable for low power applications like NS-SAR ADCs.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

No data was used for the research described in the article.

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