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A fully dynamic third-order EF-CIFF noise-shaping SAR ADC with NTF zeros optimization and passive integration

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ABSTRACT

In this paper, a third-order noise-shaping successive approximation register (NS-SAR) analog-to-digital converter (ADC) is proposed which is simple and fully dynamic. A passive integrator is utilized in the feed-forward (FF) path of a second-order NS-SAR ADC with 2nd-order error-feedback (EF) filter to reduce the effect of inband quantization and comparator noise. The integrator implements a passive gain of 4x to make up its loss arising from the charge sharing between the integrator and digital-to-analog converter capacitors at the integration phase. Another advantage of the proposed structure is employing a simple low noise and low power one-input pair comparator unlike many published NS-SAR ADCs which use a comparator with multi-input pairs leading to enhanced comparator input-referred noise and power consumption. In this work, the zeros of the noise transfer function are optimized to enhance inband noise suppression. The proposed ADC is designed at circuit level using 0.18 μm TSMC CMOS technology with Cadence Virtuoso tool. The oversampling ratio, sampling frequency, and bandwidth are 8, 2.5 MS/s, and 156.25 kHz, respectively. According to the detailed post-layout simulation results, the achieved signal-to-noise and distortion ratio of the simulated ADC is 83.1 dB with 70.3 μW power consumption from a 1.1 V supply.

1. Introduction

The successive approximation register (SAR) analog-to-digital converters (ADCs) are one of the best structures for medium resolution and speed in low power utilizations. However, the SAR ADC is not suitable for high resolution and low power applications such as the sensors for internet of things (IoT) owing to their limited resolution. Unlike SAR ADCs, the sigma-delta (SD) ADCs have high resolution due to the oversampling and noise-shaping (NS) techniques. Nonetheless, sigma-delta ADCs use power consuming operational transconductance amplifiers (OTAs) to realize active integrators making them to be unsuitable for low power applications. So, recently several researchers have tried to combine the low power property of the SAR ADC with noise-shaping ability of SD ADC to build a low power and high resolution ADC structure called the NS-SAR ADC. NS-SAR ADCs have some superiorities compared to SD ADCs. First, the NS-SAR ADC uses just one digital-to-analog converter (DAC) in the feedback and quantization operation, so its circuit complexity is reduced. Second, the residue voltage is small and it is available on the DAC voltage rails when the SAR ADC conversion is completed. So, it alleviates the issues of the loop filter nonlinearity and design.

In the first published NS-SAR ADCs [1–3], the active OTA-based devices have been utilized which are not power efficient. To alleviate this issue, the first-order NS-SAR ADCs have been reported in [4,5] using only passive switched-capacitor (SC) elements and without needing any OTA resulting in more reduced power consumption. However, these structures have a weak noise-shaping ability due to the charge sharing loss in the passive switched-capacitor circuits. In [6,7], low power NS-SAR ADCs have been suggested which utilize the open loop dynamic amplifier (DAMP) based integrators to compensate the gain loss of the integrator. Therefore, it enhances the noise-shaping ability of the ADC.

In [8], a second-order NS-SAR ADC has been presented by utilizing the error-feedback (EF) scheme to implement the noise transfer function (NTF) with optimized zeros. Actually, it increases the noise-shaping ability by small changes in the traditional NS-SAR ADC structure. An energy efficient and scaling friendly error-feedback path is realized by using a passive finite impulse response (FIR) filter. In [8], the comparator is also utilized as a DAMP in addition to the comparison in two distinct phases. Although, its NTF coefficients depend on the capacitor value ratios not on their absolute values which make them to be robust

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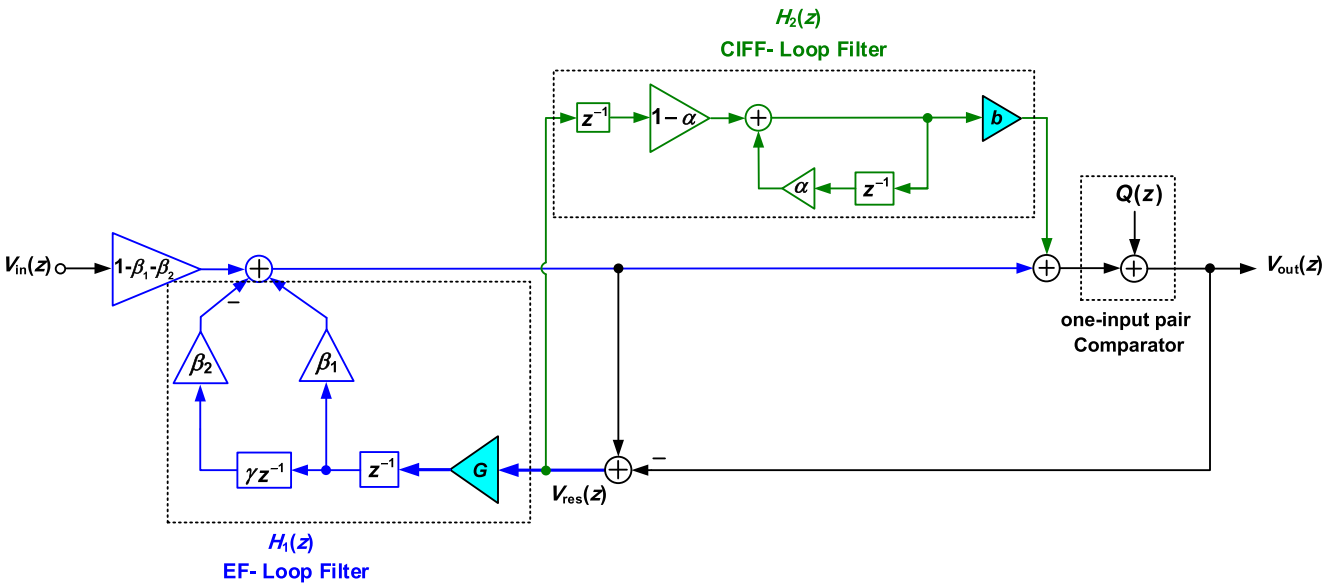

Fig. 1. Block diagram of the proposed third-order noise-shaping SAR ADC.

to the process, voltage, and temperature (PVT) variations. The DAMP gain depends on PVT variations. So, this structure uses a complex calibration procedure to solve this problem making it to be power inefficient and complicated. Furthermore, this design has finite quantization noise reduction ability at low frequencies, limiting its resolution to about 13 effective number of bits (ENOB).

In [9], a passive NS-SAR ADC is reported by employing the two-step integration to achieve a passive gain of two and embedded comparator gain ratio techniques. The comparator gain ratio technique is realized by scaling the aspect ratio of its input transistors, which is a power efficient way to provide the NS gain requirement, leading to the improved NS. But this method increases the comparator input-referred thermal noise and makes large mismatch in input transistors. Another method to obtain a gain passively is to put the integration capacitors in series with inputs of the comparator at opposite polarities in order to implement the passive addition of their voltages [10]. In this design, two capacitors retaining the residue voltage operate in a ping-pong manner and they are connected among the DAC array top plates resulting in more noise suppression. At the end of the conversion, a passive gain of two for residue voltage is obtained by stacking the capacitors.

In [11], a second-order fully passive NS-SAR ADC is presented that uses a comparator with three input pairs to provide a gain of 4 and 16 in the feed-forward path. Also, it employs a passive switched-capacitor (SC) integrator. However, the thermal noise of the comparator is high owing to the added input pairs. In [12], a configurable NS band-pass SAR ADC is implemented by an EF structure where the signal bandwidth is configured using an adjustable 2-tap SC FIR filter. In [13], a second-order NS-SAR ADC with two passive integrators is presented which are separated by the comparator preamplifier. So they are independent from each other and the capacitors size of the second integrator can be decreased. In [14], a second-order NS-SAR ADC based on a PVT robust closed-loop dynamic amplifier is reported. A second-order feed-forward (FF) NS-SAR ADC equipped with the ping-pong technique and dynamic integrator is presented in [15]. However, the last two structures use the noisy multi-input pair comparators. In [16], a second-order NS-SAR ADC with data-weighted averaging (DWA) technique is reported to alleviate the capacitors mismatch in DAC.

In [17], a closed-loop OTA is used as a PVT robust residue amplifier which does not need any calibration. But its power consumption and large input-referred noise reduce the efficiency of the NS-SAR ADC. Also, in [18], a first-order NS-SAR ADC is presented which just uses four stacked capacitors to implement a passive integrator with an embedded passive gain of 4, and its comparator has one-input pair with low thermal noise. A third-order NS-SAR ADC is presented in [19] which also suggest a kT/C noise reduction technique. In [20], a passive 2nd-order NS-SAR ADC is presented which uses the comparator gain ratio to compensate for the integration attenuation. In [21], a NS-SAR ADC with a voltage controlled oscillator (VCO) is presented where the VCO adds one order NS ability. However, in this structure, the VCO nonlinearity is the main issue [22].

In [23], a buffer-embedded NS-SAR ADC is presented. The input buffer separates the capacitive DAC (CDAC) from the sampling capacitor and cascaded integrator feed-forward (CIFF) NS filter capacitors. This method reduces the value of sampling and NS capacitors and results in an effective implementation of the following passive NS filter. But this buffer needs a separated power supply voltage and increases the ADC power consumption considerably. In [24], an EF NS-SAR ADC has been implemented using a unity-gain buffer and delay elements operating in a ping-pong method. Then the EF summation is done by stacking capacitors in series with comparator inputs. It does not need any residue amplifier but it needs a low power unity-gain buffer. Also it suffers from the kickback noise at the input of the comparator due to stacking capacitors. In [25], an EF second-order NS-SAR ADC based on the FIR- IIR filter is proposed with NTF zero-pole optimization.

In this paper, both error-feedback and cascaded integrator feed-forward techniques are utilized to realize a third-order NS-SAR ADC. As mentioned above, in many works, the comparator has been used as both the comparator and residue amplifier by scaling its input transistors size resulting in increased comparator input-referred noise and reduced ADC resolution. In this paper, one-input pair standard low noise comparator is utilized without any need to provide gain for residue voltage. Instead, a low-power floating inverter dynamic amplifier is employed to compensate the voltage attenuation raised of charge sharing summation in EF filter. Furthermore, a passive integrator in CIFF path is utilized to make a hybrid EF-CIFF structure to obtain high resolution. Also, this integrator provides a passive differential gain of 4 by stacking pre-charged integration capacitors in series with comparator inputs. So, this structure is simple and low power, and provides a third-order NS-SAR ADC which shapes the quantization and thermal noise of the ADC to higher frequencies efficiently. The early idea of the proposed NS-SAR ADC has been presented in [26]. Here, more detailed analysis, circuit level design, and post-layout simulation results are provided to evaluate the usefulness of the proposed ADC as well as its design and implementation issues.

The rest of the paper is arranged as follows. The proposed NS-SAR ADC structure and its analysis are presented in Section 2. Section 3 presents the circuit level implementation and noise analysis of the proposed ADC. The post-layout simulation results are reported in Section 4. Section 5 concludes the paper.

2. Proposed Third-Order NS-SAR ADC

In this section, first the structure of the proposed NS-SAR ADC is presented. Then, its system level design and analysis are provided.

2.1. ADC structure

Fig. 1 depicts the block diagram of the proposed third-order EF-CIFF NS-SAR ADC. Compared to the conventional SAR ADC, the proposed ADC has two additional NS filters. $H_1(z)$ is a low-power DAMP-assisted 2nd-order FIR error-feedback loop filter and $H_2(z)$ is a fully passive cascaded integrator feed-forward (CIFF) loop filter to boost the inband noise attenuation mainly at low frequencies. $V_{\text{res}}(z)$ is the residue voltage of the ADC which is accessible at the top plates of the capacitive DAC (CDAC) after the termination of the SAR conversion. The unitary delays in EF and CIFF paths represent the reality that the quantization error only will be used in the latter conversion cycle. We use a one-input pair comparator without any embedded gain. Instead, the CIFF loop provides a passive gain of b by stacking capacitors to compensate the CIFF-filter path attenuation.

Our work follows the error-feedback scheme in [8,12] to design the second-order error-feedback filter ($H_1(z)$). In EF path, the quantization error is summed with the sampled input voltage via charge sharing between the CDAC and FIR capacitors that is a simple and power-efficient way. Nevertheless, this charge sharing makes the voltage attenuation resulting in degraded NTF in ADC. So, similar to [8,12,27], a DAMP (G) is employed to amplify the residue voltage before the charge sharing in order to alleviate the NTF degradation. Furthermore, DAMP helps us to employ sort of small capacitors in EF FIR path leading to small area overhead.

In Fig. 1, γ, β_1 and β_2 are charge sharing attenuation factors. As mentioned before, albeit the DAMP solves the EF filter loss issue, but there is also attenuation in input signal voltage (V_{in}). The coefficient of (1- β_1- β_2) represents this attenuation factor in Fig. 1. The CIFF filter ($H_2(z)$) is the next part of our structure. This part is designed by a passive, low-power, switched-capacitor integrator with a passive gain [18] with some switches and capacitors. The integrator pole is the zero of the system NTF. Therefore, we design this pole as close to DC ($z = 1$) as possible to boost the quantization noise suppression at low frequencies. The (1-α) factor is the attenuation coefficient of the integrator resulted from the charge sharing among the integrator capacitors and DAC. α is the integrator pole that drifts from $z = 1$ because of the charge sharing effect. The value of α can be adjusted by setting the integrator and DAC capacitor values ratio. So, the feed-forward structure transfer function can be designed and it is not fixed. b is a passive gain which is implemented by stacking integrator capacitors at the conversion phase of the ADC in series with comparator inputs. So, just a one-input pair comparator is enough for this structure and it does not need any comparator with multiple input pairs. As mentioned already, by using a multi-input pair comparator, we can get a passive gain ratio to compensate the integration loss. However, this way increases the comparator input-referred noise and power consumption. So that, if we use a multi-input pair comparator with input pair ratio of 1:n, it leads to $(1+n)^2$ times larger input-referred noise compared to the standard one-input pair comparator [11,18]. Also, its power consumption increases multiple times higher than the standard one. So, in this method, the comparator noise can be a dominant limiting factor for performance of the ADC. Therefore, in this work, we use a one-input pair comparator to prevent these problems.

2.2. System-level design and analysis

As illustrated in Figs. 1, $H_1(z)$ and $H_2(z)$ are represented as below:

$$H_1(z) = G\left(\beta_1 z^{-1} - \beta_2 \gamma z^{-2}\right) \tag{1}$$

$$H_2(z) = bz^{-1}\frac{(1-\alpha)}{1-\alpha z^{-1}} \tag{2}$$

Also, according to Fig. 1, the input–output relation of the proposed ADC is given by:

$$V_{out}(z) = (1-\beta_1-\beta_2)V_{in}(z) + \frac{1-H_1(z)}{1+H_2(z)}Q(z) \tag{3}$$

where $Q(z)$ is the ADC's quantization noise. The zeros of 1-$H_1(z)$ and the pole of $H_2(z)$ form the NTF zeros. From (3), the signal and noise transfer functions are given by:

$$\begin{cases} STF(z) = 1-\beta_1-\beta_2 \\ NTF(z) = \dfrac{1-H_1(z)}{1+H_2(z)} = \dfrac{(1-\alpha z^{-1})\left(1-G\beta_1 z^{-1}+G\beta_2\gamma z^{-2}\right)}{1-(\alpha - b(1-\alpha))z^{-1}} \end{cases} \tag{4}$$

The SAR ADC usually employs the multi-bit quantization in the NS-SAR ADC. This property relaxes the stability of traditional high-order sigma-delta ADCs with a coarse quantizer. Therefore, we can design a high-order NTF in noise-shaping SAR ADCs safely. Of course, a higher order NTF needs more area, and it is more complicated. Therefore, taking into account this trade off, we considered a third-order NTF to be implemented as (4). The optimum location of the NTF zeros in a third-order noise-shaping ADC is given by [28]:

$$\begin{aligned} &\frac{f_1}{f_s} = 0 \ ; \\ &\frac{f_{2,3}}{f_s} = \pm\sqrt{\frac{3}{5}}\cdot\frac{f_b}{f_s} = \pm\sqrt{\frac{3}{5}}\cdot\frac{1}{2\times OSR} \end{aligned} \tag{5}$$

where f_1 and $f_{2,3}$ are frequencies of the NTF zeros. f_b and f_s are the ADC bandwidth and sampling frequency, respectively. The optimum NTF zeros location and their frequencies relation is $z_{opt} = \exp(j2\pi f_{opt}/f_s)$. So from the relation (5) and considering OSR = 8, the location of the optimum zeros is obtained as:

$$\begin{aligned} &z_{opt_1} = e^0 = 1; \\ &z_{opt_{2,3}} = e^{j2\pi\frac{f_{2,3}}{f_s}} = \cos\left(2\pi\frac{f_{2,3}}{f_s}\right) + j\sin\left(2\pi\frac{f_{2,3}}{f_s}\right) = 0.954 \pm j0.299 \end{aligned} \tag{6}$$

In the proposed ADC, both CIFF and EF techniques are utilized to realize the NTF given in (4). In this architecture, two complex conjugate zeros are realized in the error-feedback path and the DC zero is realized by the CIFF path. The CIFF path is consisted of a passive integrator. As known, the passive integrators response is not accurate owing to the charge-sharing effect that makes some deviations at the location of their pole. So, the integrator pole will be inside the unit circle. By assuming $z_1 = 0.8$ and $z_{2,3} = 0.954 \pm$ j 0.299, we have:

$$\begin{cases} z_2+z_3 = 1.908 \\ z_2 \cdot z_3 = 1 \\ z_1 = 0.8 \end{cases} \Rightarrow \text{NTF Numerator} = \left(1-0.8z^{-1}\right)\left(1-1.908z^{-1}+z^{-2}\right) \tag{7}$$

Therefore, comparing (4) and (7), we have:

$$\begin{cases} \alpha = 0.8 \\ G\beta_1 = 1.908 \\ G\beta_2\gamma = 1 \end{cases} \tag{8}$$

By assuming $G = 30$, $\gamma = 0.476$, and $b = 4$ (later they will be explained more), the values of β_1 and β_2 can be calculated. With this information, the NTF pole is eliminated. So the $NTF(z)$ is simplified as:

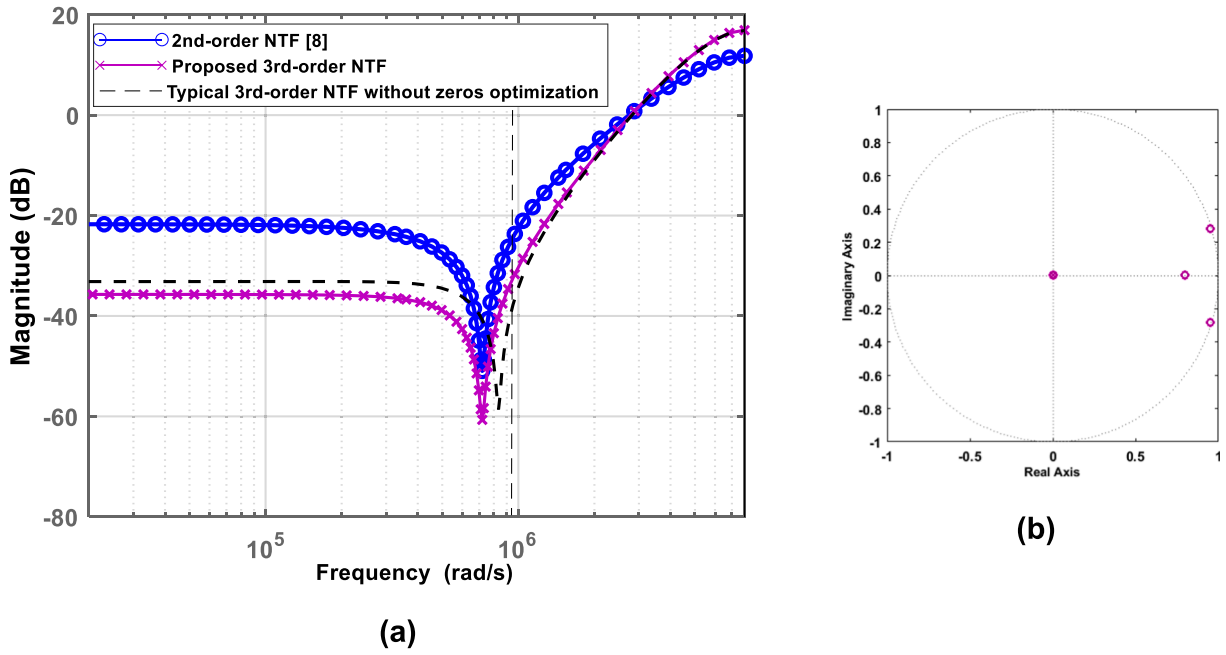

Fig. 2. (a) The magnitude of the intended NTF compared to the second-order NTF in [8] and a typical 3rd-order NTF without the zeros optimization, and (b) pole-zero plot of the intended NTF.

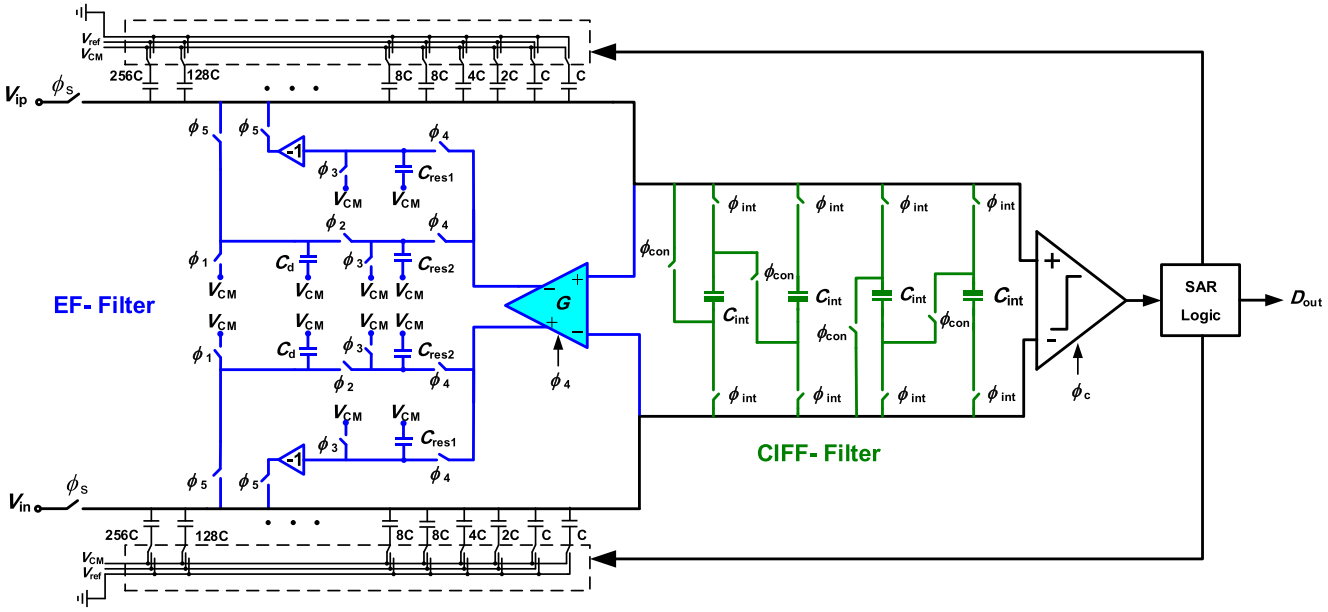

Fig. 3. Top-level schematic of the proposed third-order NS-SAR ADC.

$$NTF(z) = \left(1 - 0.8\,z^{-1}\right)\left(1 - 1.908\,z^{-1} + z^{-2}\right) \tag{9}$$

The obtained $NTF(z)$ has three zeros within the unit circle. Fig. 2(a) illustrates the bode diagram of the intended third-order NTF compared to the second-order NTF which has been realized in [8] and a typical 3rd-order NTF without the zeros optimization ($G.\beta_1 = 1.88$). The NTF magnitude is attenuated remarkably around the frequency of the zeros. So positioning the input signal bandwidth around the NTF's zeros results in an efficient ADC resolution. As shown in Fig. 2(a), two complex conjugate zeros create a deep notch at the inband frequencies. Owing to the added DC zero in the proposed NTF, the noise suppression is enhanced compared to the second-order NTF and 3rd-order NTF without the zeros optimization. As depicted in Fig. 2(b), the proposed structure has two complex conjugate zeros. However, the complex zeros are very close to the unit circle and the third zero is near to DC. They don't position precisely on the unit circle because of optimizing their location and also owing to the charge sharing attenuation effect in the passive integrator.

3. Circuit implementation of the proposed third-order NS-SAR ADC

In this section, the circuit level realization of the proposed NS-SAR ADC is explained with some details.

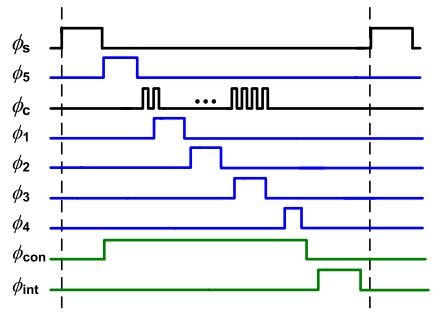

Fig. 4. Timing diagram of the proposed third-order NS-SAR ADC.

3.1. SAR ADC core

Fig. 3 shows the circuit level schematic of the proposed ADC, which contains a 10-bit SAR ADC. There are several proposed DAC switching methods to reduce the DAC switching energy and area such as those presented in [29,30,31,32]. In this work, we use the DAC switching method suggested in [29] which has three positive features. First, it has low switching energy and small overall required CDAC size. Second, an imprecision of the mid-level reference voltage (V_{CM}) does not affect the ADC accuracy. Third, it has constant common-mode voltage at the input of the comparator which relaxes the comparator realization. So it provides a fixed common-mode voltage for the comparator and the DAMP [29].

The timing diagram of the proposed NS-SAR ADC is depicted in Fig. 4. The SAR ADC has 10-bit binary weighted DAC with one redundant bit at 8C to reduce the CDAC settling error. The total value of capacitors in each top and bottom DAC arrays is considered 5.2 pF in order to achieve the kT/C noise limited performance. As shown in Fig. 3, the total capacitance of each CDAC array is 512C where C is the unit capacitance. So, C is considered as 10 fF. The DAC capacitors are implemented with metal–insulator-metal (MIM) capacitors. The basic operation of the conventional SAR ADC without noise-shaping is as follows. At the sampling phase, ϕ_s, the differential input signal is sampled on the CDAC top plates and the MSB, b_9, is determined just by the comparator decision once the conversion phase ϕ_c is started. Then depending on the b_9 value, the SAR logic decides to switch the MSB capacitor. At the same time, the initial guess of the b_8 is set to 1 which after one conversion CLK cycle, its real value will be recognized by the comparator decision. This procedure continues until all bits are obtained. Moreover, in NS-SAR ADC, the last bit, b_0, should be sent back to the CDAC to produce the final residue voltage, V_{res}, on the DAC top plates. This step is not required in conventional SAR ADCs without the noise-shaping.

3.2. CIFF NS filter

As illustrated in Fig. 3, the NS-SAR ADC has two noise-shaping filters including CIFF and EF filters. The CIFF filter is a passive integrator based on [18]. It consists of some switches and capacitors and employs the differential integration to decrease the required capacitor size for integration. It eliminates the ground connection of the single-ended integrator capacitors and replaces two single-ended capacitors with one differential capacitor. In this way, the whole needed integration capacitor size is reduced to a quarter compared with a single-ended integrator whereas their transfer function is the same [18]. As for all passive integrators, this passive integrator also encounters the signal attenuation. This is because of charge sharing between the integrator capacitors and CDAC. To alleviate this issue, most of the works [4,11,20,23,25,33] use a comparator with multi-input pairs to implement an embedded gain ratio between the input transistors of the comparator leading to the increased comparator thermal noise. But the proposed integrator in [18], implements a passive gain of 4 by stacking the integration capacitors in two groups with opposite polarity at the conversion phase.

As shown in Fig. 5(a), the value of integration capacitors is the same and it is equal to half of the CDAC capacitor (2.6 pF). This integrator operates in two phases of ϕ_{con} and ϕ_{int}. At the phase of ϕ_{int}, eight integration switches are on and all integrator capacitors are in parallel between the top plates of DAC arrays as shown in Fig. 5(a). According to the timing diagram of Fig. 4, this phase is performed after the end of the SAR conversion phase. So, the charge sharing is done between the integrator and CDAC capacitors. The integrator capacitors carry prior cycle integration voltage ($V_{int}(n-1)$) while CDAC holds the residue voltage of the SAR conversion ($V_{res}(n-1)$). Finally, it implements the passive integration of $V_{int} = V_{res} \times 0.2z^{-1}/(1–0.8z^{-1})$. By terminating this phase, the integration switches are turned off while the voltage of V_{int} is stored on each of integration capacitors (Fig. 5(a)). After signal sampling, during the conversion phase of ϕ_{con} (Fig. 5(b)), the 4 conversion switches are on to stack the 4 small integration capacitors over the DACs with opposite polarities resulting in the passive gain of four on V_{int} and the passive addition of $V_{dac} + 4V_{int}$. Based on the above discussion and according to Fig. 1, Fig. 5, and relation (4), the assumptions of $b = 4$ and $\alpha = 0.8$ in systematic design are verified. Note that in this work, bootstrapped switches are used to reduce the parasitic capacitances around switches to prevent the NTF degradation [18].

In the capacitor charge pump technique, if we split the capacitor of the integrator into more parts, then it is possible to implement a larger passive gain [18]. However, it increases the parasitic capacitance around the integrator capacitors leading to attenuate the integration result.

3.3. EF NS filter

The sampling switch in this structure is implemented as a bootstrapped switch to enhance the ADC's linearity [34]. As shown in Fig. 4, most of EF NS process is performed during the SAR conversion phase which does not limit the bandwidth of the ADC since it does not need a lot of time overhead. As depicted in Fig. 3, the capacitors of passive FIR

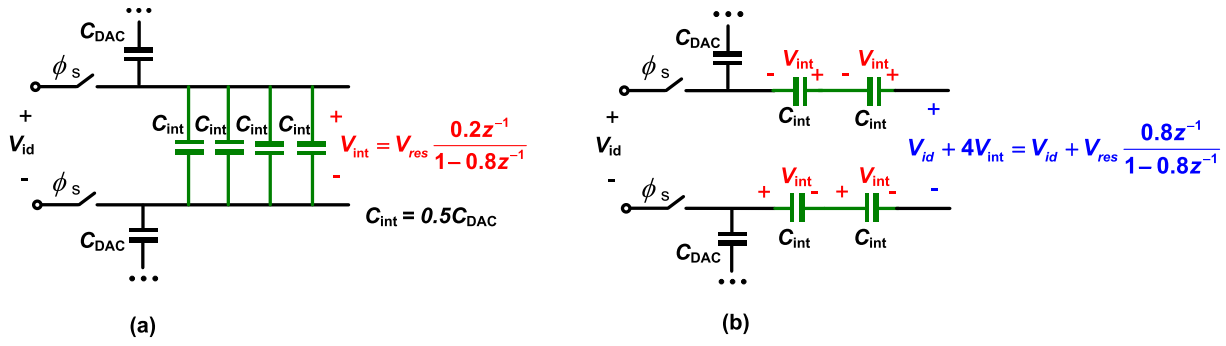

Fig. 5. (a) Differential integration with separated integration capacitors at ϕ_{int}, and (b) stacking integration capacitors during ϕ_{con}.

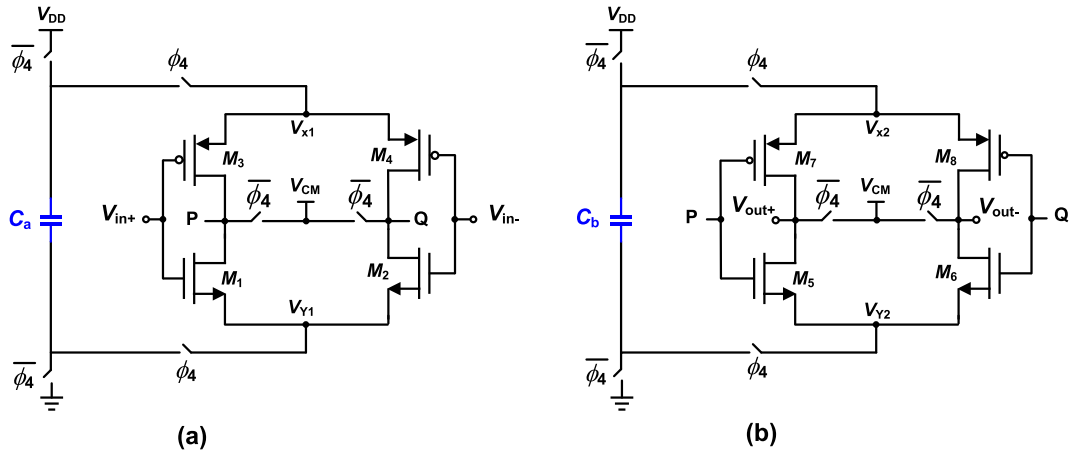

Fig. 6. Schematic of the two-stage FIDA, (a) first stage and (b) second stage.

filter include C_{res1}, C_{res2}, and C_d capacitors. The C_{res1} acts as a 1-cycle delay and C_{res2} and C_d act as a 2-cycle delay with an attenuation of 0.476 caused by the charge sharing between them. The -1 gain is not a real amplifier. It is just employed by cross-coupling in the fully-differential structure, where for simplicity; it is represented like this in Fig. 3. C_{res1} and C_{res2} have the same nominal capacitance of 382 fF, and C_d capacitance is equal to 420 fF. These values are considered to realize the coefficients of the FIR filter as below (Fig. 1):

$$\gamma = \frac{C_{res2}}{C_{res2} + C_d} = 0.476 \tag{10}$$

$$\beta_1 = \frac{C_{res1}}{C_{res1} + C_d + C_{DAC}} = 0.0636 \tag{11}$$

$$\beta_2 = \frac{C_d}{C_{res1} + C_d + C_{DAC}} = 0.07 \tag{12}$$

With the above-considered coefficients, we obtain our proposed EF NTF given in relation (9). In practice, the NTF attenuation caused by the mismatch among the FIR filter capacitors is insignificant [8]. So it is neglected. All the switches of the FIR filter are implemented by CMOS switches to reduce their on resistance with high linearity and alleviate the charge injection and clock feed-through issues in switched-capacitor circuits [35,36]. As mentioned in Section 2 and shown in Fig. 3, a low-power differential DAMP is utilized to compensate the attenuation of the EF filter coefficients. The details of this amplifier circuit will be presented in Section 3.4.

According to the timing diagram of Fig. 4, the basic operation of the EF filter is as follows. At the sampling phase of ϕ_s, the differential input signal is sampled on the CDAC. Then throughout ϕ_5, the EF capacitors of C_{res1} and C_d are connected to the CDAC which results in charge sharing summation between the current sampled input signal and last cycle EF NS voltage. However, the input signal amplitude is attenuated by a factor of $1-\beta_1-\beta_2$, too. So, at the start of the ADC conversion phase of ϕ_c, the $(1-\beta_1-\beta_2)V_{in} + V_{EF}$ will enter into the quantizer to produce the digital output code. Parallel to ϕ_c, the EF filter operates in some phases independently to prepare the situation of sampling new residue voltage at the end of the conversion cycle. During ϕ_1, the voltage on the C_d capacitor resets to V_{CM}. Then at ϕ_2, C_d is connected in parallel to C_{res2} to sample the last cycle residue voltage with one-cycle delay. At ϕ_3, the voltage on C_{res1} and C_{res2} reset to V_{CM}. After the conversion cycle, during ϕ_4, the DAMP turns on and C_{res1} and C_{res2} are connected to its output. At this phase, the current residue voltage on CDAC top plates is amplified and saved on the residue capacitors to sum with the next cycle input sample. Therefore, the EF and FF NS filters work independently at different phases resulting in an effective noise-shaping action.

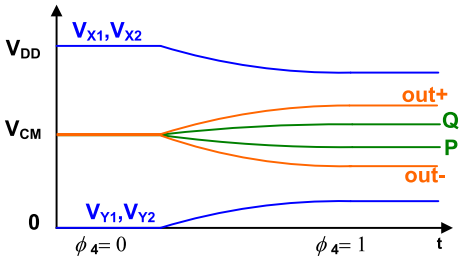

Fig. 7. Timing diagram of the two-stage FIDA.

3.4. The dynamic amplifier circuit

In [37], the presented dynamic amplifier uses a floating inverter-based dynamic amplifier (FIDA) structure. The FIDA works at the same way as quasi-differential inverter-based amplifiers. Although, rather than connecting to the actual V_{DD} and ground, a charged floating storage capacitor is used to supply it. An explanation of the DAMP operation will be provided briefly here. The FIDA provides some absorbing features, like large input common-mode voltage range, fixed output common-mode voltage, and current reuse. In [14], the FIDA is used as a residue amplifier in the closed-loop configuration. Also, in [38], it is utilized as a time-controlled open-loop amplifier. Although in close-loop format, the FIDA is greatly PVT robust, it brings rather large noise within the charge transfer phase. Instead, in [19], the FIDA is employed in an open-loop self-quenching way which does not require a close-loop configuration or any timer.

In this work, we use a two-stage FIDA structure based on [19] to provide a sufficient gain of $G = 30$ for the residue amplification. This structure is shown in Fig. 6. During $\phi_4 = 0$, the storage capacitors C_a and C_b are connected between V_{DD} and ground for recharging. When $\phi_4 = 1$, C_a and C_b capacitors are disconnected from the power lines and they are utilized to supply currents to the inverters. When the capacitor's charges are being removed, the voltage across the inverter pairs falls, that decreasing the transistor's current. Therefore, the amplifier turns off step by step with a stabilized dynamic gain as illustrated in Fig. 7.

The time-dependent gain expression of the FIDA is represented in [19]. As reported, the FIDA gain increases with a natural logarithmic characteristic of the time. More exactly, it won't completely terminate on its own. However, practically, when the amplifier running window is greater than $5\tau_0$, where $\tau 0$ is the discharge time constant of the FIDA at the onset of the working ($t = 0^+$), the FIDA gain is very time-insensitive. For example, changing the amplifier working time by 10% only alters its gain below 1%. So, using FIDA without any timer is safe. Also based on the same reason, the FIDA gain shows relatively sufficient resistance to

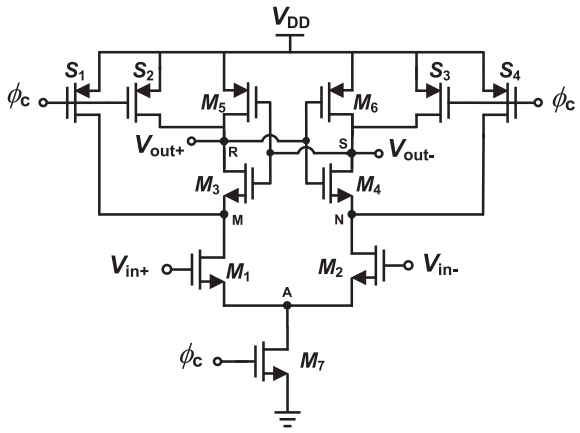

Fig. 8. Schematic of the comparator [42].

the PVT variations since the PVT changes mostly affect τ_0 [19].

During simulation, a one-time adjustment of C_a and C_b values was made to compensate for the process corner variations which is the same as a one-point calibration of temperature sensors. The trim chip has a FIDA gain of about 30 when simulated at $V_{DD} = 1.1$ V and the temperature of 27 ºC. Manual tuning of C_a and C_b is done in other PVT corners test to obtain a fine-tuned amplifier gain for each corner which will be done by off-chip capacitors. In this work, unlike other works like [8], no complicated or power-consuming calibration is required on dynamic amplifier, apart from this one-step tuning. Actually, when the ADC turns on, the gain of the FIDA can be checked by its input and output test pins which are prepared to be available to measure the gain. Then, if there is any deviation in the gain from the nominal value of 30, we can trim the capacitors of C_a and C_b by adding some off-chip capacitors in parallel to them, between the available pins, to get the desired gain value. In this work, we have done this trimming at process corner cases.

3.5. The comparator circuit

The static comparators are power consuming and are not appropriate for low power applications like SAR ADCs. Nevertheless, the dynamic latch comparator is a suitable choice for low power applications. The dynamic latch comparator can be encountered with some issues such as the input-referred offset voltage and kickback noise. However, if they are critical, they can be alleviated by several efficient and low-power techniques [39–41]. So, in this work, we use the Strong-ARM dynamic latch comparator with one-input pair which is a widely used topology as the comparator, sense amplifier, or simple robust high sensitive latch [42]. Also, it is favorable in many low-power, high-speed applications such as SAR ADCs. The circuit of the comparator is shown in Fig. 8. This structure is fully dynamic and it does not consume any static power. When $\phi_c = 0$, the comparator is in "Reset" mode and S_1-S_4 transistors are on, and M, N, R, and S nodes are connected to V_{DD}. So in this mode, parasitic capacitances of C_M, C_N, C_R, and C_S are charged to V_{DD}. However, M_1-M_7 transistors are in cut-off region. When $\phi_c = 1$, the comparator comes in "Evaluation" and next "Latch" mode. In this mode, S_1-S_4 transistors are off while M_1, M_2 and M_7 transistors turn on. So, C_M and C_N capacitors are discharged at different rates proportional to the differential input voltage of $(V_{in+} - V_{in-})$. Whenever the voltage across C_M, C_N falls to V_{DD}-V_{THn}, M_3 and M_4 transistors will be turned on and after enough discharging of C_R and C_S, the transistors of the cross-coupled latch will be turned on and the comparator result is generated. Using M_3 and M_4 transistors, no static current is consumed by this comparator so it is fully dynamic and low power [42].

3.6. Noise and non-ideality analysis of the proposed ADC

Fig. 9 shows the noise and non-ideality analysis of the proposed third-order NS-SAR ADC. We study these non-ideality sources to recognize which ones are more dominant and which ones are negligible. According to Fig. 9, the output of the ADC with neglecting the input signal is obtained as:

$$\begin{aligned} N_{out,tot}(z) = {} & \left[Q(z) + N_{comp}(z) + N_{DAC}(z) + V_{OS}(z)\right].NTF(z) \\ & + \left[N_{amp}(z) + N_{EFC}(z)\right].G.z^{-1}\left(\beta_1 - \gamma.\beta_2.z^{-1}\right) \\ & + N_{res1}(z).\beta_1 + \left[N_{drst}(z) + N_{res2}(z)\right].\gamma.\beta_2.z^{-1} \\ & + N_{dres2}(z).\beta_2 + N_{samp}(z).(1 - \beta_1 - \beta_2) \\ & + N_{int}(z).\frac{b}{1-(\alpha - b(1-\alpha)).z^{-1}}\left[1 - G.z^{-1}\left(\beta_1 - \gamma.\beta_2.z^{-1}\right)\right] \\ & + \varepsilon_{DAC}(z) \end{aligned} \tag{13}$$

where $Q(z)$, N_{comp}, N_{DAC}, and V_{os} are the quantization noise of the ADC, thermal noise of the comparator, thermal noise of the DAC at the conversion phase, and offset of the comparator, respectively. These four non-ideality terms transfer to the output by the system NTF. Therefore, they will be third-order shaped and have insignificant effect on the total performance of the ADC. N_{amp} is the FIDA input-referred noise given by $2nkT/(G.CL.\mathrm{OSR})$ [14,37] where n is the slope factor of the sub-threshold MOS transistor. We simulated the FIDA noise then considering its coefficient from (13). So we obtained its portion from total output noise which is about 25 μVrms. N_{EFC} catches the sampling noise stored on the C_{DAC}, whenever unzipping from the FIR capacitors, prior to

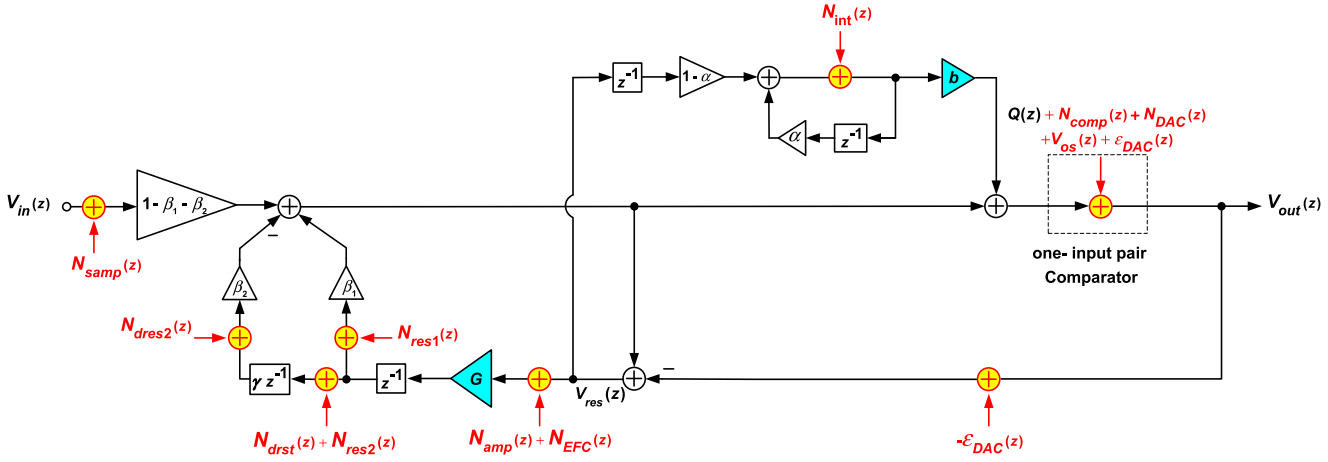

Fig. 9. Non-ideality effects in the proposed third-order NS-SAR ADC.

Table 1
Noise budgeting in the proposed NS-SAR ADC.

Noise source	RMS Voltage	Percentage
Sampling	12 μVrms	23.5%
Quantization	5 μVrms	10%
SC EF FIR filter	9 μVrms	17.5%
FIDA	25 μVrms	49%

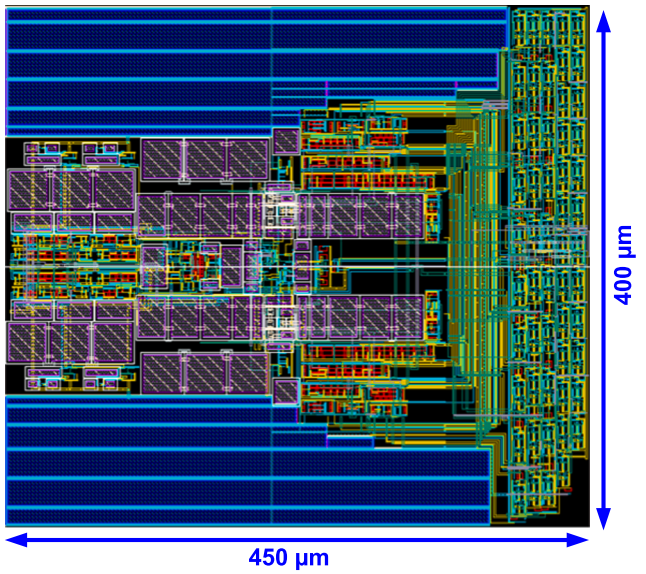

Fig. 10. Layout of the proposed 3rd-order NS-SAR ADC.

the residue amplification phase, which is obtained as $2C_{res}/(2C_{res} + C_{DAC})$x $2kT/(C_{DAC}.\mathrm{OSR})$. According to the relation (13), N_{amp} and N_{EFC} are first-order shaped. N_{res1}, N_{res2}, N_{drst}, and N_{dres2} are related to the switching noise sources of the SC FIR filter in the EF path. So $N_{res1} = N_{res2} = N_{drst}$ noise sources are equal to $2kT/(C_{res}.\mathrm{OSR})$ and $N_{dres2} = kT/(C_{res}.\mathrm{OSR})$. Considering their coefficients from (13), We calculated the sum of their noise contributions which is about 9 μVrms. N_{samp} is the differential input sampling noise on the C_{DAC} given by $2kT/(C_{DAC}.\mathrm{OSR})$ which has a coefficient of $(1 - \beta_1 - \beta_2)$ in (13). So it is obtained as 12 μVrms. N_{int} is the noise of the passive integrator received by the integrator capacitor at the integration cycle which is represented as $1.6kT/(C_{DAC}.\mathrm{OSR})$ [18]. It will be second-order shaped and has insignificant effect on the total output noise. As mentioned, $Q(z)$ is the quantization noise of the ADC which is third-order shaped. So, its value can be calculated by $(V_{LSB})^2/12\mathrm{x}\ \pi^6/(7.\ \mathrm{OSR}^7)$ where V_{LSB} is the LSB value of the ADC [36]. The obtained Q(z) is about 5 μVrms. Finally, ϵ_{DAC} is the DAC mismatch nonlinearity effect. These noise sources construct the total output noise power of the ADC. The obtained main noise portions in the proposed ADC are summarized in Table 1.

4. Post-layout simulation results

To evaluate the usefulness of the proposed third-order NS-SAR ADC, a design prototype has been carried out and it has been designed in 0.18-μm TSMC CMOS technology with 1.1 V power supply. The metal–insulator-metal (MIM) capacitors are used to realize the required capacitors. The sampling frequency of the proposed ADC is 2.5 MHz with an OSR of 8 which results in 156.25 kHz signal bandwidth. Fig. 10 depicts the layout of the designed ADC. As shown in Fig. 10, the active area of the simulated ADC is 400 μm × 450 μm. In blank spaces, MOS decoupling capacitors have been widely utilized between the power supply voltage (V_{DD}) and the ground. Its total power consumption is about 70.3 μW where 5.6 μW is consumed in the analog part including the comparator (3.1 μW) and FIDA (2.5 μW). The power of 29 μW is consumed by the digital part and 35.7 μW power is dissipated by the CDAC. The simulated device parameters of the comparator and FIDA have been summarized in Table 2 and Table 3, respectively.

Table 2
Simulated comparator parameter sizes.

Parameter	M	W (μm)	L (μm)
M_1, M_2	1	1.8	0.18
M_3, M_4	1	0.72	0.36
M_5, M_6	1	0.54	0.18
M_7	1	0.22	0.18
S_{1-4}	1	0.54	0.18

Table 3
Simulated FIDA parameter sizes.

Parameter	M	W (μm)	L (μm)
M_1, M_2	2	1	0.36
M_3, M_4	6	1	0.36
M_5, M_6	6	1	0.36
M_7, M_8	4	1.2	0.36
C_a	1 pF		
C_b	1.1 pF		

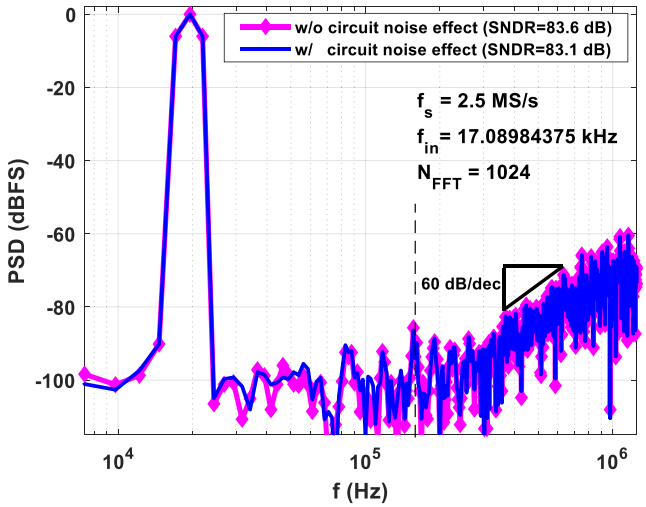

Fig. 11. Post-layout simulated output spectrum of the proposed third-order NS-SAR ADC with and without the circuit noise effect (TT @ 27 °C; V_{DD} = 1.1 V).

Fig. 11 shows the post-layout simulation result of 1024 points Fast Fourier Transform (FFT) spectrum with Hann window, which is obtained using Cadence Virtuoso circuit simulator tool. According to Table 1, the overall circuit noise voltage is about 51 μVrms. The circuit noise is considered in FFT simulation. Fig. 11 also illustrates FFT result with and without the circuit noise consideration. As shown in Fig. 11, the slope of the out-of-band noise is 60 dB/dec which corresponds to the third-order noise-shaping. Over 156.25 kHz signal bandwidth, the achieved peak signal-to-noise and distortion ratio (SNDR) is about 83.1 dB and 83.6 dB with and without the circuit noise effect, respectively. It shows an effective noise-shaping structure. As it is seen, the SNDR is reduced about 0.5 dB because of circuit noise effect. Utilizing optimized NTF, this work achieves 13.5 bit ENOB with OSR = 8. The capacitor mismatch of the CDAC is eliminated in this simulation in order to illustrate and study the effectiveness of the noise-shaping and circuit noise effect in the proposed structure.

The dynamic behavior of the proposed ADC at the worst PVT variation cases with and without the circuit noise effect has been studied with post-layout simulations in Cadence Virtuoso. The simulated results

Table 4
Performance summary of the post-layout simulated NS-SAR ADC in worst-case PVT situations.

Parameter	FF @ −40 °C V_{DD} = 1.2 V	FS @ 27 °C V_{DD} = 1.1 V	TT @ 27 °C V_{DD} = 1.1 V	SF @ 27 °C V_{DD} = 1.1 V	SS @ 85 °C V_{DD} = 1 V
SNDR (w/o circuit noise effect)	84.44 dB	82.86 dB	83.6 dB	80.1 dB	82.26 dB
ENOB (w/o circuit noise effect)	13.73 bit	13.47 bit	13.6 bit	13.01 bit	13.37 bit
SNDR (with circuit noise effect)	83.6 dB	82.54 dB	83.1 dB	80 dB	82.1 dB
ENOB (with circuit noise effect)	13.6 bit	13.41 bit	13.5 bit	13.00 bit	13.34 bit
Power	110 μW	71.6 μW	70.3 μW	60.5 μW	48.5 μW
Sampling rate	2.5 MHz				
Signal bandwidth	156.25 kHz				
OSR	8				
Input signal frequency	17.08984375 kHz				

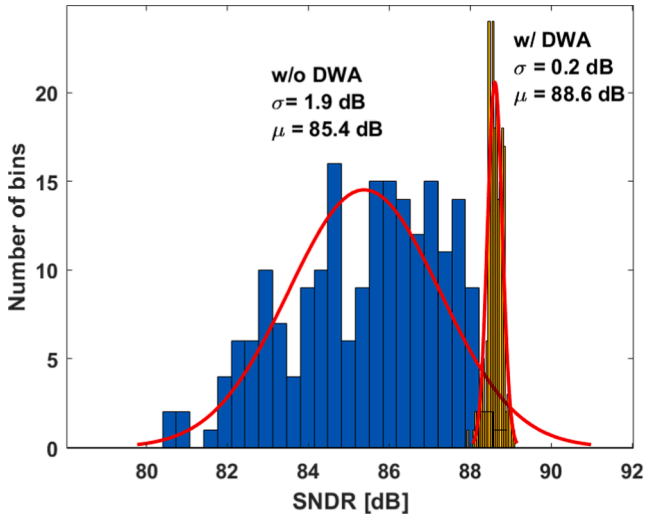

Fig. 12. SNDR Monte Carlo simulation result with and without the DWA method in MATLAB.

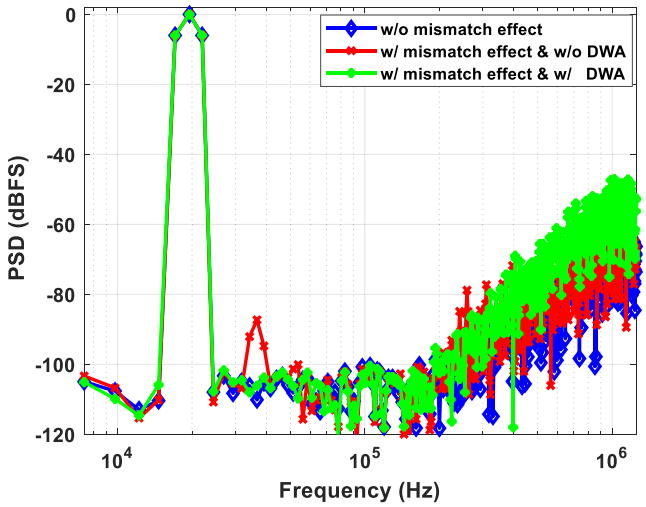

Fig. 13. Simulated output spectrum of the proposed ADC with and without the mismatch and DWA method in MATLAB.

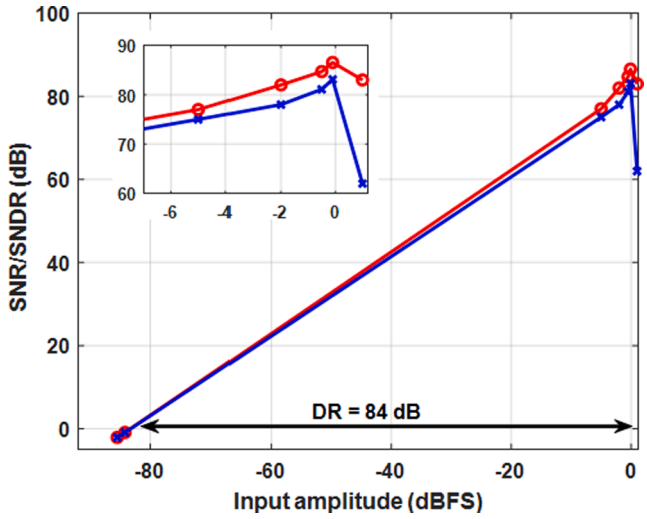

Fig. 14. Post-layout simulated SNR and SNDR versus the input signal amplitude of the proposed NS-SAR ADC (TT @ 27 °C; V_{DD} = 1.1 V).

are represented in Table 4. As it is seen, the proposed ADC is PVT robust and is consistent with design goal at different situations.

Taking the capacitor mismatch into account, the inband harmonic distortion arising from the capacitors mismatch is studied by running a Monte Carlo simulation with 200 runs in MATLAB. Owing to very long simulation time which is required for transistor level Monte Carlo simulations, this study is done systematically in MATLAB. To have a CDAC with high linearity and low mismatch, the size of the DAC capacitors can be chosen large enough, but it results in large area and enhanced switching energy consumption in the SAR ADC. Besides, several calibration methods can be utilized to alleviate the DAC capacitors mismatch in SAR ADCs [39,43,44]. Nonetheless, the digital background calibration techniques needs more power consumption and increases the design complexity. To avoid from more power consumption and complicated calibration scheme, in this work, we used the data weighted averaging (DWA) algorithm to decrease the inband distortions [45]. This method is a popular scheme to reduce the DAC mismatch effect in oversampling structures like sigma-delta and NS-SAR ADCs. We considered the capacitor mismatch of 0.5% [36] and an overall circuit noise voltage of 51 μVrms, OSR = 8, f_s = 2.5 MHz, BW = 156.25 kHz, f_{in} = 17.08984375 kHz, N_{FFT} = 1024, and 200 samples in this simulation. The Monte Carlo simulation result of SNDR is shown in Fig. 12. As it is seen, using the DWA algorithm, the average SNDR is increased from 85.4 dB to 88.6 dB. Also the standard deviation of the SNDR is reduced from 1.9 dB to 0.2 dB. Fig. 13 shows the ADC output spectrum with and without mismatch and DWA algorithm. As it is illustrated, by using the DWA technique, the amplitude of inband harmonic distortions is reduced and they are shaped to higher frequencies.

By considering the circuit noise voltage of 51 μVrms, the post-layout simulation results of signal-to-noise ratio (SNR) and SNDR versus the input signal amplitude are depicted in Fig. 14. Here the simulation conditions are the same as Fig. 11. As it is shown, the dynamic-range (DR) of the proposed NS-SAR ADC is about 84 dB.

A performance summary and a comparison over several recent NS-SAR ADCs are reported in Table 5. This work does not use the closed-loop amplifier that consumes nearly high power. Instead of that, we use a FIDA to implement an outstanding optimized NTF without needing any complicated calibration scheme for amplifier gain like [8]. The proposed structure remains PVT robust via one-time tuning FIDA capacitor to compensate PVT effects. Moreover, compared with the passive NS-SAR ADCs in [10,11], this work employs a passive gain of 4 by stacking the integration capacitors based on [18], which decreases the comparator input-referred noise considerably since a comparator with multi-input pairs is not needed. Also, it does not add noticeable kT/

Table 5
Performance comparison of the proposed third-order NS-SAR ADC with some similar works.

Reference	Architecture	Gain type	NTF order	Technology (nm)	Optimized NTF Zeros	No. of Comparator input pairs	Supply (V)	Sampling rate (MHz)	Bandwidth (kHz)	OSR	Power (μW)	SNDR (dB)	FOM_S (dB)
AEUE 2015* [3]	EF	OTA	1	90	NO	1	0.5	1.6	50	16	4.4	59.6	160.1
ESSCIRC 2016 [4]	CIFF	MIC	1	130	NO	2	1.2	2	125	8	61	74	167
CICC 2017 [7]	CIFF	DA & MIC	3	65	NO	3	1	10	250	20	257.8	83.4	173.3
JSSC 2018 [8]	EF	DA	2	40	YES	1	1.1	10	625	8	84	79	178
TVLSI 2018* [9]	CIFF	MIC & CS	1	65	NO	2	1	100	2000	25	561	82	176.8
JSSC 2019 [11]	CIFF	MIC	2	40	NO	3	1.1	8.4	262	16	143	78.4	171
TCAS-II 2020 [15]	CIFF	DA	2	65	NO	3	1.2	100	3125	16	1240	77	171
MEJ 2020* [16]	EF	DA	2	130	YES	1	1.2	1	62.5	8	96	76.95	165
TCAS-I 2020 [12]	EF	DA	2	65	YES	1	1	10	(N − 1 ~ N)* 625	8	70	71.9–74.6	171.4~ 174
JSSC 2020 [14]	CIFF	DA &CS	2	40	NO	1	1.1	10	625	8	107	83.8	181.5
TVLSI 2020* [13]	CIFF	MIC	2	130	NO	2	1.2	2	125	8	59.9	78.69	171.9
JSSC 2021 [19]	EF-CIFF	DA	3	65	YES	2	1.1	10	625	8	119	84.8	182
CICC 2021 [17]	EF-CIFF	OTA & MIC	3	130	YES	2	1.2	2	125	8	96	79.57	170.7
TCAS-I 2021 [23]	CIFF	MIC	2	65	YES	3	0.9/ 2.1	80	2000	20	2130	73.8	163.5
JSSC 2021 [33]	TI- CIFF	MIC	3	40	YES	3	1.1	400	33,300	6	8500	73.7	169.6
JSSC 2021 [18]	MES& CIFF	CS	1	40	NO	1	1.1	2	40	25	67.4	90.5	178.2
JSSC 2022 [21]	1–1 MASH	MIC & VCO	2	65	YES	2	1.1	24	1100	11	160	71.5	169.9
TCAS-II 2022 [24]	EF	CS	2	65	YES	1	1.2	20	625	16	113.02	79.3	176.73
This work*	EF-CIFF	DA & CS	3	180	YES	1	1.1	2.5	156.25	8	70.3	83.1	176.57

FOM_S = SNDR + 10 $\log_{10}$ (Bandwidth/Power) * Simulation Results.
MIC = multi-input comparator; DA = Dynamic amplifier; CS = capacitor stacking; MES = Mismatch error shaping.

C noise. The size of integration capacitor is reduced by four times by using the differential integration technique. According to the simulation results from the sample implemented ADC, the achieved Schreier's figure-of-merit (FoM) is 176.57 dB, which is comparable with the current state-of-the-art works as well.

5. Conclusion

This paper presents a robust, simple, and scaling-friendly third-order noise-shaping SAR ADC. A combination of EF and FF techniques is utilized to create an effective third-order NS-SAR ADC with fewer modifications in general SAR ADC. It employs a passive integrator to enhance the inband quantization noise attenuation with low power. The integrator loss is compensated by providing a passive gain of 4 with stacking capacitors. Further, we use a FIDA without needing any PVT calibration and just requiring a one-step manual tuning. The NTF zeros are optimized to more reduce the inband quantization. The obtained SNDR is 83.1 dB leading to Schreier's FoM of 176.57 dB. The proposed ADC is a good candidate for high resolution and low power applications.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

No data was used for the research described in the article.

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