An Energy-Efficient DAC Switching Method for SAR ADCs

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***Abstract*—This brief presents a capacitor switching technique to reduce the power consumption in successive approximation register (SAR) analog-to-digital converters (ADCs). The proposed method ideally does not consume any switching energy in digital-to-analog converter and for a 10-bit ADC; it achieves 87% reduction in the total capacitor area compared to the conventional SAR ADC. In addition, the accuracy of the proposed SAR ADC does not depend on the accuracy of the mid-level reference voltage (V_{cm}). Moreover, the common-mode input voltage of the comparator will remain constant. The proposed ADC is simulated in a 90-nm CMOS technology with sampling rate of 100 kS/s and resolution of 10-bit. The simulation results achieve an 8.5 effective number of bits with about 0.5-μW power consumption resulting in a FoM of 9.76 fJ/conversion-step.**

***Index Terms*—Successive approximation register (SAR) ADCs, charge-redistribution DACs, DAC switching energy.**

I. Introduction

SUCCESSIVE approximation register (SAR) analog-to-digital converters (ADCs) are more often utilized in energy limited applications with moderate sampling rates and resolutions. In charge-redistribution SAR ADCs, the capacitor switching in DAC arrays consumes a considerable part of the total power. Recently, several methods have been proposed to reduce the DAC switching energy and the capacitor size [1]–[6]. In comparison with the conventional scheme, these references reduce the DAC switching energy up to 99.3 percent. But, in [1] and [3]–[6], the large variation of the common-mode voltage in the fully-differential DAC needs a comparator with the rail-to-rail input. In addition, the accuracy of ADC in [1], [3], and [5] highly depends on the precision of the mid-level reference voltage (V_{cm}). Moreover, in most of these methods, the DAC capacitors are binary weighted which is more prone to the mismatch than the unary weighted capacitors.

In this brief, a new switching technique is presented to reduce both the DAC switching energy and total capacitor size by utilizing only the unary weighted capacitors. The inaccuracy of V_{cm} does not affect the ADC precision, and the outputs of differential DAC have a constant common-mode voltage making the realization of the comparator much more relaxed. The power consumption of the DAC array is reduced remarkably at the expense of logic complexity.

This brief is organized as follows. In Section II, the main ideas behind this approach are presented. The proposed capacitor switching technique is described in Section III. The algorithm of DAC switching scheme is provided in Section IV. The circuit level simulation results are presented in Section V, and finally, Section VI concludes this brief.

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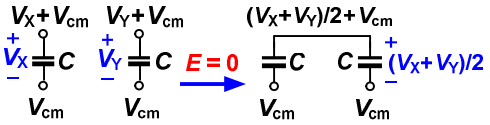

Fig. 1. One of the ideas used in the proposed capacitor switching method.

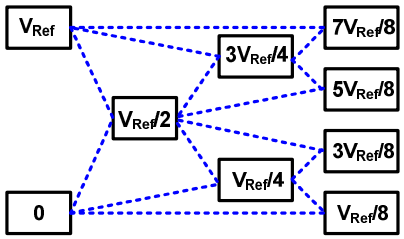

Fig. 2. Generating the threshold voltages in a 3-bit SAR ADC.

II. The Main Ideas

There are two main ideas used in the proposed capacitor switching scheme. Fig. 1 illustrates the first idea. If the top plates of two identical capacitors with different charges ($C\times V_X$ and $C\times V_Y$) are connected together and their bottom plates are remained connected to V_{cm}, any energy will not be drained from V_{cm} during this transition and their final charge will be the average of their previous charges. This is because the energy consumption in this transition can be calculated as:

$$E = V_{cm} \times \Delta Q = V_{cm} \times (\Delta Q_1 + \Delta Q_2) \tag{1}$$

where

$$\Delta Q_1 + \Delta Q_2 = C \times \left[(V_X + V_Y)/2 - V_X\right] + C \times \left[(V_X + V_Y)/2 - V_Y\right] = 0$$

Fig. 2 illustrates the required threshold voltages for a 3-bit SAR ADC. The second idea is that the threshold voltage in each conversion step of the SAR ADC is the average of two threshold voltages which have been generated in the previous steps [7].

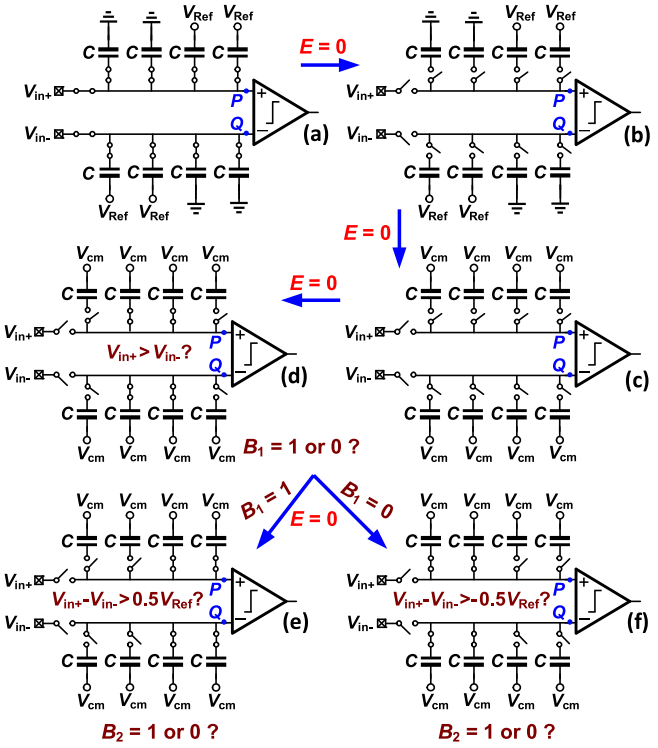

Fig. 3. Proposed DAC switching scheme of 2-bit ADC: (a) sampling step, (b) second step, (c) third step, (d) defining MSB and (e & f) defining the second bit.

III. Proposed Capacitor Switching Technique

In this section, the proposed DAC switching method is firstly explained for a 2-bit SAR ADC, and then it is clarified for an N-bit SAR ADC. Finally, the required number of capacitors for an N-bit SAR ADC is specified.

A. Proposed 2-Bit SAR ADC

Fig. 3 illustrates the proposed DAC switching scheme for an ideal, i.e., zero parasitic capacitor at the input of the comparator, 2-bit SAR ADC. This algorithm is divided into two different phases. The first phase has three steps. In the first step as shown in Fig. 3(a), the differential input is sampled on the top plate of all capacitors while in both DAC arrays, the bottom plate of half of the capacitors is connected to the reference voltage (V_{Ref}) and the other half to the GND. Therefore, in the upper DAC array, at the positive input of the comparator (node P), half of the capacitors have been charged to $V_{\mathrm{in+}}$ and the other half to $V_{\mathrm{in+}} - V_{\mathrm{Ref}}$. Similarly, in the lower DAC array, at the negative input of the comparator (node Q), half of the capacitors have been charged to $V_{\mathrm{in-}}$ and the other half to $V_{\mathrm{in-}} - V_{\mathrm{Ref}}$.

In the next step as shown in Fig. 3(b), all capacitors and the input signal are disconnected from the comparator's inputs. In the last step of the first phase as illustrated in Fig. 3(c), the bottom plates of all capacitors are connected to the common mode voltage (V_{cm}) and remain connected to V_{cm} until the end of the conversion. It should be noted that since there is no path to charge or discharge the capacitors, their charge would not change and any energy will not be consumed in this phase.

The output bits of the SAR ADC are defined in the second phase. As shown in Fig. 3(d), in order to define the first bit, the voltage of node P is $V_P = V_{\mathrm{in+}} - V_{\mathrm{Ref}}/2 + V_{\mathrm{cm}}$ as a result of connecting top plates of one capacitor already charged with $V_{\mathrm{in+}}$ and one capacitor already charged with $V_{\mathrm{in+}} - V_{\mathrm{Ref}}$. The same procedure is performed in node Q by connecting two capacitors already charged with $V_{\mathrm{in-}}$ and $V_{\mathrm{in-}} - V_{\mathrm{Ref}}$, resulting in $V_{\mathrm{Q}} = V_{\mathrm{in-}} - V_{\mathrm{Ref}}/2 + V_{\mathrm{cm}}$. Therefore, $V_{\mathrm{in+}} - V_{\mathrm{in-}}$ is compared with zero and this defines the most significant bit (MSB).

In order to define the second bit, if the first bit is 1, the top plate of one capacitor charged with $V_{\mathrm{in+}} - V_{\mathrm{Ref}}/2$ is connected to that of another capacitor charged with $V_{\mathrm{in+}} - V_{\mathrm{Ref}}$ as shown in Fig. 3(e). Thus, the voltage of $V_P = V_{\mathrm{in+}} - 3V_{\mathrm{Ref}}/4 + V_{\mathrm{cm}}$ is generated in node P. The required voltage of $V_{\mathrm{Q}} = V_{\mathrm{in-}} - V_{\mathrm{Ref}}/4 + V_{\mathrm{cm}}$ at node Q is produced by connecting two capacitors charged with $V_{\mathrm{in-}} - V_{\mathrm{Ref}}/2$ and $V_{\mathrm{in-}}$. Therefore, in this step, $V_{\mathrm{in+}} - V_{\mathrm{in-}}$ is compared with $V_{\mathrm{Ref}}/2$ and this defines the second bit. As illustrated in Fig. 3(f), the exact opposite procedure takes place if the first bit is 0, and therefore, $V_{\mathrm{in+}} - V_{\mathrm{in-}}$ is compared with $-V_{\mathrm{Ref}}/2$. In this phase, since in all steps, the condition of the first main idea is set, so no energy will be drained from V_{cm}.

B. Proposed N-Bit SAR ADC

The first phase is the same for all ADC resolutions. So it exactly has the same three steps as the 2-bit SAR ADC. At the end of this phase in node P, half of the capacitors have been charged to $V_{\mathrm{in+}}$ and the other half to $V_{\mathrm{in+}} - V_{\mathrm{Ref}}$ and in the lower DAC array, in node Q, half of the capacitors have been charged to $V_{\mathrm{in-}}$ and the other half to $V_{\mathrm{in-}} - V_{\mathrm{Ref}}$. The bottom plates of all capacitors are connected to V_{cm} and remain connected to V_{cm} until the end of the conversion in order to meet the conditions of the first main idea. Therefore, there is not any energy consumption from V_{cm} and since there is not any connection to V_{Ref}, any energy is not drained from that too.

In the second phase, in each step, $V_{\mathrm{in+}} - V_{\mathrm{in-}}$ should be compared with the threshold voltage of that step. In order to perform this comparison, in the i-th step by connecting specific capacitors to each other, the voltage of node P can be written as $V_{\mathrm{P}} = V_{\mathrm{in+}} - V_{\mathrm{mp,i}} + V_{\mathrm{cm}}$ and the voltage of node Q can also be written as $V_{\mathrm{Q}} = V_{\mathrm{in-}} - V_{\mathrm{mq,i}} + V_{\mathrm{cm}}$. Therefore $V_{\mathrm{in+}} - V_{in-}$ is compared with $V_{\mathrm{mp,i}} - V_{\mathrm{mq,i}}$. So $V_{\mathrm{mp,i}}$ and $V_{\mathrm{mq,i}}$ should be determined such that $V_{\mathrm{mp,i}} - V_{\mathrm{mq,i}}$ become the threshold voltage of this step ($V_{\mathrm{th,i}}$).

In order to reach the voltage of $V_P = V_{\mathrm{in+}} - V_{\mathrm{mp,i}} + V_{\mathrm{cm}}$ in the ith step, charge of the capacitors which are connected to this node should be $V_{\mathrm{in+}} - V_{\mathrm{mp,i}}$. As mentioned in the second main idea, this required charge is acquired by averaging two groups of capacitors with specific charges. So $V_{\mathrm{in+}} - V_{\mathrm{mp,i}}$ is the average of two groups of capacitors with different charges that the higher charge is $V_{\mathrm{in+}} - V_{\mathrm{lp,i}}$ and the lower charge is $V_{\mathrm{in+}} - V_{\mathrm{hp,i}}$. A similar procedure takes place in node Q by connecting two groups of capacitors with the charge of $V_{\mathrm{in-}} - V_{\mathrm{hq,i}}$ and $V_{\mathrm{in-}} - V_{\mathrm{lq,i}}$ in order to generate the required voltage of $V_{\mathrm{Q}} = V_{\mathrm{in-}} - V_{\mathrm{mq,i}} + V_{\mathrm{cm}}$ in node Q.

Fig. 4 illustrates the flowchart of generating the threshold voltage to define the $(i+1)$-th bit according to the threshold voltage of the ith bit. In fact, the voltages of $V_{\mathrm{lp,i+1}}$, $V_{\mathrm{hp,i+1}}$, $V_{\mathrm{lq,i+1}}$ and $V_{\mathrm{hq,i+1}}$ are defined according to their previous amounts and the output of the comparator in the ith step, in order to determine the threshold voltage of the $(i+1)$-th step.

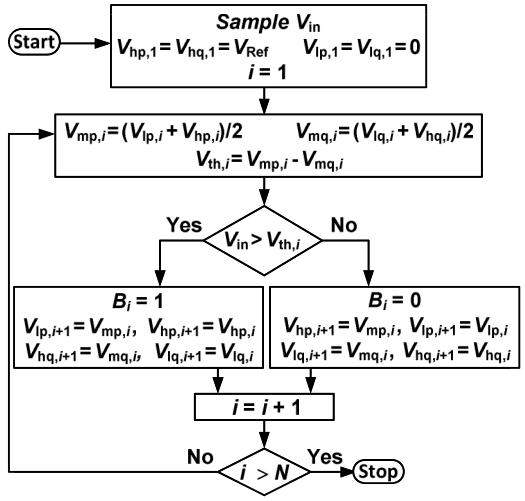

Fig. 4. Flowchart of the proposed SAR ADC.

C. Number of Required Capacitors for an N-Bit SAR ADC

In the proposed DAC switching scheme, the number of required capacitors is determined by relation (2). If the number of required capacitors for an N-bit DAC in each capacitor array is $f(N)$, then the number of required capacitors for an $(N+1)$-bit DAC in each capacitor array, $f(N+1)$, is obtained as:

$$f(N+1)=3\times\frac{f(N)}{2},\quad \text{if } \frac{f(N)}{2} \text{ is even}$$
$$f(N+1)=3\times\frac{f(N)}{2}+1,\quad \text{if } \frac{f(N)}{2} \text{ is odd} \tag{2}$$

where $f(N)=2$ for $N=1$.

For example, based on this relation, the required number of capacitors for a 2-bit SAR ADC is 4 at each capacitor array.

Finally the number of capacitors that should be connected to each other in order to define the ith bit in an N-bit SAR ADC is determined. If in node P, $K_{\rm i}$ capacitors with the charge of $V_{\rm in+}-V_{\rm hp,i}$ are connected to $K_{\rm i}$ capacitors with the charge of $V_{\rm in+}-V_{\rm lp,i}$, therefore $2K_{\rm i}$ capacitors with the charge of $V_{\rm in+}-V_{\rm mp,i}$ are generated. $K_{\rm i}$ is calculated from the following relation:

$$K_{\rm i}=\begin{cases}\frac{1}{2}\times\left(\frac{f(N-i)}{2}\right) & \text{if } \frac{f(N-i)}{2} \text{ is even}\\ \frac{1}{2}\times\left(\frac{f(N-i)}{2}+1\right) & \text{if } \frac{f(N-i)}{2} \text{ is odd}\\ 1 & \text{if } i=N\end{cases} \tag{3}$$

For example, in a 2-bit SAR ADC, for the first bit ($i=1$) according to relation (3), K_1 is 1 and as presented in Fig. 3(d), two capacitors are connected to each other at each input of the comparator.

D. Comparison of Switching Schemes

In Table I, the main features of the proposed switching scheme and several recently reported methods are compared. From mathematical calculations and neglecting the parasitic capacitors at the comparator's inputs, the average switching energy of the proposed method is zero. It means that after the sampling step, no more energy is drained from $V_{\rm cm}$ during the DAC switching period based on the first main idea. Since all of the capacitors are disconnected from $V_{\rm Ref}$, there is not any energy draining from that either. But, the unequal parasitic capacitors at the comparator's inputs may affect the precision of the ADC and also results in a non-zero DAC switching energy. Nonetheless, in each conversion step, the voltage changes at nodes P and Q are equal but in an opposite direction. So, the total energy drained from $V_{\rm cm}$ through the parasitic capacitors at the nodes P and Q will be zero provided that the circuit is fully symmetric. Otherwise, the switching energy due to these parasitic capacitors is not zero, but it is very smaller than the DAC switching energy in all energy efficient schemes reported yet.

TABLE I
COMPARISON OF SEVERAL SWITCHING TECHNIQUES FOR 10-BIT SAR ADC

Switching scheme	Ave. switching energy ($CV^2_{\rm Ref}$)	Energy saving	Area reduction	Logic complexity	Parasitic Sensitivity	Sensitivity to the accuracy of $V_{\rm cm}$
Tri-level [1]	42.4	96.89%	75%	Medium	Low	Very high (all bits except MSB)
[2]	85.05	93.7%	75%	Low	Low	Very low (only LSB)
[3]	15.88	98.83%	75%	Low	Low	Very high (all bits except MSB)
[4]	31.87	97.66%	50%	Low	Low	No
[5]	15.8	97.4%	75.5%	Low	Low	Very high (all bits from the third bit)
[6]	10.2	99.3%	71.9%	Medium	Low	Very low (only LSB)
This work	0	100%	87%	High	Low	No

In the proposed technique, unary weighted capacitors are used in the DAC arrays making the design more robust to the systematic mismatch. Furthermore, the process of averaging which is used to generate the output voltage in each step leads to the reduction of the effective standard deviation of the capacitor mismatch based on the following relation [7]:

$$\sigma_{CT}=\sigma_{Cu}/\sqrt{C_T/C_u} \tag{4}$$

where C_u is the unit capacitor with the standard deviation of $\sigma_{\rm Cu}$ and C_T is the total capacitance shared in each comparison with a standard deviation of σ_{CT}. The results of a behavioral Monte Carlo simulation with 3 $\sigma_{Cu}=0.01C_u$ show the average and standard deviation of SNDR about 61.8 dB and 0.15 dB, respectively. The mismatch amount of capacitors is considered according to the 90 nm TSMC models for MIM capacitors.

The other advantage of the proposed method is that for each extra ADC bit, the required size of capacitors approximately increases by 50% especially beyond 5-bit, while in [1]–[6], this ratio is 100%. Although the total number of capacitors and switches are more than other schemes with binary weighted capacitors, all capacitors and switches are the same size, and hence, for a 10-bit ADC, the required total size of capacitors is reduced about 87% compared to the conventional SAR ADC.

In the proposed switching scheme, since in all steps exactly opposite procedures take place in nodes P and Q, this method is a monotonic approach and the outputs of differential DAC since the $V_{\rm cm}$ appears as a common-mode term between the upper and lower DAC capacitor arrays, the proposed scheme does not have any dependency on the accuracy of $V_{\rm cm}$. Also, it

does not draw any current from $V_{\rm cm}$ making the realization of the mid-level reference voltage much more relaxed with less area. The main drawback of the proposed ADC is the increased digital logic complexity since the number of switches that should be turned on each step is different. Also, the utilized top-plate sampling leads to the signal dependent charge injection and to minimize this effect, bootstrapping switches are adopted for sampling the input signal.

Noise analysis in this method is similar to the conventional method. For the sake of simplicity, it is assumed that there is no correlation between the thermal noise sources. Thus, during the sampling phase, the kT/C noise of capacitor array for a 10-bit SAR ADC can be approximated as:

$$V_{n,DAC}^2 \approx kT/124C_u. \tag{5}$$

IV. Algorithm of DAC Switching

It has been discussed in Section III which groups of the capacitors are connected to each other in each step to generate the required voltage in nodes P and Q.

The relation (2) shows that the required number of capacitors for an N-bit SAR ADC in each DAC array is $f(N)$. In each step, the required voltage change in nodes P and Q are exactly the opposite. As shown in Fig. 5, the capacitors are numbered from 1 to $f(N)$ at each input of the comparator. In the sampling phase, the capacitors from 1 to $f(N)/2$ (left side) in node P are connected to GND and the capacitors from $f(N)/2+1$ to $f(N)$ (right side) are connected to $V_{\rm Ref}$. Conversely, in node Q, the capacitors from 1 to $f(N)/2$ (left side) are connected to $V_{\rm Ref}$ and the capacitors from $f(N)/2+1$ to $f(N)$ (right side) are connected to GND. Therefore, the controller of the capacitors 1 to $f(N)$ in both inputs are exactly the same. The similar arrangement is applied to the capacitors for a 2-bit ADC in Fig. 3. Therefore, the control signals for the capacitors 1 to 4 is the same in both inputs of the comparator.

The next step is to determine the required switches to be turned on in each step. The switches that should be turned on in the first step are determined according to the main algorithm. There are $f(N)$ switches in each input of the comparator for an N-bit SAR ADC. From relation (3), $2K_1$ switches should be turned on in the first step. If these switches are numbered from m_1 to n_1, m_1 and n_1 are determined as:

$$\begin{aligned} m_1 &= f(N)/2 - K_1 + 1 \\ n_1 &= f(N)/2 + K_1 \end{aligned} \tag{6}$$

After the first step, in each step, the switches that should be turned on slide toward one side of the previous group of on switches based on the output of the comparator. If the output of the comparator is 0, it slides to the left side toward the lower threshold voltages in node P and higher threshold voltages in node Q. Therefore, the overall threshold voltage is reduced. Conversely, if the output of the comparator is 1, it slides to the right side toward the higher threshold voltages in node P and lower threshold voltages in node Q. Thus, the overall threshold voltage is increased. Based on relation (3), in the ith step, $2K_{\rm i}$ switches are turned on and these switches are numbered from $m_{\rm i}$ to $n_{\rm i}$, where $n_{\rm i}$ is $m_{\rm i}+2K_{\rm i}-1$ in the arrangement of Fig. 5. The switches that should be turned on in the next step are defined with respect to the output of the comparator in the ith step. Therefore, if the switches that should be turned on in $(i+1)$-th step are numbered from $m_{\rm i+1}$ to $n_{\rm i+1}$, based on the output of the comparator, $m_{\rm i+1}$ and $n_{\rm i+1}$ are defined as

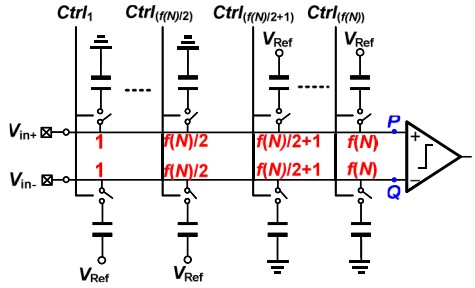

Fig. 5. Proposed arrangement of the capacitors in an N-bit SAR ADC.

relation (7) where $B_{\rm i}$ is the output of the comparator in the ith step.

$$if\ B_i = 0 \Rightarrow \begin{cases} m_{i+1} = m_i - K_{i+1} \\ n_{i+1} = m_i + K_{i+1} - 1 \end{cases} \tag{7}$$

$$if\ B_i = 1 \Rightarrow \begin{cases} m_{i+1} = n_i - K_{i+1} + 1 \\ n_{i+1} = n_i + K_{i+1} \end{cases} \tag{8}$$

Fig. 6 attempts to illustrate the algorithm for a 4-bit SAR ADC. Based on relation (2), in a 4-bit SAR ADC, 10 capacitors are required at each input of the comparator. The first row shows these 10 capacitors in node P at the sampling phase. Half of these capacitors are charged to $V_{\rm in+}$ and the other half are charged to $V_{\rm in+}-V_{\rm Ref}$. In the first step, based on relation (6), the switches from 4 to 7 turn on, and therefore, these capacitors are connected to each other and their charge will be the average of their initial charges. After this step, according to the output of the comparator, the next group of capacitors that should be connected to each other will be specified according to the relation (7). For example, in the second step, if the output of the comparator is 0, capacitors 3 and 4 are connected to each other and if the output of the comparator is 1, capacitors 7 and 8 are connected to each other. In each row, according to the output of the comparator, just one of these connections take place and the charge of rest of the capacitors would not change.

It should be noted that the connection of a specific group of capacitors in each step may lead to different results based on their previous charges. For example, capacitors 3 and 4 in the last step of Fig. 6 may be connected to each other in two different conditions and their final charge is different in these situations based on their previous charges.

V. Circuit Level Simulation Results

To evaluate the efficiency of the proposed SAR ADC, a 10-bit ADC with 100 kHz sampling rate has been realized in circuit level using a 90 nm CMOS process and simulation results are reported here. The comparator circuit reported in [8] is utilized here and it is optimized for low power consumption. To measure the dynamic performance of the simulated ADC, a 6.8109 kHz sinusoidal input signal is applied. Fig. 7 shows the output power spectrum of the simulated ADC for a full-scale input signal. As it is seen, the achieved SNDR is about 52.84 dB corresponding to about 8.5 effective number of bits (ENOBs). The circuit nonlinearities especially the switches charge injection make some harmonics at the ADC output spectrum. This method is sensitive to the signal dependent charge injection like all other top-plate sampling methods. It can also be sensitive to the charge sharing from the switches on the bottom plate.

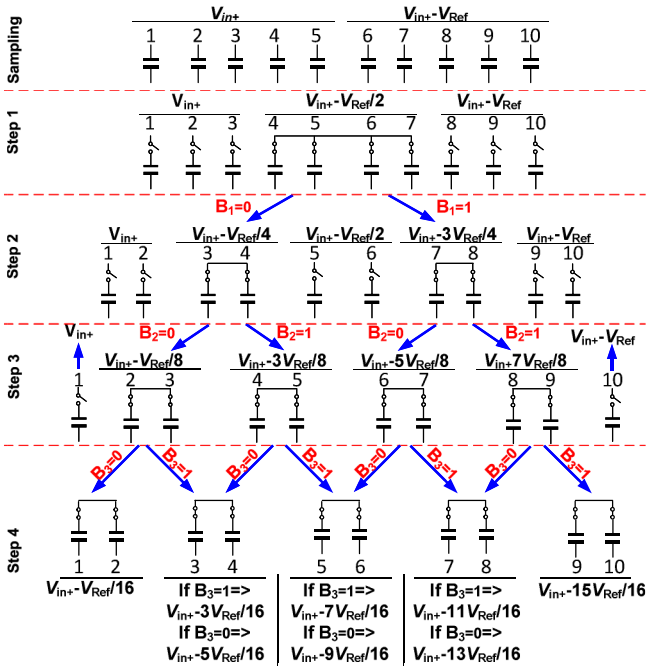

Fig. 6. Proposed DAC switching algorithm.

TABLE II
POWER BREAKDOWN OF THE SIMULATED SAR ADC

	DAC array	Comparator	Logic unit
Power consumption (nW)	81.3	73.1	356.6
Ratio to total power consumption	16%	14%	70%

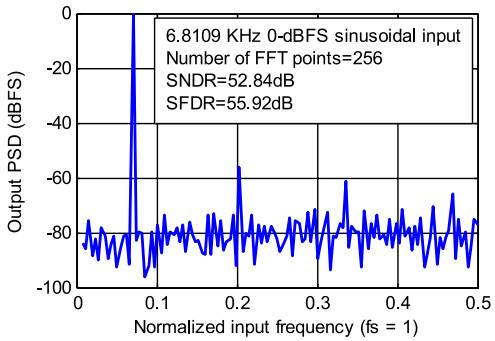

Fig. 7. Simulated output PSD of the proposed 10-bit SAR ADC.

Table II presents the power consumption of different parts of the simulated ADC. As it is seen, the logic unit consumes most of the power in this design, while the DAC array is responsible for most of the power consumption in conventional SAR ADCs. So, as theoretically expected, the DAC switching power is significantly reduced by the proposed algorithm.

The circuit level simulation results of the proposed 10-bit ADC are summarized in Table III along with several implemented SAR ADCs. In this Table, the simulation results of the proposed ADC are compared with the measured results of the others. Although this is not fair comparison, the achieved outstanding FoM verifies the usefulness of the proposed DAC switching scheme in SAR ADCs.

TABLE III
COMPARISON OF SEVERAL IMPLEMENTATIONS

Switching scheme	Technology	ENOB/ Resolution	Supply voltage	Power consumption	Sampling rate	FoM* (fJ/conv.)
[7]	90 nm	4.5/8	0.7 V	700 nW	100 KHz	310
[9]	0.13 um	8.8/10	1 V	15.6 uW	1.1 MHz	31.8
[10]	28 nm	9.42/10	1V	11.7 uW	--	41.2
[11]	65 nm	9.2/10	0.6 V	1.1 nW	1.1 kHz	1.7
[12]	0.11 um	9.1/10	1 V	100 nW	20 kHz	9.1
[13]	0.13 um	11/13	0.5 V	1.47 uW	40 kHz	17.9
This work**	90 nm	8.5/10	1 V	500 nW	100 kHz	9.76

* FoM = POWER /(2^{ENOB}×SAMPLING RATE)
** Simulation results

VI. CONCLUSION

In this brief, an energy efficient DAC switching method for SAR ADCs is proposed. This method does not consume any energy after the sampling phase and reduces the total required area of capacitors by about 87% for a 10-bit SAR ADC in comparison with the conventional method. Circuit level simulation results in the context of 10-bit 100 kHz sampling rate ADC are provided to verify the usefulness of the proposed method. According to these results, the capacitive DAC consumes much lower power than the logic circuit.

REFERENCES

[1] C. Yuan and Y. Lam, "Low-energy and area-efficient tri-level switching scheme for SAR ADC," *Electron. Lett.*, vol. 48, no. 9, pp. 482–483, Apr. 2012.
[2] E. Rahimi and M. Yavari, "Energy-efficient high-accuracy switching method for SAR ADCs," *Electron. Lett.*, vol. 50, no. 7, pp. 499–501, Mar. 2014.
[3] L. Xie, G. Wen, J. Liu, and Y. Wang, "Energy-efficient hybrid capacitor switching scheme for SAR ADC," *Electron. Lett.*, vol. 50, no. 1, pp. 22–23, Jan. 2014.
[4] B. Yazdani, A. Khorami, and M. Sharifkhani, "Low-power DAC with charge redistribution sampling method for SAR ADCs," *Electron. Lett.*, vol. 52, no. 3, pp. 187–188, Feb. 2016.
[5] X. Tong and M. Ghovanloo, "Energy-efficient switching scheme in SAR ADC for biomedical electronics," *Electron. Lett.*, vol. 51, no. 9, pp. 676–678, Apr. 2015.
[6] D. Li, Q. Meng, and F. Li, "Improved dual-capacitive arrays DAC architecture for SAR ADC," *Electron. Lett.*, vol. 52, no. 12, pp. 1013–1015, Jun. 2016.
[7] F. Chen, A. P. Chandrakasan, and V. Stojanovic, "A low-power area-efficient switching scheme for charge-sharing DACs in SAR ADCs," in *Proc. IEEE CICC*, San Jose, CA, USA, Sep. 2010, pp. 1–4.
[8] J. Craninckx and G. van der Plas, "A 65fJ/conversion-step 0-to-50MS/s 0-to-0.7mW 9b charge-sharing SAR ADC in 90nm digital CMOS," in *ISSCC Dig. Tech. Papers*, San Francisco, CA, USA, Feb. 2007, pp. 246–247.
[9] L. Sun, B. Li, A. K. Y. Wong, W. T. Ng, and K. P. Pun, "A charge recycling SAR ADC with a LSB-down switching scheme," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 62, no. 2, pp. 356–365, Feb. 2015.
[10] L. Fick, D. Fick, M. Alioto, D. Blaauw, and D. Sylvester, "A 346 µm 2 VCO-based, reference-free, self-timed sensor interface for cubic-millimeter sensor nodes in 28 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 49, no. 11, pp. 2462–2473, Nov. 2014.
[11] P. Harpe, H. Gao, R. van Dommele, E. Cantatore, and A. H. M. van Roermund, "A 0.20 mm^2 3 nW signal acquisition IC for miniature sensor nodes in 65 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 51, no. 1, pp. 240–248, Jan. 2016.
[12] H. Lee, S. Park, C. Lim, and C. Kim, "A 100-nW 9.1-ENOB 20-kS/s SAR ADC for portable pulse oximeter," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 62, no. 4, pp. 357–361, Apr. 2015.
[13] H. Ha, S.-K. Lee, B. Kim, H.-J. Park, and J.-Y. Sim, "A 0.5-V, 1.47-40-kS/s 13-bit SAR ADC with capacitor error compensation," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 61, no. 11, pp. 840–844, Nov. 2014.