An Accurate Analysis of Slew Rate for Two-Stage CMOS Opamps

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***Abstract*—This brief presents a time-domain model for the slew rate of CMOS two-stage Miller compensated operational transconductance amplifiers. The effects of both the first- and second-stage currents are considered in this model and a simple analytical expression is given in terms of the compensation and load capacitors, output voltage change, and device sizes. HSPICE simulation results are provided to show the validity of the proposed model using a 0.25-μm CMOS technology.**

***Index Terms*—Linear settling, operational transconductance amplifiers (OTAs), slew rate, switched-capacitor circuits.**

I. Introduction

RECENTLY, design of high-speed and low-power OTAs is becoming more challenging due to technology feature size scaling and the power supply voltage reduction. To design low-power and fast settling OTAs, it is needed to model some of their parameters such as the slew rate accurately with simple relations. Changing of OTAs output voltage occurs in two different manners called the linear settling and nonlinear settling or selwing in switched-capacitor circuits. Linear settling depends on the OTAs unity gain bandwidth while the slewing behavior is determined by a parameter called the slew rate. Slewing occurs when one of the input signals is much larger than the other. During this period, one of the differential input transistors is cut off. So, the total settling time is made up of two distinct regions: a slewing period ($t_{\rm SL}$) and a settling period ($t_{\rm ST}$) [1]–[3]. During slewing period, the OTA also behaves as a nonlinear device, forcing its output to follow the input.

Slewing of an OTA is a large-signal characteristic; therefore, a small-signal analysis in the s-domain cannot be used [1]. A time-domain slew rate analysis for a two-stage opamp shown in Fig. 1 has been reported in [1] and the following results have been obtained for positive and negative slew rates $\rm SR^+$ and $\rm SR^-$, respectively

$$\mathrm{SR}^+ = \frac{\frac{I_1}{C_C}}{1+2\frac{a_1(a_1-b_1)}{\Delta V(a_1+b_1)}} \tag{1}$$

$$\mathrm{SR}^- = \frac{-\frac{I_1}{C_C}}{1+2\frac{a_2(a_2-b_2)}{\Delta V(a_2+b_2)}} \tag{2}$$

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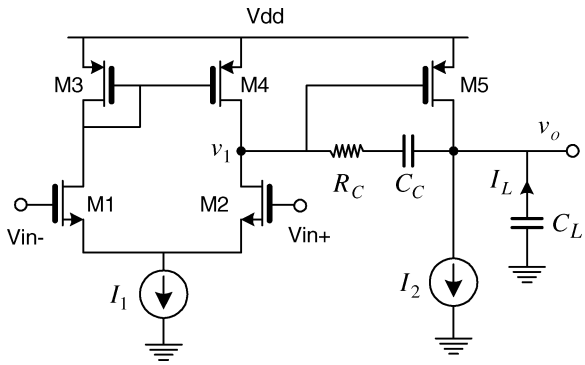

Fig. 1. Single-ended CMOS two-stage OTA with nMOS input pair.

where

$$a_1 = \sqrt{\frac{2\left(I_2 + I_1\left(1+\frac{C_L}{C_C}\right)\right)}{\beta_{p5}}}$$

$$a_2 = \sqrt{\frac{2\left(I_2 - I_1\left(1+\frac{C_L}{C_C}\right)\right)}{\beta_{p5}}}$$

$$b_1 = \sqrt{\frac{2I_2}{\beta_{p5}}} + I_1 R_C$$

$$b_2 = \sqrt{\frac{2I_2}{\beta_{p5}}} - I_1 R_C$$

$$\beta_{pi} = \mu_p C_{OX}\left(\frac{W}{L}\right)_i, \qquad i = 4,5$$

and ΔV is the output voltage change during slewing period.

It is worth to mentioning that this architecture has been chosen for its simplicity and the results can be extended to the other two-stage Miller compensated structures without much effort and also for pMOS input pair [1]. Although this model shows good agreement with simulation results, but it can only be used when

$$I_2 > \frac{C_C + C_L}{C_C} I_1. \tag{3}$$

Because, it is needed to ensure that a_2 is real, and so the slew rate. So, this model predicts the positive slew rate of nMOS input pair two-stage Miller compensated OTAs very well and it fails to predict the negative slew rate when relation (3) is not satisfied. It is worth mentioning that the current of the second

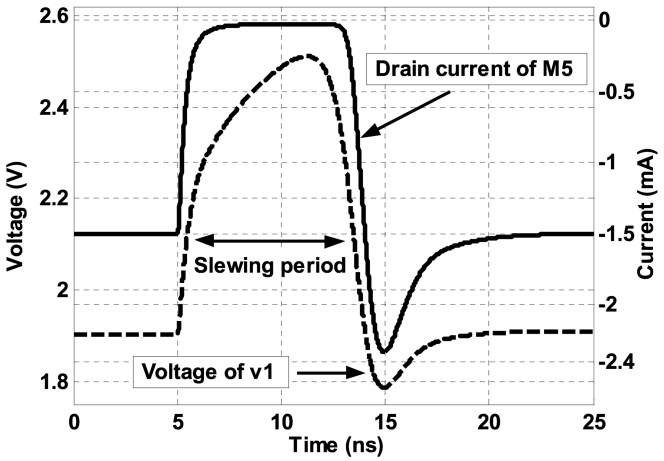

Fig. 2. Drain–source current of M5 and drain voltage of M4 during negative slewing period of Fig. 1.

stage, I_2, cannot be chosen very large due to the power constrains since capacitance load in many switched-capacitor circuits is very large. It is power efficient that the slew rate is limited to the second stage current instead of the first stage current in the two-stage opamps with large load capacitances. Therefore, in this brief, a new model is presented to predict the negative slew rate of nMOS input pair and the positive slew rate of pMOS input pair CMOS two-stage Miller compensated OTAs when condition (3) could not be satisfied.

The brief is organized as follows. Section II presents a novel time-domain model to calculate the negative and positive slew rates of nMOS and pMOS input pair two-stage OTAs, respectively. Circuit level simulation results are provided and compared with the proposed model in Section III. Finally, Section IV concludes the brief.

II. Proposed Model

A. Negative Slew Rate of nMOS Input Pair

During negative slewing period of the OTA shown in Fig. 1, Vin experiences a large negative step. If I_2 is not high enough to support both I_1 and $I_{\rm D5}$ during this period, the drain voltage of M4, v_1, increases so as to turn off the transistor M5. This condition is illustrated in Fig. 2. This plot was generated using HSPICE simulation results of the OTA shown in Fig. 1 with circuit parameters of Table I. As drain voltage of M4 increases, the value of source–drain voltage of M4 decreases. Hence, M4 will be forced to operate in the triode region. This is the key point to write the equations needed to obtain the negative slew rate in this brief. When M4 enters the triode region, the current flowing through the compensation capacitance is no longer constant and it will be a function of v_1. So, the large-signal node equations to obtain the negative slew rate of the circuit shown in Fig. 1 will be as follows:

$$\begin{aligned} I_4 &\approx \mu_p C_{OX}\left(\frac{W}{L}\right)_4\left(\left(V_{DD}-V_{G4}-|V_{tp}|\right)V_{SD4}\right) \\ &= \sqrt{2I_1\beta_{p4}}\left(V_{DD}-v_1\right) \end{aligned} \tag{4}$$

$$I_L = -C_L\frac{dv_o}{dt} \tag{5}$$

TABLE I
Circuit Parameters

Parameter	Value (Fig. 1)	Value (Fig. 3)
$(W/L)_{1,2}$	50/0. 5	150/0.5
$(W/L)_{3,4}$	100/1	40/1
$(W/L)_5$	150/0.5	50/0.5
V_{tp}, V_{tn}	-0.585 V	0.536 V
R_C	400 Ω	320 Ω
ΔV	-1 V	1 V
I_1	1 mA	
C_C	5 pF	
C_L	5 pF	
V_{DD}	3 V	
$\mu_p C_{OX}$	62 μA/V^2	
$\mu_n C_{OX}$	192 μA/V^2	

$$I_4 = C_C\frac{d\left(v_1-v_o-I_4R_C\right)}{dt} \tag{6}$$

$$I_2 = I_4 + I_L. \tag{7}$$

The initial condition of v_1 is obtained based on the fact that the transistor M5 is in cutoff and the transistor M4 is in triode at $t=0^+$. Also the voltage of v_1 at $t=0^-$ is obtained through the saturation region relation of M5. So, the initial condition to solve the above-mentioned differential equations is as follows:

$$v_1(0^+) = v_1(0^-) + I_4(0^+)R_C \tag{8}$$

where

$$\begin{aligned} I_4(0^+) &= k_{p4}\left(V_{DD}-v_1(0^+)\right), \qquad k_{p4} = \sqrt{2I_1\beta_{p4}} \\ v_1(0^-) &= V_{DD}-V_{SG5} = V_{DD}-|V_{tp}|-\sqrt{\frac{2I_2}{\beta_{p5}}}. \end{aligned} \tag{9}$$

Replacing the relations (9) into the relation (8), the initial condition of v_1, i.e., $v_1(0^+)$, will be obtained as follows:

$$v_1(0^+) = \frac{V_{DD}-|V_{tp}|-\sqrt{\frac{2I_2}{\beta_{p5}}}+k_{p4}R_CV_{DD}}{1+k_{p4}R_C}. \tag{10}$$

On the other hand, rearranging the differential equations of (4)–(7) results in

$$\alpha_1\frac{dv_1}{dt}+\alpha_2v_1=\alpha_3 \tag{11}$$

where

$$\begin{aligned} \alpha_1 &= C_CC_L\left(1+k_{p4}R_C\right) \\ \alpha_2 &= k_{p4}\left(C_L+C_C\right) \\ \alpha_3 &= k_{p4}\left(C_L+C_C\right)V_{DD}-I_2C_C. \end{aligned}$$

Solving the differential equation (11) with initial condition (10) one can show that the $v_1(t)$ will be as follows:

$$v_1(t) = A\exp\left(-\frac{\alpha_2}{\alpha_1}t\right)+\frac{\alpha_3}{\alpha_2} \tag{12}$$

where

$$A = \frac{I_2C_C}{k_{p4}(C_C+C_L)}-\frac{|V_{tp}|+\sqrt{\frac{2I_2}{\beta_{p5}}}}{1+k_{p4}R_C}.$$

Hence, the output voltage after some manipulations will be as follows:

$$v_o(t) = \gamma_1 t + \gamma_2 \exp\left(-\frac{\alpha_2}{\alpha_1}t\right) + C \tag{13}$$

where

$$\gamma_1 = -\frac{I_2}{C_L + C_C}$$

$$\gamma_2 = \frac{I_2 C_C^2 (1 + R_C k_{p4})}{k_{p4}(C_C + C_L)^2} - \frac{C_C}{C_C + C_L}\left(|V_{tp}| + \sqrt{\frac{2I_2}{\beta_{p5}}}\right)$$

and C is a constant where its value can be determined by the initial condition of the output voltage.

The slew rate of an OTA is obtained by deriving the derivative of its output voltage with respect to time t. However, the output voltage as shown in the (13) is itself a function of time. Therefore, the effective slew rate defined as $\mathrm{SR}^- = (v_o(t_{\mathrm{SL}}) - v_o(0^+))/t_{\mathrm{SL}}$ is a more useful quantity, where t_{SL} is the time that it takes the output voltage to change from its original value to the value when the OTA enters the linear region [1]. So, the negative slew rate can be derived as follows:

$$\mathrm{SR}^- = \gamma_1 + \frac{\gamma_2}{t_{\mathrm{SL}}}\left(\exp\left(-\frac{\alpha_2}{\alpha_1}t_{\mathrm{SL}}\right) - 1\right). \tag{14}$$

However, since $t_{\mathrm{SL}} = \Delta V/\mathrm{SR}^-$, the above relation can be rearranged as follows:

$$\mathrm{SR}^- = -\frac{I_2}{C_C + C_L}\left(1 + \frac{\gamma_2}{\Delta V}\right)^{-1} \tag{15}$$

where the exponential term has been neglected since it is negligible in practical implementations.

Relation (15) shows that the effective negative slew rate in a two-stage OTA with nMOS input transistors is not only a function of I_2, C_L and C_C, but also a function of k_{p4}, R_C, β_{p5}, I_1 through k_{p4}, and the output voltage change, ΔV. The conventional model reported previously in many books and literature for the absolute value of both negative and positive slew rates has been simply as follows [4], [5]:

$$\mathrm{SR} = \min\left(\frac{I_1}{C_C}, \frac{I_2}{C_C + C_L}\right). \tag{16}$$

As seen from relations (15) and (16), the actual slew rate can be smaller or greater than the value predicted by the conventional model, depending on the circuit parameters and bias conditions. When γ_2 is negative, the effective slew rate is smaller than the value determined by (16) since ΔV is negative. Whereas when γ_2 is positive, its value will be greater than that obtained by the conventional model. When γ_2 is zero, the proposed model reduces to the conventional model.

B. Positive Slew Rate of pMOS Input Pair

During positive slewing of a two-stage OTA with pMOS input pair shown in Fig. 3, i.e., when a large positive input signal is applied to the inputs of the OTA, the transistor M2 turns off and all of the current I_1 flows through the transistor M1. During this period if the current of I_2 is not sufficient to satisfy the condition

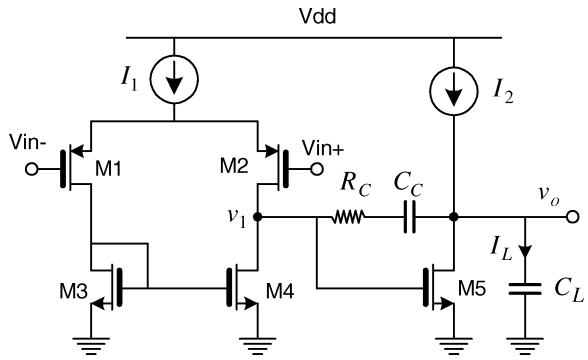

Fig. 3. Single-ended CMOS two-stage OTA with pMOS input pair.

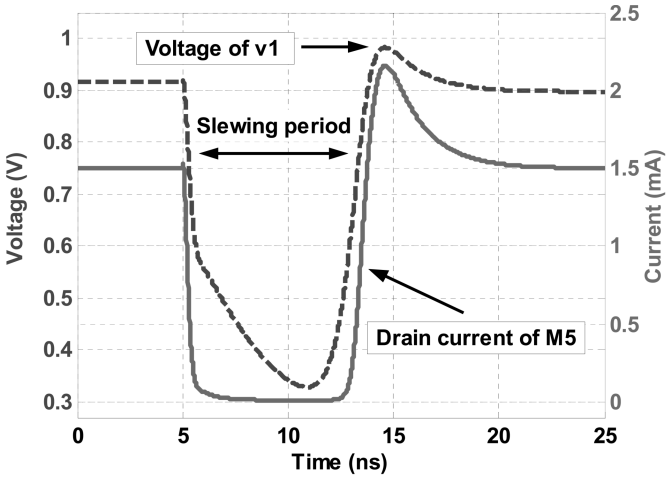

Fig. 4. Drain–source current of M5 and drain voltage of M4 during positive slewing period of Fig. 3.

(3), the drain of M4 is decreased to force the transistor M4 into the triode region. As a result, this turns off M5 as discussed for the nMOS input pair two-stage OTA in the previous subsection and is also shown in Fig. 4.

So, to obtain the positive slew rate, the large-signal equations of the circuit can be written as follows:

$$I_4 \approx \mu_n C_{OX}\left(\frac{W}{L}\right)_4 ((V_{G4} - V_{tn})V_{DS4}) = \sqrt{2I_1\beta_{n4}}\,v_1 \tag{17}$$

$$I_L = C_L\frac{dv_o}{dt} \tag{18}$$

$$I_4 = C_C\frac{d(v_o - v_1 - I_4R_C)}{dt} \tag{19}$$

$$I_2 = I_4 + I_L. \tag{20}$$

The initial condition to solve the differential equations (17)–(20) is as follows:

$$v_1(0^+) = v_1(0^-) - I_4(0^+)R_C \tag{21}$$

where

$$I_4(0^+) = k_{n4}v_1(0^+), \quad k_{n4} = \sqrt{2I_1\beta_{n4}}$$

$$v_1(0^-) = V_{GS5} = V_{tn} + \sqrt{\frac{2I_2}{\beta_{n5}}}. \tag{22}$$

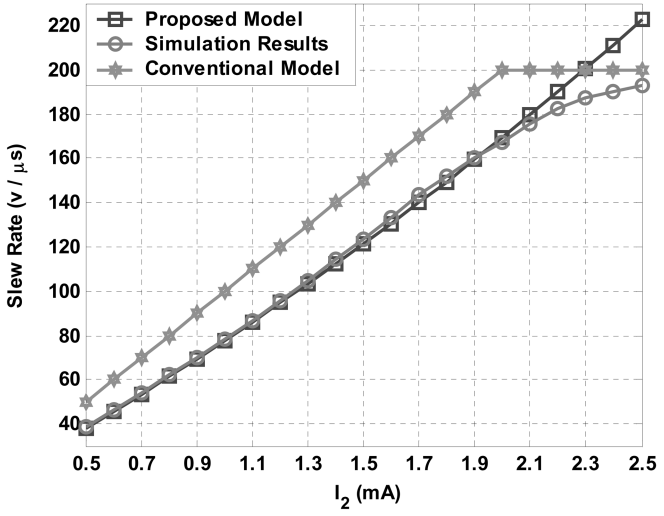

Fig. 5. Negative slew rate versus the current of the second stage of the nMOS input pair two-stage OTA.

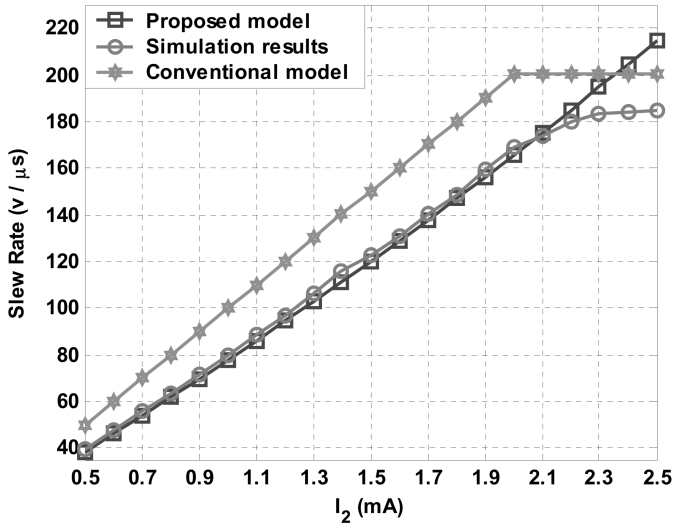

Fig. 6. Positive slew rate versus the current of the second stage of the pMOS input pair two-stage OTA.

So, the initial condition of $v_1(0^+)$ during positive slewing will be obtained as follows:

$$v_1(0^+) = \frac{V_{tn} + \sqrt{\frac{2I_2}{\beta_{n5}}}}{1 + k_{n4}R_C}. \tag{23}$$

Hence, employing the similar approach used for the calculation of the negative slew rate in the previous subsection, the positive slew rate of the pMOS input pair two-stage OTA shown in Fig. 3, when condition (3) is not satisfied, is obtained as follows:

$$\mathrm{SR}^+ = \frac{I_2}{C_C + C_L}\left(1 + \frac{\gamma_3}{\Delta V}\right)^{-1} \tag{24}$$

where

$$\gamma_3 = \frac{C_C}{C_C + C_L}\left(V_{tn} + \sqrt{\frac{2I_2}{\beta_{n5}}}\right) - \frac{I_2 C_C^2 \left(1 + R_C k_{n4}\right)}{k_{n4}\left(C_C + C_L\right)^2}.$$

III. Simulation Results

In order to show the validity of the proposed model for the negative and positive slew rates of CMOS two-stage Miller compensated OTAs with nMOS and pMOS input pairs, respectively, circuit level simulations with HSPICE were performed using a 0.25-μm BSIM3v3 level 49 mixed-signal CMOS models. The OTAs shown in Figs. 1 and 3 were simulated with the design parameters shown in Table I in a unity gain feedback structure. The simulation results confirm the usefulness and validity of the proposed model as shown in Figs. 5 and 6. Here, the absolute value of slew rate is shown. The proposed model has an excellent agreement with simulation results. Also, these results show that the slew rate can be smaller than the value predicted by the conventional model used in many books and literature when condition (3) is not satisfied. The proposed model also has a near perfect agreement with simulation results for a wide range of the circuit parameters. It works very well even when condition (3) starts to be satisfied. But, when the current of the second stage increases, the turn off condition of M5 and also the triode region of M4 during slewing period would no longer occur. So, the proposed models in (15) and (24) starts to deviate from the circuit simulation results as shown in Figs. 5 and 6. For a large current in the second stage, i.e., when condition (3) is satisfied, the negative slew rate of the nMOS input pair OTA can be obtained using relation (2) as proposed in [1]. Also, the positive slew rate of the pMOS input pair OTA when condition (3) is satisfied can be obtained by using relation (1) with replacing the corresponding nMOS circuit parameters with those of the pMOS counterparts. But, choosing a large current for the second stage will not be a power efficient design when a large load capacitor exists.

IV. Conclusion

A novel time-domain analysis of slew rate for CMOS two-stage OTAs was presented in this brief. The previous analytical model suffers from several constraints imposed on the bias currents and device sizes resulting in no power efficient designs for two-stage OTAs used with a large load capacitor. Also, the conventional model used in the literature can have large disagreement with simulation results and the proposed model in this brief depending on the circuit parameters and bias conditions. Simulation results indicate that the proposed model has a perfect agreement with the circuit simulator results such as HSPICE.

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