Journal of Circuits, Systems, and Computers
Vol. 19, No. 7 (2010) 1381–1398

DOI: 10.1142/S0218126610006712

World Scientific
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ACTIVE-FEEDBACK SINGLE MILLER CAPACITOR FREQUENCY COMPENSATION TECHNIQUES FOR THREE-STAGE AMPLIFIERS*

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Received 31 August 2009
Accepted 31 March 2010

This paper presents two novel active-feedback single Miller capacitor frequency compensation techniques for low-power three-stage amplifiers. These techniques include the active-feedback single Miller capacitor frequency compensation (AFSMC) and the dual active-feedback single Miller capacitor frequency compensation (DAFSMC). In the proposed techniques, only one Miller capacitor in series with a current buffer is utilized. The main advantages of the proposed three-stage amplifiers are the enhanced unity-gain bandwidth and the reduced silicon area. Small-signal analyses are performed and the design equations are obtained. Extensive HSPICE simulation results are provided to show the usefulness of the proposed AFSMC and DAFSMC amplifiers in both large and small capacitive loads.

Keywords: Active-feedback; multistage amplifiers; frequency compensation; reversed nested Miller compensation.

1. Introduction

Multistage amplifiers are widely used in the analog and mixed signal circuits to achieve high dc gain and large output signal swing simultaneously, because, although the cascoding of transistors is a well-known means to increase the dc gain of the single-stage amplifiers; however, this is not possible in the recent sub-micron CMOS technologies due to the reduced power supply voltage dictated by the technology scaling. However, multistage amplifiers have additional frequency poles and zeros resulting in inherently instability and reduced signal bandwidth if any frequency compensation technique is not employed.

There are generally two different compensation schemes in the three-stage amplifiers: nested Miller compensation (NMC) and reversed nested Miller compensation

*This paper was recommended by Regional Editor Piero Malcovati.

(RNMC).[1] In three-stage NMC amplifiers, the second stage is non-inverting and the last stage is inverting. This approach employs two compensation capacitors and exploits the Miller effect to split the frequency poles to achieve the desired phase margin and transient response. Nonetheless, this solution results in a gain-bandwidth product of one-quarter that can be achieved by a single-stage amplifier and in a high power consumption.[2] Recently, a few different compensation schemes have been proposed in order to overcome the inherent limits of the NMC amplifiers.[2–9]

An RNMC amplifier usually has a higher bandwidth than the NMC one since in the RNMC amplifier as shown in Fig. 1(a) the inner compensation capacitor is located between the output of the first and second stages and, hence, does not load the amplifier's output.[1] However, the basic RNMC scheme has the stability problem because of appearing a low frequency right half plane (RHP) zero in its frequency response.[10] To alleviate this problem, many RNMC techniques have been reported which are basically canceling the RHP zero such as the RNMC amplifier with a nulling resistor or voltage and/or current followers,[10,11] the reversed active feedback frequency compensation (RAFFC),[12] the RNMC amplifier with voltage buffer and resistor,[13] and single Miller capacitor with a nulling resistor.[14]

In Ref. 6 a three-stage amplifier with a single Miller capacitor compensation (SMC), shown in Fig. 1(b), has been introduced. This technique achieves one left half plane (LHP) zero and another RHP zero and needs a relatively large compensation capacitor especially in the heavily capacitive load applications. In this paper, two

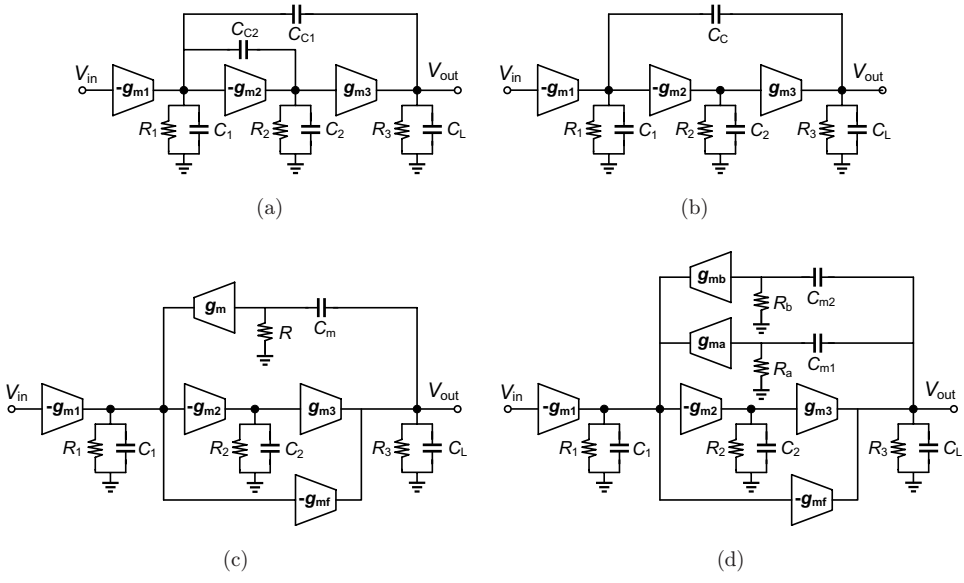


Fig. 1. (a) Conventional RNMC amplifier, (b) SMC amplifier, and the proposed (c) AFSMC and (d) DAFSMC amplifiers.

single Miller capacitor frequency compensation techniques with single and dual active-feedback circuits for three-stage amplifiers are proposed. These techniques are called AFSMC and DAFSMC, respectively. The single Miller capacitor active-feedback topology (AFSMC) has been firstly proposed in Ref. 15 and more developed as DAFSMC in this paper. It should be noted that single Miller capacitor with active feedback topology was more recently utilized in an NMC amplifier in Ref. 16 for small capacitive loads.

The paper is organized as follows. In Sec. 2, the proposed frequency compensation techniques are described and small-signal analyses are performed with both large and small capacitive loads to obtain the design equations. The circuit implementation and the simulation results of the proposed amplifiers are presented in Secs. 3 and 4, respectively. Finally, Sec. 5 concludes the paper.

2. Compensation Techniques

2.1. *Overall structures*

Figures 1(c) and 1(d) shows the basic block diagram of the proposed AFSMC and DAFSMC three-stage amplifiers, respectively, where g_{mi}, C_i, and R_i represent the ith stage transconductance, the equivalent parasitic capacitance, and the output resistance of the corresponding gain stages, respectively. R, R_a and R_b represent the input resistance of the corresponding current buffer stages. C_L includes the load capacitor as well as the output parasitic capacitor of the third stage.

In AFSMC amplifier, a single Miller capacitor, C_m, in series with a current buffer stage, g_m, is placed between the output of the first and third stages of the amplifier whereas in the DAFSMC amplifier, two such active-feedback networks comprising of g_{ma} and g_{mb} current buffer stages and C_{m1} and C_{m2} compensation capacitors are employed.

With an active-feedback frequency compensation scheme that is possible to achieve both high dc gain and large signal bandwidth simultaneously, and reduce the size of the compensation capacitor(s) to save the silicon die area.[3] Moreover, the RHP zero is canceled because the signal feed through the compensation capacitor(s) becomes negligible. In fact, this technique is like the well-known cascode compensation scheme which is widely used in the two-stage amplifiers.

An additional transconductance stage, g_{mf}, is employed between the output of the first and third stages. This forms a push−pull class AB stage at the output node that improves the large-signal transient response by enhancing the slew-rate of the amplifier. Moreover, considering $g_{m3} = g_{mf}$ simplifies the small-signal analysis of the amplifier and is used in the small-signal analysis of the proposed amplifiers.

It is worth mentioning that in the both proposed amplifiers, the RNMC technique is employed since an RNMC amplifier outperforms the NMC one especially in large capacitive loads. Nonetheless, the proposed compensation techniques can also be used in the NMC amplifiers as well.

2.2. *Small-signal analysis*

Figure 2 shows the equivalent small-signal circuit of the proposed three-stage DAFSMC amplifier where the inter stage coupling capacitors are neglected. By writing KCL at nodes A and B we have:

$$\frac{v_a}{R_{\mathrm{A}}} + sC_{m1}(v_a - v_{\mathrm{out}}) = 0 \Longrightarrow v_a = \frac{sC_{m1}v_{\mathrm{out}}}{g_{ma} + sC_{m1}} = v_{\mathrm{out}} \Big/ \left(1 + \frac{g_{ma}}{sC_{m1}}\right), \tag{1}$$

$$\frac{v_b}{R_{\mathrm{B}}} + sC_{m2}(v_b - v_{\mathrm{out}}) = 0 \Longrightarrow v_b = \frac{sC_{m2}v_{\mathrm{out}}}{g_{mb} + sC_{m2}} = v_{\mathrm{out}} \Big/ \left(1 + \frac{g_{mb}}{sC_{m2}}\right), \tag{2}$$

where the input resistance of each current buffer stage was considered equal to the reciprocal of its transconductance, i.e., $R_a = g_{ma}^{-1}, R_b = g_{mb}^{-1}$, and $R = g_m^{-1}$. This assumption is true as is clearly seen in the circuit implementation of the amplifiers. By considering $g_{ma}/C_{m1} = g_{mb}/C_{m2}$ the input voltage of both current buffer stages in the DAFSMC amplifier becomes equal making the compensation capacitors to be paralleled and the transconductance of the current buffer stages to be added. This condition can easily be satisfied by appropriate design of the DAFSMC amplifier as will be shown in the next sections. Therefore, by considering $C_m = C_{m1} + C_{m2}$, $g_m = g_{ma} + g_{mb}$, the small-signal equations of both proposed amplifiers are the same and hence we will consider only one small-signal analysis for both AFSMC and DAFSMC amplifiers.

According to Fig. 2, the small-signal equations of both proposed amplifiers are given by:

$$g_{m1}v_{\mathrm{in}} + \frac{v_1}{R_1} + sC_1v_1 - g_mv_b = 0\,, \tag{3}$$

$$g_{m2}v_1 + \frac{v_2}{R_2} + sC_2v_2 = 0\,, \tag{4}$$

$$-g_{m3}v_2 + \frac{v_{\mathrm{out}}}{R_3} + sC_Lv_{\mathrm{out}} + g_{mf}v_1 + sC_m(v_{\mathrm{out}} - v_b) = 0\,, \tag{5}$$

$$g_mv_b + sC_m(v_b - v_{\mathrm{out}}) = 0\,. \tag{6}$$

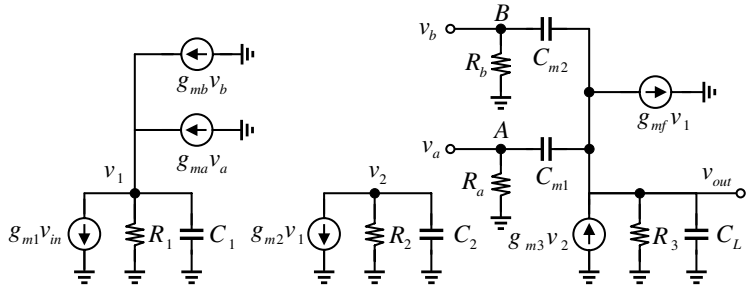


Fig. 2. Equivalent small-signal circuit of the proposed DAFSMC three-stage amplifier.

Therefore, the small-signal transfer function of both proposed amplifiers is obtained as:

$$A_v(s) = \frac{v_{\text{out}}(s)}{v_{\text{in}}(s)} = A_{dc} \times \frac{(1 + b_1 s + b_2 s^2)}{1 + d_1 s + d_2 s^2 + d_3 s^3 + d_4 s^4}\,, \tag{7}$$

where

$$A_{\text{dc}} = g_{m1} R_1 R_3 (g_{mf} + g_{m2} g_{m3} R_2)\,, \tag{8}$$

$$b_1 = \frac{g_m g_{mf} R_2 C_2 + g_{m2} g_{m3} R_2 C_m + g_{mf} C_m}{g_m (g_{m2} g_{m3} R_2 + g_{mf})}\,, \tag{9}$$

$$b_2 = \frac{g_{mf} R_2 C_2 C_m}{g_m (g_{m2} g_{m3} R_2 + g_{mf})}\,, \tag{10}$$

$$d_1 = g_m^{-1} C_m + R_1 C_1 + R_2 C_2 + R_3 [C_L + C_m (1 + g_{m2} g_{m3} R_1 R_2 + g_{mf} R_1)]\,, \tag{11}$$

$$\begin{aligned} d_2 \;=\; & R_1 R_2 C_2 (g_{mf} R_3 C_m + C_1) + g_m^{-1} C_m (R_2 C_2 + R_1 C_1 + R_3 C_L) \\ & + R_3 (C_{\text{L}} + C_m)(R_2 C_2 + R_1 C_1)\,, \end{aligned} \tag{12}$$

$$d_3 = R_1 R_2 C_1 C_2 [g_m^{-1} C_m + R_3 (C_m + C_{\text{L}})] + g_m^{-1} R_3 C_m C_{\text{L}} (R_2 C_2 + R_1 C_1)\,, \tag{13}$$

$$d_4 = g_m^{-1} R_1 R_2 R_3 C_1 C_2 C_m C_L\,. \tag{14}$$

In the following, two different cases in regards of the load capacitor are considered to simplify the small-signal transfer function given in (7) to get a clear insight into the operation of the proposed amplifiers. Moreover, in both cases, it is assumed that the dc gain of all stages is much larger than one, i.e., $g_{m1,2,3} R_{1,2,3} \gg 1$ and $g_m R_{1,2,3} \gg 1$.

2.2.1. *Large load capacitor*

When the load capacitor is very large and we have $C_L \gg C_{m1}, C_{m2} \gg C_i$, the small-signal transfer function given in (7) is simplified as

$$\begin{aligned} A_v(s) &= A_{\text{dc}} \times \frac{(1 + b_1 s + b_2 s^2)}{(1 + s/\omega_{p1})(1 + a_1 s + a_2 s^2 + a_3 s^3)} \\ &= A_{\text{dc}} \times \frac{\left(1 + \dfrac{C_m}{g_m} s + \dfrac{C_m C_2}{g_m g_{m2}} s^2\right)}{(1 + s/\omega_{p1})\left(1 + \dfrac{C_1 C_L}{g_{m2} g_{m3} R_2 C_m} s + \dfrac{C_L C_1 (g_m R_2 C_2 + C_m)}{g_{m2} g_{m3} g_m R_2 C_m} s^2 + \dfrac{C_1 C_2 C_L}{g_{m2} g_{m3} g_m} s^3\right)}, \end{aligned} \tag{15}$$

$$A_{\text{dc}} = g_{m1} g_{m2} g_{m3} R_1 R_2 R_3\,, \quad \omega_{p1} = \frac{1}{g_{m2} g_{m3} R_1 R_2 R_3 C_m}\,, \tag{16}$$

where A_{dc} and ω_{p1} are the dc gain and dominant real pole of the amplifiers, respectively. In relations (15) and (16), it was also assumed that $R_1 C_1 \gg R_2 C_2$ and

$C_m \ll g_m R_1 C_1$. These assumptions can easily be achieved by making the first stage output resistance (R_1) much larger than that of the second stage one. For this reason and also to achieve high dc gain, a cascode structure was utilized in the circuit realization of the first stage amplifier whereas a simple common source topology was employed in the second stage amplifier.

The gain-bandwidth product (ω_{GBW}) of the proposed amplifiers is simply given by:

$$\omega_{\mathrm{GBW}} \approx A_{\mathrm{dc}}\omega_{p1} = \frac{1}{g_{m2}g_{m3}R_1R_2R_3C_m} \times g_{m1}\, g_{m2}\, g_{m3} R_1 R_2 R_3 = \frac{g_{m1}}{C_m}\,. \tag{17}$$

As is seen from relation (15), the proposed amplifiers have two zeros and three non-dominant poles. The zeros are given by:

$$\omega_{z1} = -\frac{g_m}{C_m}\,, \tag{18}$$

$$\omega_{z2} = -\frac{g_{mf} + g_{m2}g_{m3}R_2}{g_{mf}R_2C_2} \approx -\frac{g_{m2}g_{m3}R_2}{g_{mf}C_2R_2} = -\frac{g_{m2}}{C_2}\,, \tag{19}$$

where both zeros are located at the left half plane and, hence, not only the amplifier's stability is not degraded due to the zeros, but also the LHP zeros can lead to an extra phase margin which improves the stability and transient performance of the amplifier provided they are located after the unity-gain frequency in the closed-loop configuration.

To drive the nondominant poles, it is assumed that the third nondominant pole is much larger than the first and second nondominant poles. Therefore, the third nondominant pole of the amplifier is given by:

$$\omega_{p4} \approx -\frac{a_2}{a_3} = -\frac{g_m}{C_m} - \frac{1}{R_2C_2}\,. \tag{20}$$

The first and second nondominant poles are hence given by:

$$\omega_{p2,3} = -\frac{g_m}{2(g_mR_2C_2 + C_m)}\left(1 \pm \sqrt{1 - 4\frac{g_{m2}g_{m3}R_2C_m(g_mR_2C_2 + C_m)}{g_mC_1C_L}}\right)$$

$$\Longrightarrow |\omega_{p2,3}| \approx \sqrt{\frac{g_m g_{m2} g_{m3} R_2 C_m}{C_1 C_L (g_m R_2 C_2 + C_m)}}\,. \tag{21}$$

As is clear the poles splitting have been performed sufficiently and we have $|\omega_{p1}| \ll |\omega_{p2,3}| \ll |\omega_{p4}|$.

The stability analysis of the proposed amplifiers is determined by neglecting the effect of the zeros in the open-loop signal transfer function given in (15) and also the high-frequency nondominant pole, ω_{p4}, and then considering the closed-loop transfer function of the amplifiers in a unity-gain feedback configuration. Therefore, the

closed-loop unity-gain feedback transfer function of the amplifiers is given by:

$$A_{v,\mathrm{cl}}(s) \approx \frac{1}{1 + s\dfrac{1}{\omega_{\mathrm{GBW}}} + s^2\dfrac{a_1}{\omega_{\mathrm{GBW}}} + s^3\dfrac{a_2}{\omega_{\mathrm{GBW}}}} \,. \tag{22}$$

Since the order of the numerator in relation (22) is less than that of its denominator, the stability of the amplifiers is basically determined by the denominator. By applying the Routh−Hurwitz stability criterion as described in Ref. 17 on the characteristic equation (22), the following asymptotic stability condition is obtained:

$$a_1 > a_2\omega_{\mathrm{GBW}} \Longrightarrow \omega_{\mathrm{GBW}} < \frac{g_m}{g_m R_2 C_2 + C_m} \,. \tag{23}$$

As is seen from (23), the ω_{GBW} can be increased by choosing a large transconductance for the current buffer stages. Therefore, the transconductance of the current buffer stages is used as an important design parameter in enhancing the ω_{GBW}. This is one of the main advantages of the active-feedback frequency compensation technique.[3] It should be noted that the transconductance of the current buffer stages can be made larger without considerable increase in the power consumption because the current buffer stages do not need to drive the large load capacitors unlike the output stage. Moreover, as is clear employing two different current buffers in the DAFSMC amplifier doubles the maximum achievable gain-bandwidth product compared to that of the AFSMC one. This extra current buffer stage can be realized without any power dissipation as is seen in the circuit realization of the proposed amplifiers in the next section.

The asymptotic stability condition given in relation (23) also results in the following design constraint:

$$\frac{g_{m1}}{C_m} < \frac{g_m}{g_m R_2 C_2 + C_m} \Longrightarrow g_m > \frac{g_{m1} C_m}{C_m - g_{m1} R_2 C_2} \,. \tag{24}$$

This relation is also simplified if we make $C_m \gg g_{m1} R_2 C_2$ by proper design of the second stage amplifier and hence results in $g_m > g_{m1}$. Therefore, to ensure the stability of the closed-loop amplifier it is sufficient to make the transconductance of current buffers greater than the first stage transconductance.

To avoid any peaking at the frequency response of the proposed amplifiers, a proper value of the damping factor of the second-order polynomial at the denominator of the open-loop transfer function given in relation (15) should be considered.[2] By using a third-order Butterworth response in order to arrange the nondominant poles of the proposed amplifiers similar to that described in Ref. 3 which corresponds to a damping factor of $1/\sqrt{2}$, the following design constraints are obtained:

$$a_1 = \frac{1}{2\omega_{\mathrm{GBW}}} \Longrightarrow C_m = \sqrt{\frac{2 g_{m1} C_1 C_{\mathrm{L}}}{g_{m2} g_{m3} R_2}} \,, \tag{25}$$

$$a_2 = \frac{a_1^2}{2} \Longrightarrow g_m = \frac{4 g_{m1}}{1 - \sqrt{\dfrac{8 g_{m1} g_{m2} g_{m3} C_2^2 R_2^3}{C_1 C_L}}} \approx 4 g_{m1} \,. \tag{26}$$

Table 1. Stability conditions of different multistage amplifiers.

Topology	Stability conditions (Butterworth response)	Max GBW (asymptotic stability condition)
Basic RNMC	$g_{m2}=4g_{m1},\quad C_{C1}=\sqrt{\dfrac{2g_{m1}C_{C2}C_L}{g_{m3}}}$	$\omega_{\rm GBW}=\dfrac{g_{m1}}{C_{C1}}<\dfrac{g_{m2}}{C_{C1}}$
SMC[6]	$C_C=\dfrac{2g_{m1}C_L}{g_{m2}g_{m3}R_2}$	$\omega_{\rm GBW}=\dfrac{g_{m1}}{C_C}<\dfrac{1}{C_2R_2}$
DAFSMC [this work] $C_L\gg C_{m1,2}$	$C_{m1}+C_{m2}=\sqrt{\dfrac{2g_{m1}C_1C_L}{g_{m2}g_{m3}R_2}}$	$\omega_{\rm GBW}=\dfrac{g_{m1}}{C_{m1}+C_{m2}}<\dfrac{g_{ma}+g_{mb}}{(g_{ma}+g_{mb})R_2C_2+(C_{m1}+C_{m2})}$
DAFSMC [this work] Small C_L	$C_{m1}+C_{m2}=\sqrt{\dfrac{2g_{m1}C_1C_L}{g_{m3}}}$ $g_{ma}+g_{mb}=4g_{m1}$	$\omega_{\rm GBW}=\dfrac{g_{m1}}{C_{m1}+C_{m2}}<\dfrac{g_{ma}+g_{mb}}{C_{m1}+C_{m2}}$

According to (25), the size of the compensation capacitors can be very smaller than that of the load capacitor, C_L. This helps us to decrease the value of the compensation capacitors significantly without any stability concern especially in the large capacitive load applications yielding a considerable amount in saving of the silicon area.

Table 1 summarizes the stability conditions and the maximum achievable $\omega_{\rm GBW}$ for the basic RNMC, SMC, and the proposed three-stage amplifiers. As is clear from this table, the proposed AFSMC and DAFSMC amplifiers need the smaller compensation capacitor(s) than the basic RNMC and SMC amplifiers. Although the maximum unity-gain bandwidth of the SMC amplifier can be comparable to that of the proposed ones, however, since the SMC amplifier needs a larger compensation capacitor, its unity-gain bandwidth is very smaller than that of the AFSMC and DAFSMC amplifiers with the same first-stage transconductance, g_{m1}.

2.2.2. *Small load capacitor*

If the load capacitor is not very larger than the compensation capacitor(s), in this case the only assumption can be made to simplify the small-signal transfer function is the large dc gain in stage amplifiers. In this case, it can readily be shown that we have:

$$\begin{aligned} A_v(s) &= \frac{v_{\rm out}(s)}{v_{\rm in}(s)} = A_{\rm dc}\times\frac{(1+b_1s+b_2s^2)}{(1+s/\omega_{p1})(1+a_1s+a_2s^2+a_3s^3)} \\ &= A_{\rm dc}\times\frac{\left(1+\dfrac{C_m}{g_{mb}}s\right)\left(1+\dfrac{C_2}{g_{m2}}s\right)}{\left(1+\dfrac{s}{\omega_{p1}}\right)\left(1+\dfrac{C_2}{g_{m2}}s+\dfrac{C_1C_2C_L}{g_{m2}g_{m3}C_m}s^2+\dfrac{C_1C_2C_L}{g_{m2}g_{m3}g_{mb}}s^3\right)}, \end{aligned} \tag{27}$$

where $A_{\rm dc}$ and ω_{p1} are also given by relation (16). By the following conditions, the small-signal transfer function is simplified as (29):

$$\frac{C_2}{g_{m2}} \gg \frac{C_1C_L}{g_{m3}C_m}, \quad \frac{C_1C_2C_L}{g_{m2}g_{m3}C_m} \gg \frac{C_1C_L}{g_{m3}g_m} \Longrightarrow \frac{g_{m2}}{C_2} \ll \frac{g_{m3}C_m}{C_1C_L}, \quad \frac{g_{m2}}{C_2} \ll \frac{g_m}{C_m}, \tag{28}$$

$$A_v(s) \approx A_{\rm dc} \times \frac{\left(1+\frac{C_m}{g_m}s\right)\left(1+\frac{C_2}{g_{m2}}s\right)}{\left(1+\frac{s}{\omega_{p1}}\right)\left(1+\frac{C_2}{g_{m2}}s\right)\left(1+\frac{C_1C_L}{g_{m3}C_m}s+\frac{C_1C_L}{g_{m3}g_m}s^2\right)} = A_{\rm dc} \times \frac{\left(1+\frac{C_m}{g_m}s\right)}{\left(1+\frac{s}{\omega_{p1}}\right)\left(1+\frac{C_1C_L}{g_{m3}C_m}s+\frac{C_1C_L}{g_{m3}g_m}s^2\right)}, \tag{29}$$

where one of the nondominant poles associated with C_2 is simply cancelled with the second zero. This pole-zero cancellation can be performed either at frequencies well beyond the unity-gain bandwidth or in the passband frequencies. Although, the pole-zero incomplete cancellation beyond the unity-gain bandwidth does not degrade the amplifier's closed-loop settling behavior,[18] however, this needs a large transconductance in current buffers and third stage amplifier and hence results in more power dissipation. Therefore, the pole-zero cancellation can be made in the passband and the required conditions can be satisfied by using a lower transconductance in the second stage amplifier and also making the second stage output parasitic capacitor, C_2, in order of a few pF by using nonminimum channel length transistors. Thus, the zero and nondominant poles are given by:

$$\omega_{z1} = -\frac{g_m}{C_m}, \tag{30}$$

$$\omega_{p2,3} \approx -\frac{g_m}{2C_m}\left(1 \pm \sqrt{1-\frac{4g_{m3}C_m^2}{g_mC_1C_L}}\right) \Longrightarrow |\omega_{p2,3}| \approx \sqrt{\frac{g_mg_{m3}}{C_1C_L}}. \tag{31}$$

It is worth mentioning that when the load capacitor is very larger than the compensation capacitor (the first case we considered) the conditions required to simplify the small-signal transfer function as (29) cannot be easily satisfied. Moreover, the assumptions made in (28) can easily be satisfied when the load capacitor decreases.

Similar to the previous sub-section, from Routh-Hurwitz criterion the maximum unity-gain bandwidth and minimum required transconductance for current buffers are derived as follows:

$$\omega_{\rm GBW} = \frac{g_{m1}}{C_m} < \frac{g_m}{C_m} \Longrightarrow g_{m1} < g_m. \tag{32}$$

Moreover, using a third-order Butterworth response in order to arrange the non-dominant poles as described in Eqs. (25) and (26) results in:

$$C_m = \sqrt{\frac{2g_{m1}C_1C_L}{g_{m3}}}, \quad g_m = 4g_{m1}\,. \tag{33}$$

The stability conditions and the maximum achievable ω_{GBW} for the proposed three-stage amplifiers are also summarized in Table 1 when the load capacitor is not very larger than the compensation capacitor(s).

3. Circuit Implementation

The circuit realization of the proposed three-stage DAFSMC amplifier is shown in Fig. 3. The first gain stage is a pMOS input pair folded-cascode amplifier realized by transistors M0−M10. The second inverting stage is implemented by a common-source amplifier with an active load. The last non-inverting stage is realized by transistors M13−M16. The g_{ma} and g_{mb} current buffers are simply realized by transistors M6 and M8 of the folded-cascode input stage amplifier, respectively, without any extra power dissipation. Finally, the feedforward transconductance stage, g_{mf}, is realized by M16.

To implement the proposed AFSMC amplifier it is sufficient to remove the upper compensation capacitor, C_{m2}, in Fig. 3 and use a twice (or in general the sum of C_{m1} and C_{m2}) size at the lower compensation capacitor, C_{m1}. It is worth mentioning that if $C_m = C_{m1} + C_{m2}$ then the unity-gain bandwidths of both the proposed amplifiers are the same.

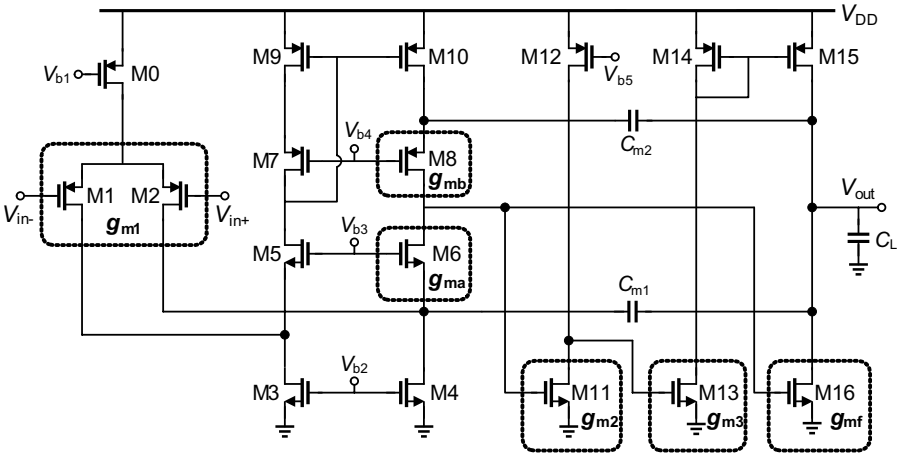


Fig. 3. Circuit implementation of the proposed DAFSMC and AFSMC three-stage amplifiers (C_{m2} is not used in the AFSMC amplifier).

4. Simulation Results

To prove the effectiveness of the proposed compensation techniques, HSPICE simulation results are performed using a standard 0.35 μm BSIM3v3 CMOS technology. The amplifiers were designed to achieve a dc gain about 100 dB and a gain-bandwidth product about 10 MHz and 20 MHz with a phase margin of at least 65° while driving the capacitive loads of 500 pF and 20 pF, respectively, from a single 1.5 V power supply. The simulations were performed in different process corner cases with a temperature variation spanning from −40°C to 85°C. Two different capacitive loads with the values of 500 pF and 20 pF were considered in all the simulations.

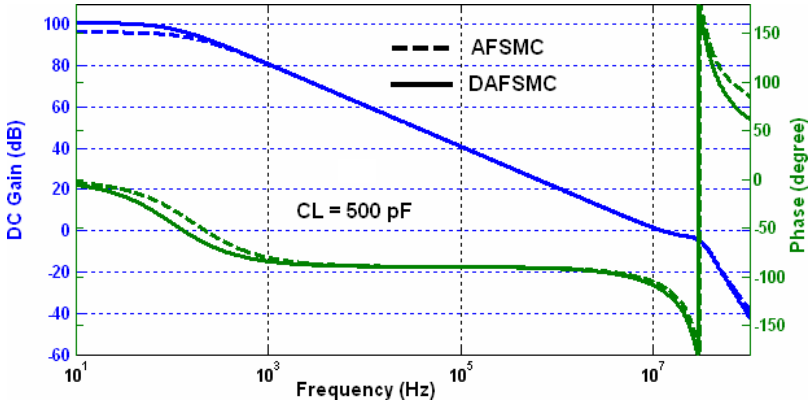
Table 2 shows the design parameters used in the circuit simulations. Figure 4 shows the simulated open-loop frequency response of the proposed amplifiers with both 500 pF and 20 pF load capacitors. The large signal transient response of the AFSMC and DAFSMC amplifiers in a unity-gain negative feedback configuration to a 500-mV input step is shown in Fig. 5 for different capacitive loads. Tables 3 and 4 summarize the simulation results of the proposed three-stage amplifiers. In Table 5, the simulated device parameters have been summarized.

The robustness of the proposed amplifiers against process and mismatch variations were evaluated through extensive circuit level Monte Carlo simulations. The results are shown in Fig. 6 where the gain bandwidth product and phase margin of the proposed amplifiers in two different load capacitor conditions are illustrated for 500 iterations in which both process and local variations of device parameters were taken into account. As is seen the proposed amplifiers are more tolerant to the process variations and show negligible performance degradation.

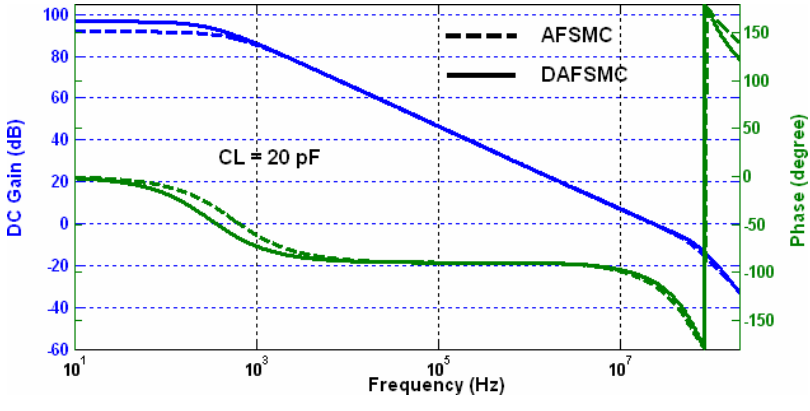
To characterize and compare the small signal (ω_{GBW}) and the large signal (slew rate) behaviors of different three-stage amplifiers the following figures of merits have

Table 2. Design parameters used in the simulations.

	AFSMC		DAFSMC	
Parameter	$C_L = 500$ pF	$C_L = 20$ pF	$C_L = 500$ pF	$C_L = 20$ pF
$(W/L)_{1,2}$	$4 \times 3\,\mu$m/$0.35\,\mu$m	$4 \times 5\,\mu$m/$0.35\,\mu$m	$4 \times 3\,\mu$m/$0.35\,\mu$m	$4 \times 5\,\mu$m/$0.35\,\mu$m
$(W/L)_{3,4}$	$2 \times 4\,\mu$m/$0.35\,\mu$m	$4 \times 8\,\mu$m/$0.35\,\mu$m	$2 \times 3\,\mu$m/$0.35\,\mu$m	$4 \times 4\,\mu$m/$0.35\,\mu$m
$(W/L)_{5,6}$	$2 \times 4\,\mu$m/$0.35\,\mu$m	$4 \times 4\,\mu$m/$0.35\,\mu$m	$2 \times 3\,\mu$m/$0.35\,\mu$m	$2 \times 4\,\mu$m/$0.35\,\mu$m
$(W/L)_{7,8}$	$4 \times 8\,\mu$m/$0.35\,\mu$m	$8 \times 10\,\mu$m/$0.35\,\mu$m	$4 \times 6\,\mu$m/$0.35\,\mu$m	$4 \times 10\,\mu$m/$0.35\,\mu$m
$(W/L)_{9,10}$	$4 \times 5\,\mu$m/$0.35\,\mu$m	$8 \times 8\,\mu$m/$0.35\,\mu$m	$4 \times 4\,\mu$m/$0.35\,\mu$m	$4 \times 8\,\mu$m/$0.35\,\mu$m
$(W/L)_{11}$	$2 \times 3\,\mu$m/$0.35\,\mu$m	$1 \times 2\,\mu$m/$0.35\,\mu$m	$2 \times 3\,\mu$m/$0.35\,\mu$m	$1 \times 2\,\mu$m/$0.35\,\mu$m
$(W/L)_{12}$	$4 \times 2\,\mu$m/$0.35\,\mu$m	$2 \times 4\,\mu$m/$0.35\,\mu$m	$4 \times 2\,\mu$m/$0.35\,\mu$m	$2 \times 4\,\mu$m/$0.35\,\mu$m
$(W/L)_{13}$	$4 \times 3\,\mu$m/$0.35\,\mu$m	$8 \times 40\,\mu$m/$3.0\,\mu$m	$4 \times 3\,\mu$m/$0.35\,\mu$m	$8 \times 40\,\mu$m/$3.0\,\mu$m
$(W/L)_{14,15}$	$4 \times 8\,\mu$m/$0.35\,\mu$m	$4 \times 8\,\mu$m/$0.35\,\mu$m	$4 \times 8\,\mu$m/$0.35\,\mu$m	$4 \times 8\,\mu$m/$0.35\,\mu$m
$(W/L)_{16}$	$4 \times 3\,\mu$m/$0.35\,\mu$m	$4 \times 8\,\mu$m/$0.35\,\mu$m	$4 \times 3\,\mu$m/$0.35\,\mu$m	$4 \times 8\,\mu$m/$0.35\,\mu$m
$(W/L)_0$	$4 \times 4\,\mu$m/$0.35\,\mu$m	$4 \times 4\,\mu$m/$0.35\,\mu$m	$4 \times 4\,\mu$m/$0.35\,\mu$m	$4 \times 4\,\mu$m/$0.35\,\mu$m
C_{m1}, C_{m2} (DAFSMC)	—	—	0.5 pF	0.5 pF
C_m(AFSMC)	1 pF	1 pF	—	—



(a)



(b)

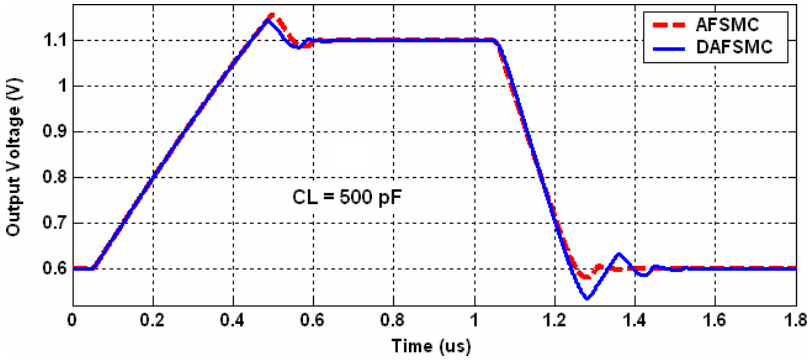
Fig. 4. Simulated open-loop frequency response of the amplifiers: (a) $C_L = 500\,\text{pF}$ and (b) $C_L = 20\,\text{pF}$.

been proposed[5]:

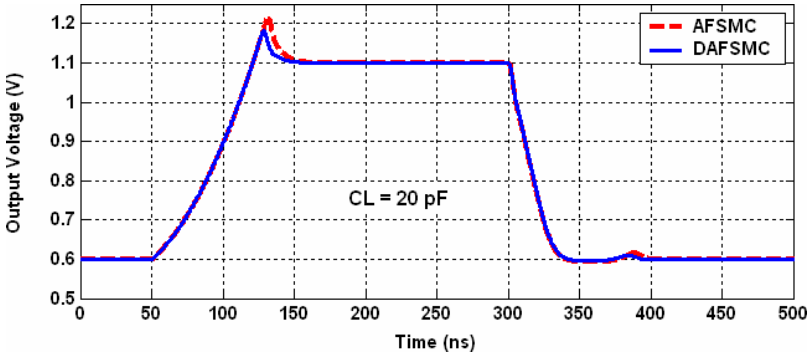
$$\text{FOM}_S = \frac{\omega_{\text{GBW}} \times C_L}{Power}\,, \quad \text{FOM}_L = \frac{\text{SR} \times C_L}{Power}\,, \tag{34}$$

$$\text{IFOM}_S = \frac{\omega_{\text{GBW}} \times C_L}{I_{\text{DD}}}\,, \quad \text{IFOM}_L = \frac{\text{SR} \times C_L}{I_{\text{DD}}}\,. \tag{35}$$

Table 6 summarizes the performance results of a few recently published three-stage amplifiers as well as the proposed ones in this paper. As is seen, the proposed amplifiers outperform all of the amplifiers listed in Table 6 as well. It is worth mentioning that the simulation results of the proposed amplifiers have been compared to the experimental results of the previously reported amplifiers in Table 6. Although this comparison is not fair, however, since the proposed amplifiers do not rely on any specific matching requirement, and on the other hand, they achieve a



(a)



(b)

Fig. 5. Simulated large signal transient response of the proposed amplifiers: (a) $C_L = 500\,\text{pF}$ and (b) $C_L = 20\,\text{pF}$.

small-signal figure of merit about three times that of the best reported values, therefore, a higher figure of merit is also expected for the measured results of the proposed amplifiers as well. When the load capacitor is small, it is more power efficient to employ the proposed single Miller capacitor active feedback technique in NMC amplifiers instead of RNMC ones as also recently used in Ref. 16. Because, in this case, a lower transconductance in the second stage amplifier is needed. Hence, a non-inverting second stage transconductance which is used in NMC amplifiers will be power efficient than employing a non-inverting transconductance in the third stage used in RNMC amplifiers.

The proposed DAFSMC amplifier outperforms the AFSMC one in regards of the both large signal and small signal figures of merits as theoretically expected since the transconductance of current buffers in the DAFSMC amplifier is about twice that of AFSMC one without any extra power dissipation.

Table 3. Performance summary of the simulated amplifiers ($C_L = 500\,\text{pF}$).

	Value					
	AFSMC			DAFSMC		
Parameter	TT 27°C	FF −40°C	SS 85°C	TT 27°C	FF −40°C	SS 85°C
DC gain (dB)	96.3	93.2	98.8	100.9	97.6	103.5
ω_{GBW} (MHz)	12.8	16.0	11.0	12.9	16.4	11.0
Phase margin (degree)	70.0	73.2	66.5	65.2	67.5	62.3
Power (μW)	195	220	181	173	199	158
SR^+/SR^-(V/μs)	1.35/2.72	2.0/4.16	0.93/1.72	1.36/2.9	2.0/4.37	0.95/1.9
0.1% Settling time (t_{s+}, t_{s-}) (ns)	595 375	397 250	860 544	591 523	394 371	883 809

Table 4. Performance summary of the simulated amplifiers ($C_L = 20\,\text{pF}$).

	Value					
	AFSMC			DAFSMC		
Parameter	TT 27°C	FF −40°C	SS 85°C	TT 27°C	FF −40°C	SS 85°C
DC gain (dB)	91.7	89.1	94.2	96.6	94.0	99.0
ω_{GBW} (MHz)	23.3	29.5	20.5	23.2	29.2	20.4
Phase margin (degree)	66.8	75.0	57.8	70.8	76.0	65.5
Power (μW)	470	636	407	396	562	334
SR^+/SR^-(V/μs)	9.1/16.4	12.1/17.5	7.4/15	9/16	12/17	7.5/15
0.1% Settling time (t_{s+}, t_{s-}) (ns)	111 122	73 46	131 180	105 113	68 44	122.5 165

Table 5. Simulated device parameters.

	AFSMC		DAFSMC	
Parameter	$C_L = 500\,\text{pF}$	$C_L = 20\,\text{pF}$	$C_L = 500\,\text{p}F$	$C_L = 20\,\text{pF}$
g_{m1}	73.0 μA/V	140.4 μA/V	73.5 μA/V	138.0 μA/V
g_{m2}	282.2 μA/V	83.6 μA/V	284.5 μA/V	83.4 μA/V
g_{m3}	587.4 μA/V	1425.8 μA/V	592.0 μA/V	1423.1 μA/V
g_{mf}	575.7 μA/V	1482.4 μA/V	580.2 μA/V	1479.9 μA/V
g_{ma}	353.5 μA/V	946.8 μA/V	191.4 μA/V	475.7 μA/V
g_{mb}	—	—	168.0 μA/V	468.4 μA/V
R_1	1893 kΩ	617.2 kΩ	3197 kΩ	1102 kΩ
R_2	84.8 kΩ	226.8 kΩ	84 kΩ	227.4 kΩ
R_3	33.6 kΩ	12.8 kΩ	33.3 kΩ	16.5 kΩ
C_1	76.5 fF	146 fF	64.3 fF	83.8 fF
C_2	36.7 fF	2614 fF	36.7 fF	2613 fF

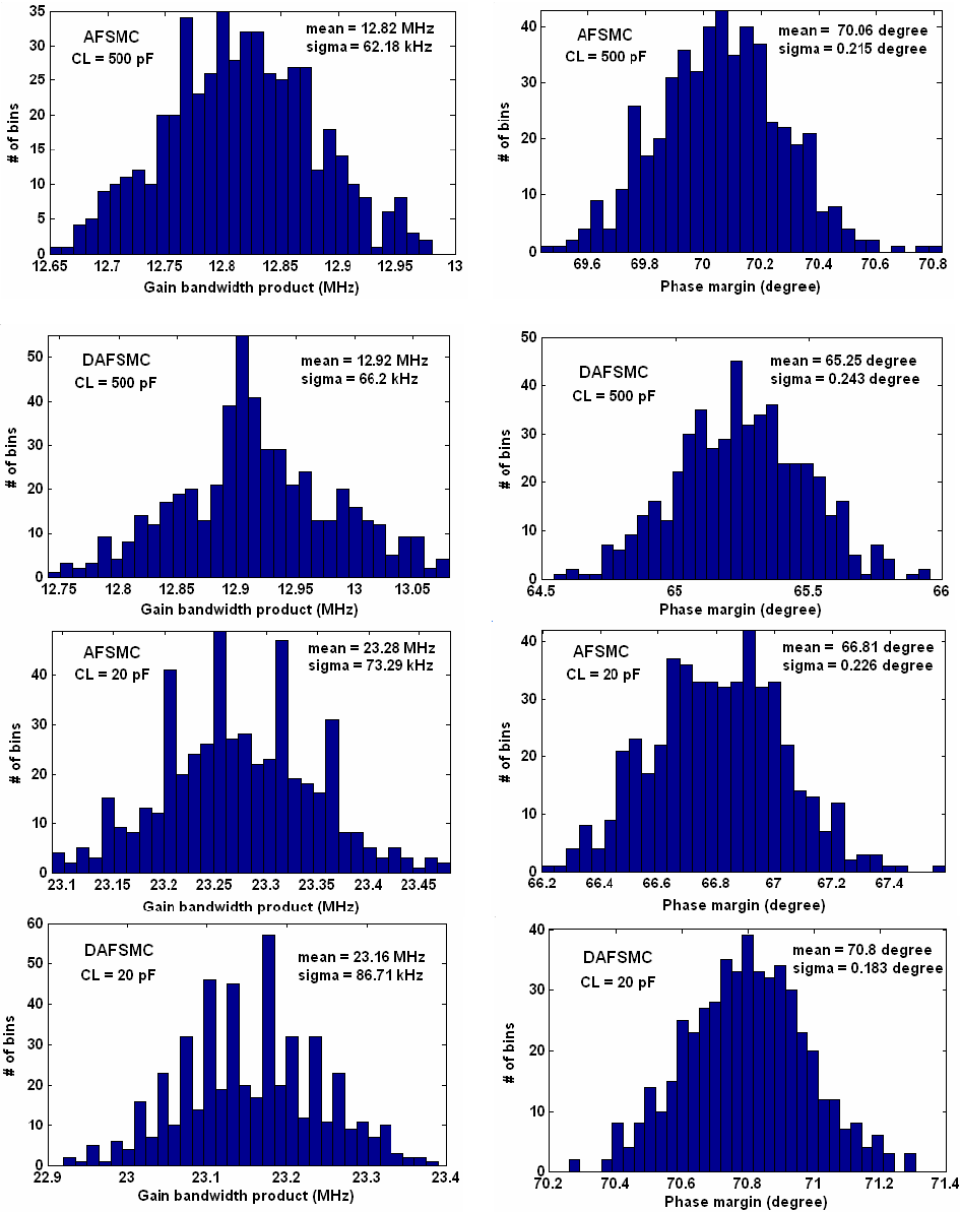


Fig. 6. Monte Carlo analysis results of gain-bandwidth product and phase margin of the proposed amplifiers with both 500 pF and 20 pF load capacitors.

Table 6. Comparison of different multistage amplifiers.

Amplifier topology	C_L (pF)	DC gain (dB)	V_{DD}	Power (mW)	GBW (MHz)	Average slew rate (V/μs)	Compensation capacitor(s): (pF)	FOM_S (MHz × pF)/ mW	FOM_L (V/μs × pF)/ mW	$IFOM_S$ (V/μs × pF)/ MHz′pF/mA	$IFOM_L$ (V/μs × pF)/ mA	CMOS technology
AFFC[3]	120	>100	2 V	0.40	4.5	1.49	$C_a = 7.0, C_m = 4$	1350	447	2700	894	0.8 μm
PFC[4]	130	>100	1.5 V	0.275	2.7	1.0	$C_{m1} = 15, C_{m2} = 3$	1276	473	1914	710	0.35 μm
$ACBC_F$[5]	500	>100	2 V	0.324	1.9	1.0	$C_m = 10, C_a = 3$	2932	1543	5864	3086	0.35 μm
SMC[6]	120	>100	2 V	0.38	4.6	2.3	$C_m = 7.0$	1453	726	2906	1452	0.5 μm
SMFFC[6]	120	>100	2 V	0.41	9.0	3.4	$C_m = 4.0$	2634	995	5268	1990	0.5 μm
TCFC[7]	150	>100	1.5 V	0.045	2.85	1.35	$C_{m1} = 1.1, C_{m2} = 0.92$	9500	3450	14,250	5175	0.35 μm
[8]	500	113	1.5 V	0.225	1.4	2.0	$C_{C1} = 30, C_{C2} = 20$	3111	4444	4667	6666	0.35 μm
RAFFC[12]	500	113	3 V	0.105	1.1	1.29	$C_{m1} = 11, C_{m2} = 0.35$	5238	6143	15,714	18,429	0.5 μm
[13]	500	109	3 V	0.249	2.87	1.55	$C_{C1} = 10, C_{C2} = 0.3$	5764	3112	17,292	9336	0.5 μm
[14][a]	150	112	1.5 V	0.021	1.8	0.7	$C_{C1} = 2$	12,857	5000	19,286	7500	0.35 μm
AFSMC[a] (this work)	500	96.3	1.5 V	0.195	12.8	2.04	$C_{m1} = 1.0$	32,821	5231	49,231	7846	0.35 μm
DAFSMC[a] (this work)	500	100.9	1.5 V	0.173	12.9	2.13	$C_{m1} = C_{m2} = 0.5$	37,283	6156	55,925	9234	0.35 μm
[9]	10	>100	3 V	1.473	20	18.3	$C_{C1} = 4, C_{C2} = 1.4$	135.8	124.2	407.3	372.7	0.35 μm
[11]	15	83.1	3 V	1.4	19.5	13.8	$C_{C1} = 0.7, C_{C2} = 3$	209	147.9	626.8	443.6	0.6 μm
[16]	20	>100	1.5 V	0.09	9.6	6.1	$C_a = 1.0$	2133	1356	3200	2033	0.35 μm
AFSMC[a] (this work)	20	91.7	1.5 V	0.470	23.3	12.75	$C_{m1} = 1.0$	991.5	542.6	1487	814	0.35 μm
DAFSMC[a] (this work)	20	96.6	1.5 V	0.396	23.2	12.5	$C_{m1} = C_{m2} = 0.5$	1172	631.3	1757.5	947	0.35 μm

Note: [a]Simulation results.

5. Conclusions

In this paper, two novel frequency compensation schemes called AFSMC and DAFSMC for three-stage amplifiers were proposed. It was shown that a larger bandwidth compared to the other reported techniques can be obtained by using a single Miller compensation capacitor with an active-feedback network. Furthermore, by using the active-feedback capacitors the die area of the amplifier is significantly reduced since their values can be made very small.

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