PAPER Special Section on Analog Circuit Techniques and Related Topics

A Design Procedure for CMOS Three-Stage NMC Amplifiers

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SUMMARY This paper presents a novel time-domain design procedure for fast-settling three-stage nested-Miller compensated (NMC) amplifiers. In the proposed design methodology, the amplifier is designed to settle within a definite time period with a given settling accuracy by optimizing both the power consumption and silicon die area. Detailed design equations are presented and the circuit level simulation results are provided to verify the usefulness of the proposed design procedure with respect to the previously reported design schemes.

key words: *three-stage amplifiers, nested-Miller compensation, small-signal settling, switched-capacitor circuits*

1. Introduction

The operational amplifiers widely used in the analog and mixed signal circuits are required to achieve high dc gain and large output swing in low voltage environments. Multistage amplifiers can be used to achieve high dc gain and large output signal swing simultaneously, because, although the cascoding of transistors is a well-known means to increase the dc gain of the single-stage amplifiers, however, this is not possible in the recent sub-micron CMOS technologies due to the reduced power supply voltage dictated by the technology scaling. Nonetheless, multistage amplifiers have additional frequency poles and zeros resulting in inherently instability and reduced signal bandwidth if any frequency compensation technique is not employed.

There are generally two different compensation schemes in the three-stage amplifiers: nested Miller compensation (NMC) and reversed nested Miller compensation (RNMC) [1]. In three-stage NMC amplifiers, the second stage is non-inverting and the last stage is inverting. This approach employs two compensation capacitors and exploits the Miller effect to split the frequency poles to achieve the desired phase margin and transient response. Nonetheless, this solution results in a gain-bandwidth product of one-quarter that can be achieved by a single-stage amplifier and in a high power consumption [2]. Recently, a few variants of the basic nested-Miller compensation scheme have been proposed in order to overcome the inherent limits of the NMC amplifiers [2]–[9].

On the other hand, in switched-capacitor applications the amplifier is needed to settle within a definite time period with a desired settling accuracy. Therefore, the transient settling performance is among the most critical aspects of high-speed amplifiers. The poor settling performance of amplifiers often makes them unsuitable to be used in switched-capacitors applications such as analog-to-digital converters. This issue has not been considered extensively in literature. There are only a few publications considering the settling performance in design optimization of three-stage NMC amplifiers.

In [7] the device parameters are sized based on the required value of gain bandwidth, slew rate, and noise budget and the design is not optimized for settling purposes. Design of a single-stage amplifier based on the unity-gain bandwidth and slew rate results in a fast settling behavior, but, this is not achieved in three-stage amplifiers where the settling performance can also be superior to the single-stage amplifiers as theoretically explored in [11].

In [10] a capacitor sizing rule based on damping factor of the open-loop transfer function has been proposed to achieve fast settling. In [11] the closed-loop analysis of three-stage amplifiers to predict and minimize the settling time by considering a third-order system with no zeros has been performed. The complete analysis including the effect of the zeros following a circuit level design example has been reported in [12]. In this design scheme, the value of compensation capacitors and small-signal settling time of an NMC amplifier are optimized for a given stage amplifiers transconductance and hence for a given power dissipation budget. Hence, this is not a complete design procedure since it does not support the optimization of all device parameters including the stage amplifiers transconductance for a given settling time and accuracy while this is necessary in the design of switched-capacitor circuits. This technique was also extended for other NMC-based three-stage amplifiers in [13].

In [14], only a few design points such as the effect of LHP and RHP zeros and open loop transfer function damping factor on the settling behavior are investigated. Hence, the damping factor of the non-dominant poles in the open-loop transfer function was considered as the single parameter to design fast-settling three-stage NMC amplifiers. Nonetheless, it is not reported any design optimization of the device parameters in this paper. Besides, the design approach presented in [14] needs an initial design based on heuristic choice of components. The final design is refined through extensive Spice simulations. Moreover, the power consumption is not considered in this design scheme.

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In [15] a design procedure for three-stage NMC amplifiers has been presented by considering both the large and small-signal settling regimes and also the circuit noise. However, since the zeros are neglected, the proposed design methodology does not predict the small-signal settling behavior with sufficient accuracy. To move the zeros to the higher frequencies, a larger transconductance is needed in the third stage amplifier and hence this results in more power dissipation.

In this paper, a new design methodology is presented for three-stage NMC amplifiers. In the proposed scheme the closed-loop poles and zeros are optimized to minimize the required power consumption and the value of compensation capacitors for a given settling time and accuracy. The linear settling behavior of three-stage amplifiers is only considered in this paper like [10]–[14] since the slewing behavior of class A amplifiers is well understood. Although the detailed design procedure and equations were presented for basic three-stage NMC amplifiers, but, the proposed design scheme can be employed in the other variations of three-stage NMC and RNMC amplifiers with a straight forward extension.

The paper is organized as follows. In Sect. 2, the basic block diagram of three-stage NMC amplifiers and a typical circuit implementation are studied and the closed-loop transfer function with an arbitrary feedback factor is obtained. A standard third order system with three poles and two zeros is considered to develop the proposed design scheme in Sect. 3. A design example and simulation results are provided in Sect. 4. Finally, Sect. 5 concludes the paper.

2. NMC Three-Stage Amplifier

Figure 1 illustrates the basic block diagram of three-stage NMC amplifiers where g_{mi}, C_i, and R_i represent the ith stage transconductance, the equivalent parasitic capacitance, and the output resistance of the corresponding gain stages, respectively. C_L includes the load capacitor as well as the output parasitic capacitor of the third stage. The capacitors C_{m1} and C_{m2} perform the nested Miller compensation providing the closed-loop response stability.

A typical circuit implementation of a three-stage NMC amplifier is shown in Fig. 2. The first gain stage is an nMOS input differential pair realized by transistors M1-M5. The second non-inverting stage is implemented by a common-source amplifier and active current mirror comprised of transistors M6-M9. The last inverting stage is realized by transistors M10 and M11.

By assuming high intrinsic dc gain in stage amplifiers and compensation and load capacitors are much greater than all parasitic capacitances of the circuit, i.e. $g_{mi}R_i \gg 1$ and $C_L, C_{m1}, C_{m2} \gg C_{1,2}$, and $g_{m3} \gg g_{m1}, g_{m2}$, the closed-loop signal transfer function of the NMC amplifier is expressed by:

$$A_v(s) = \frac{A_{dc}}{1+\beta A_{dc}} \frac{1 - \frac{C_{m2}}{g_{m3}}s - \frac{C_{m1}C_{m2}}{g_{m2}g_{m3}}s^2}{D(s)} \tag{1}$$

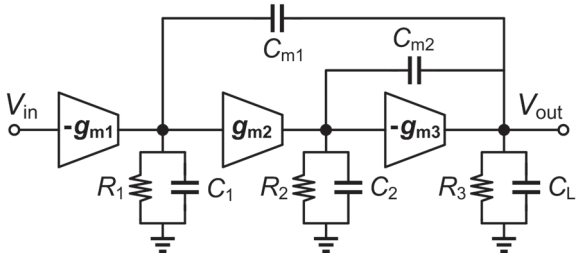

Fig. 1 Block diagram of basic three-stage NMC amplifier.

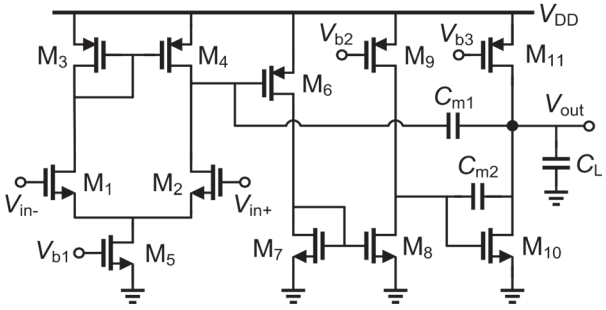

Fig. 2 Circuit implementation of an NMC three-stage amplifier.

$$D(s) = 1 + \left(\frac{C_{m1}}{\beta g_{m1}} - \frac{C_{m2}}{g_{m3}}\right)s + \left(\frac{g_{m3} - g_{m2} - \beta g_{m1}}{\beta g_{m1}}\frac{C_{m1}C_{m2}}{g_{m2}g_{m3}}\right)s^2 + \frac{C_{m1}C_{m2}C_L}{\beta g_{m1}g_{m2}g_{m3}}s^3$$

where A_{dc} is the overall dc gain of the amplifier and β is the feedback factor. The amplifier gain-bandwidth product (ω_{GBW}) is well approximated by the open-loop unity-gain frequency as $\omega_{GBW} = g_{m1}/C_{m1}$.

As is seen from (1), the closed-loop amplifier has three poles and two zeros. The zeros are simply given by:

$$\omega_{z,RHP} = \frac{g_{m2}}{2C_{m1}}\left(-1 + \sqrt{1 + \frac{4g_{m3}C_{m1}}{g_{m2}C_{m2}}}\right) \tag{2}$$

$$\omega_{z,LHP} = -\frac{g_{m2}}{2C_{m1}}\left(1 + \sqrt{1 + \frac{4g_{m3}C_{m1}}{g_{m2}C_{m2}}}\right) \tag{3}$$

The right half plane (RHP) zero is located at a lower frequency than the left half plane (LHP) zero. The RHP zero can potentially degrade the closed-loop stability and is required to be equal or larger than the magnitude of the open-loop non-dominants poles [3]. To remove this RHP zero, different modifications on the basic three-stage NMC amplifier have been proposed such as placing a nulling resistor in series with the compensation capacitors called the NMCNR amplifier [3].

3. Design Procedure

In order to investigate the small-signal settling behavior of the three-stage NMC amplifiers and develop a systematic design procedure, the following standard transfer function

with three poles and two zeros is considered:

$$H(s) = H_0 \frac{(1+s/\omega_{z1})(1+s/\omega_{z2})}{(1+s/\omega_p)\left(1+\frac{2\zeta}{\omega_n}s+\frac{s^2}{\omega_n^2}\right)} = \frac{k(s+z_1\zeta\omega_n)(s+z_2\zeta\omega_n)}{(s+\alpha\zeta\omega_n)(s^2+2\zeta\omega_n s+\omega_n^2)} \quad (4)$$

There are five different system parameters determining the settling performance of a system described by (4). ω_n and ζ are called the natural frequency and damping factor, respectively. The zeros and real pole have been normalized with respect to the real part of complex poles with the normalization factors of z_1, z_2, and α, respectively.

In switched-capacitor circuits, the step response determines the small-signal settling performance in the time domain. The time response $s(t)$ can be obtained by using the inverse Laplace transformation. The settling time is the time period required by the amplifier output to reach and remain within a specified error band centered on the output steady state value, starting from the time when an input step is applied to the amplifier. Hence, the settling error in a definite time period of t_{ss} defined as $\varepsilon_s = (s(\infty) - s(t_{ss}))/s(\infty)$ is given by:

$$\varepsilon_s = a_1 e^{-\alpha\zeta\omega_n t_{ss}} + a_2 e^{-\zeta\omega_n t_{ss}} \cos\left(\omega_n t_{ss}\sqrt{1-\zeta^2}\right) + a_3 e^{-\zeta\omega_n t_{ss}} \sin\left(\omega_n t_{ss}\sqrt{1-\zeta^2}\right) \quad (5)$$

where $s(t)$ is the step response and a_1, a_2, and a_3 are as follows:

$$a_1 = \frac{(z_1-\alpha)(z_2-\alpha)}{z_1 z_2\,(1-2\alpha\zeta^2+\alpha^2\zeta^2)}$$

$$a_2 = \frac{\alpha\,(z_1+z_2)-\alpha^2+z_1 z_2\alpha\zeta^2\,(\alpha-2)}{z_1 z_2\,(1-2\alpha\zeta^2+\alpha^2\zeta^2)}$$

$$a_3 = \frac{A}{z_1 z_2\zeta\,(1-2\alpha\zeta^2+\alpha^2\zeta^2)\sqrt{1-\zeta^2}}$$

$$A = \alpha^2\zeta^2+\alpha\zeta^2(z_1+z_2)-\alpha-\alpha^2\zeta^2(z_1+z_2) +\alpha z_1 z_2\zeta^2\left(1-2\zeta^2+\alpha\zeta^2\right)$$

The relation expressed in (5) is very complicated to analytically obtain the system parameters, i.e. z_1, z_2, α, ω_n and ζ, for a specific settling error in a definite time period of t_{ss}. Therefore, numerical calculations are utilized to optimize the small-signal settling behavior. This is performed by searching different possibilities of the system parameters to satisfy the relation (5) and selecting the one that results in the minimum possible value for ω_n and considering several design hints as follows.

Firstly, the effects of α and ζ on the settling behavior is studied by neglecting the effects of the zeros. For a given settling error level, the optimal value of ζ corresponds to minimizing the value of $\omega_n t_{ss}$ since this results in the narrowest required bandwidth. The frequency of oscillatory term in (5) is inversely related to ζ and hence ζ will control the sign of the oscillatory term. Figure 3 shows the effect of

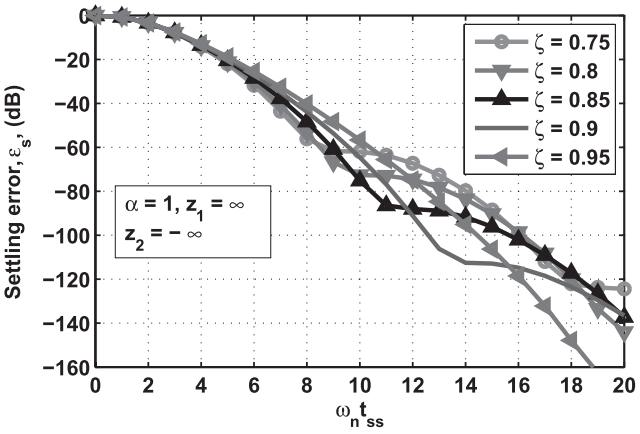

Fig. 3 Settling error versus $\omega_n t_{ss}$ for different values of ζ.

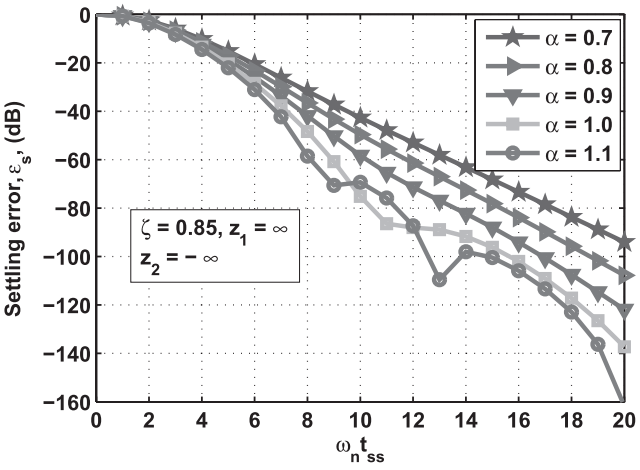

Fig. 4 Settling error versus $\omega_n t_{ss}$ for different values of α.

ζ on the settling behavior. As is seen there is a fast-settling region with high slope followed by a slow settling region. In fast-settling region the slope is inversely proportional to ζ and the amplifier will not overshoot when $\alpha \leq 1$ [16]. So, the optimal value of ζ is selected such that the inflection point is placed after desired settling accuracy and ζ should be as small as possible. For example, the optimal value of ζ for −40 dB and −60 dB settling errors is 0.7 and 0.85, respectively, with considering a sufficient margin for process variations that result in random changes in system parameters.

After optimization the value of ζ for a given settling accuracy, the effect of α in the settling performance is investigated. As shown in Fig. 4, when α is decreased, the real pole is closed to the origin and the system looks like a single-pole one. On the other hand, increasing α results in large overshoots and high sensitivity to the changes in the pole positions. There is a tradeoff between optimal linear settling and robust design because decreasing α increases the required $\omega_n t_{ss}$. Therefore, depending on the required settling accuracy, α can be considered in the range of 0.8 to 1.0 to achieve a robust design as well as not excessively

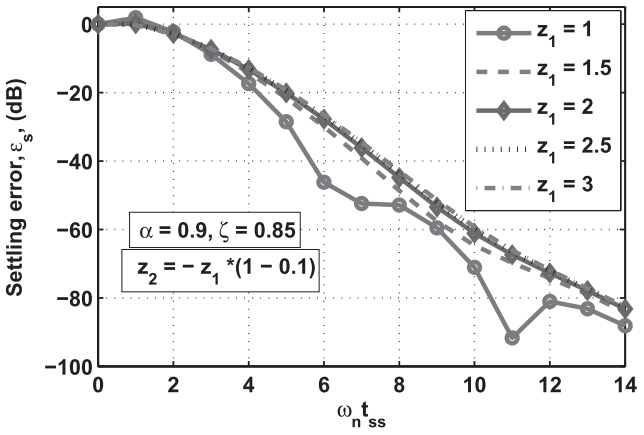

Fig. 5 Settling error versus $\omega_n t_{ss}$ for different values of z_1 and z_2.

increase the required amplifier bandwidth.

Now, the effect of the zeros on the settling performance is considered. As given in relations (2) and (3) the zeros are not independent and they have about 10% difference in their magnitude in most practical applications and hence their effect should be investigated together. Figure 5 shows the settling error for different values of the zeros. As is seen, the value of z_1 needs to be higher than 2 to achieve much less sensitivity to the process variations. With such value of the zeros, their effect on the settling performance is negligible as is seen from Figs. 4 and 5 where approximately the same value of $\omega_n t_{ss}$ is required.

Having known the system parameters from the above-mentioned design procedure and hints, the device electrical parameters such as transconductance of the stage amplifiers and the value of compensation capacitors are obtained by equating relations (1) and (4). This results in the following relations:

$$g_{m1} = \frac{\alpha\omega_n C_L}{\beta\zeta|z_1 z_2|} \tag{6}$$

$$g_{m2} = \frac{\omega_n C_L\left(\alpha\,(z_1+z_2) - 2\alpha z_1 z_2\zeta^2 - z_1 z_2\right)(z_1+z_2)}{z_1^2 z_2^2 \zeta} \tag{7}$$

$$g_{m3} = \omega_n C_L \frac{B}{z_1^2 z_2^2 \zeta} \tag{8}$$

$$C_{m1} = \frac{C_L\left(\alpha(z_1+z_2) - 2\alpha z_1 z_2\zeta^2 - z_1 z_2\right)}{z_1^2 z_2^2 \zeta^2} \tag{9}$$

$$C_{m2} = \frac{C_L\,(z_1+z_2)}{|z_1^3 z_2^3|\zeta^2} B \tag{10}$$

where

$$B = z_1 z_2\left[\alpha\zeta^2(z_1 z_2 - 2z_1 - 2z_2) + (\alpha - z_1 - z_2)\right] + 2z_1^2 z_2^2\zeta^2 + \alpha\left(z_1^2 + z_2^2\right) \tag{11}$$

The power consumption and silicon die area of the transistors in an operational amplifier are directly related to their transconductance [17]. In relations (6)–(8) the required value of stage amplifiers transconductance is optimized by choosing an appropriate value of the system parameters. This is performed by minimizing the required value of ω_n and considering several design hints to achieve a robust design against process corner cases, temperature variations, and device mismatches. As is seen from relations (6)–(8), they are directly related to ω_n. Hence, the power consumption of the amplifier is also optimized somehow. This means that the system parameters are not directly optimized to minimize the power consumption since the main design procedure is to develop a systematic approach to achieve fast settling with sufficient robustness and minimized power consumption. It worth mentioning that although it is possible to minimize the required total value of transconductances by properly choosing the system parameters, i.e. $z_1, z_2, \alpha, \omega_n$ and ζ, however, this will not only result in a fast settling design, but also may result in an unstable design.

One the other hand, the overall required die area is determined by the size of the compensation capacitors. The proposed design approach results in near optimal sized compensation capacitors as will be shown in the next section by comparing the required value of the compensation capacitors in this design methodology and their optimal values proposed in [12]. It is worth mentioning that although there is not any direct attempt to optimize the value of compensation capacitors, however, this is also achieved by properly sizing of the system parameters.

4. Design Example and Simulation Results

To verify the usefulness of the proposed design procedure, the amplifier shown in Fig. 2 was designed and simulated using a commercial 0.35 μm CMOS technology with HSPICE. The design is targeted to achieve 0.1% or −60 dB settling accuracy within 25 ns while driving a 2 pF load capacitance from a single 1.8 V power supply in a unity-gain voltage follower configuration.

The system parameters using the proposed design procedure in Sect. 3 are obtained as $\alpha = 0.9$, $\zeta = 0.85$, $z_1 = 2$, $z_2 = -1.8$, and $\omega_n t_{ss} = 10$. Since t_{ss} was considered 25 ns hence $\omega_n = 4 \times 10^8$ is achieved. Then, relations (6)–(10) are used to find the optimal values of the stage amplifiers transconductance and the compensation capacitors as $g_{m1} = 235\,\mu$A/V, $g_{m2} = 123\,\mu$A/V, $g_{m3} = 2.33$ mA/V, $C_{m1} = 1.8$ pF, and $C_{m2} = 0.4$ pF.

To achieve large output signal swing and sufficient linearity, all devices are biased in strong inversion with effective overdrive voltage (V_{eff}) about 200 mV. Hence having known g_m and V_{eff} of all critical devices, their bias currents and aspect ratios are obtained. The non-minimum channel length is utilized in all transistors to get large dc gain. The resulted device parameters are summarized in Table 1.

Figure 6 shows the amplifier's settling response when a 50 mV step is applied to the amplifier's input to ensure the linear settling for three different corner cases and temperature variations spanning from −40°C to 85°C. The simulation results are summarized in Table 2 where t_{ss+} and t_{ss-} represent the settling time when a positive and negative in-

Table 1 Simulated device sizes.

Parameter	W/L	$g_m(\mu A/V)$
M1, M2	$1\times4\,\mu m/0.5\,\mu m$	**243(g_{m1})**
M3, M4	$4\times4\,\mu m/0.5\,\mu m$	238
M5	$2\times4\,\mu m/0.5\,\mu m$	480
M6	$2\times5\,\mu m/0.5\,\mu m$	**133(g_{m2})**
M7, M8	$1\times2\,\mu m/0.5\,\mu m$	118
M9	$2\times4\,\mu m/0.5\,\mu m$	121
M10	$4\times8\,\mu m/0.5\,\mu m$	**2260(g_{m3})**
M11	$12\times12\,\mu m/0.5\,\mu m$	2402
C_{m1}	1.8 pF	
C_{m2}	0.4 pF	

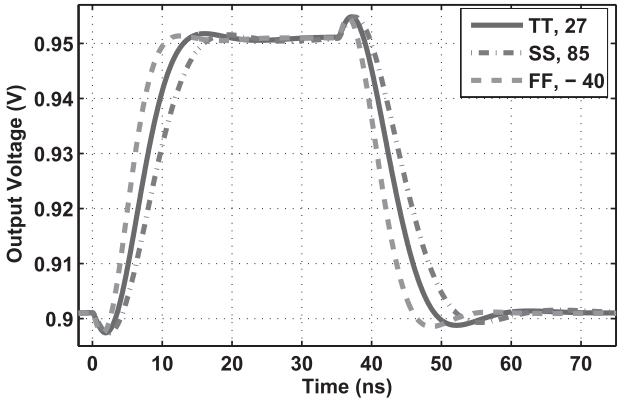

Fig. 6 Settling response to a 50 mV input step.

Table 2 Simulation results summary.

Parameter	TT@27°C	SS@85°C	FF@−40°C
DC gain (dB)	85.7	86.8	84.4
f_{GBW} (MHz)	21.3	17.3	27.7
Phase margin (degree)	62.0	62.8	61.9
0.1% settling time (t_{ss+}/t_{ss-})	13.1 ns 20.9 ns	16.0 ns 23.9 ns	10.2 ns 16.7 ns
$N = t_{ss+}\times2\pi\times f_{GBW}$	1.75	1.74	1.78
$N = t_{ss-}\times2\pi\times f_{GBW}$	2.8	2.6	2.9
Static power consumption	545 μW	538 μW	552 μW
Power supply voltage	1.8 V		
Technology	0.35 μm 2P4M CMOS		

put step is applied to the amplifier, respectively. It is worth mentioning that in a single-ended amplifier, the positive and negative settling times can be different whereas the settling time of a standard ideal third-order system described by relation (4) is the same for both positive and negative input steps. Hence, in the design of single-ended amplifiers, the worst case of positive and negative settling times should be considered to be well within the desired value.

The time constant of a closed-loop single-pole amplifier is given by $\tau = 1/(\beta\times\omega_{GBW})$ where β and ω_{GBW} represent the feedback factor and unity-gain bandwidth of the open-loop amplifier, respectively. Hence, the settling error is derived as $\varepsilon_s = e^{-t_{ss}/\tau} = e^{-N}$ for a first-order system. As is clear, the settling error can be described by $N = t_{ss}/\tau$ which is called the normalized settling time. This parameter shows how many time constants are needed that the amplifier's output to settle with a given settling accuracy. However, in high-order systems the relation between the normalized settling time and the settling error is somehow complicated. Nonetheless, this parameter can also be used to describe the settling performance with respect to a single pole amplifier. As theoretically demonstrated in [11], the required normalized settling time for a desired settling accuracy in a three-stage amplifier can be less than that of a single-stage amplifier. This means that third-order amplifiers can be designed to settle faster than the first- and second-order amplifiers. Therefore, the value of N can be used to provide a fair comparison between the different designed amplifiers to evaluate the settling performance optimization.

As summarized in Table 2, the achieved N is comparable to the limits reported in literature which is 4 for 0.1% settling error as theoretically suggested in [11]. This clearly indicates that the proposed design methodology results in better small-signal settling performance compared to the previously best reported designs even considering different process corner cases, temperature and device variations. It should be noted that in Table 2, the value of N is separately computed for the positive and negative settling times since as mentioned before, the positive and negative settling times of a single-ended amplifier can be different. The minimal variation of N across the process corner cases suggests robust settling performance of the designed amplifier as also examined by Monte Carlo simulations.

The robustness of the proposed design procedure against process and mismatch variations were evaluated through extensive circuit level Monte Carlo simulations. The results are shown in Fig. 7 where both the positive and negative settling times for 0.1% dynamic settling error of the designed amplifier are illustrated for 500 iterations in which both process and local variations of device parameters were taken into account and 5% intentional absolute variation was considered in the compensation capacitors. As is seen the designed amplifier is more tolerant to the process and components variations and shows negligible performance degradation.

The proposed design scheme in [7] results in large compensation capacitors and stage amplifiers transconductance compared to the proposed design procedure in this paper. As an example, the proposed design procedure needs $g_{m1} = 96.5\,\mu$A/V, $g_{m2} = 48.8\,\mu$A/V, $g_{m3} = 943\,\mu$A/V, $C_{m1} = 7.3$ pF, and $C_{m2} = 1.6$ pF for 1% settling error within 150 ns settling time with $C_L = 10$ pF. While for the same settling time and error, the reported device parameters in [7] are as $g_{m1} = g_{m2} = 500\,\mu$A/V, $g_{m3} = 2$ mA/V, $C_{m1} = 8$ pF, and $C_{m2} = 6.6$ pF. It is also worth mentioning that the NMCNR amplifier was designed in [7] which usually achieves a higher performance respected to the conventional NMC amplifier by moving the RHP zero to the higher frequencies as mentioned in [14]. In other words, if the proposed design procedure is utilized in the design of NMCNR amplifiers much better performance is also expected.

In comparison with [12], the proposed design procedure is evaluated in two different conditions. Firstly, to achieve 0.1% settling error within 25 ns, the value of com-

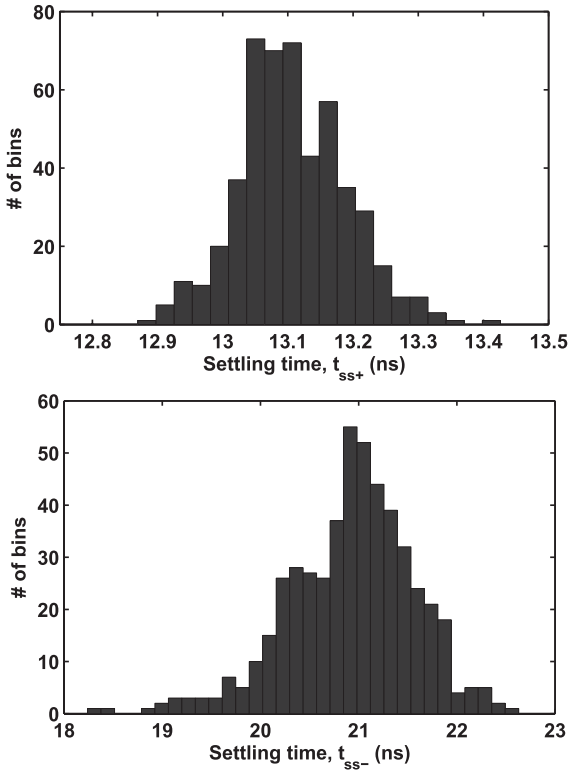

Fig. 7 Monte Carlo simulation results of both positive and negative settling times.

pensation capacitors are also obtained from the relations reported in [12] by assuming the stage amplifiers transconductance obtained here. Hence, $C_{m1} = 1.53\,\text{pF}$, $C_{m2} = 0.34\,\text{pF}$, and $t_{ss} = 15\,\text{ns}$ are calculated from the relations mentioned in [12]. As seen from Table 1, the value of compensation capacitors in the presented design example is very close to their optimized values in [12]. This clearly shows that the proposed design scheme also optimizes the die area. Besides, according to the simulation results reported in Table 2, the settling time of the proposed design is also optimized.

As another example, a design with 1% settling error within $1.15\,\mu\text{s}$ with $C_L = 10\,\text{pF}$ (reported in [12]) is performed by the proposed design procedure. By using the relations (6)–(10) and Figs. (3)–(5), the device parameters are obtained as $g_{m1} = 12.6\,\mu\text{A/V}$, $g_{m2} = 6.4\,\mu\text{A/V}$, $g_{m3} = 123\,\mu\text{A/V}$, $C_{m1} = 7.3\,\text{pF}$, and $C_{m2} = 1.6\,\text{pF}$. Compared to the results reported in [12], the same results are approximately achieved here. Therefore, in the presented design procedure the optimal value of stage amplifiers transconductance and compensation capacitors are systematically obtained while in the design scheme in [12], [13] only the value of compensation capacitors and settling time are achieved through a systematic optimization by primary assuming the transconductance value of the stage amplifiers.

Comparing the presented design example in [14] for 0.1% settling error within 25 ns with $C_L = 2\,\text{pF}$ with this paper, the proposed design scheme needs a much smaller value for the inner compensation capacitor, C_{m2}, for the same settling error and time. The required current consumption is about six times lower than that reported in [14] even the basic NMC amplifier was designed in this paper while the NMCNR technique was used as the design example in [14].

The presented design procedure is applicable to third order systems described by relation (4) and therefore can be extended to other three-stage amplifiers as well. It can help circuit designers as well as it can be used in the computer aided circuit design tools.

5. Conclusions

A novel systematic design procedure was presented for fast-settling three-stage NMC amplifiers. The value of stage amplifiers transconductance and compensation capacitors are optimized for a given settling accuracy within a definite time period to achieve a low-power and robust design. The proposed design methodology can be used in the design of three-stage amplifiers to realize fast-settling switched-capacitors circuits.

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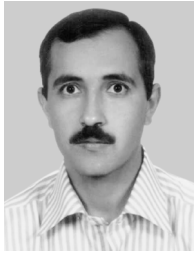

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