

# Hybrid Cascode Compensation for Two-Stage CMOS Opamps

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**SUMMARY** This paper presents the analysis of hybrid cascode compensation scheme, merged Ahuja and improved Ahuja style compensation methods, which is used in two-stage CMOS operational transconductance amplifiers (OTAs). The open loop signal transfer function is derived to allow the accurate estimation of the poles and zeros. This analytical approach shows that the non-dominant poles and zeros of the hybrid cascode compensation are about 40 percent greater than those of the conventional cascode compensation. Circuit level simulation results are provided to show the accuracy of the calculated expressions and also the usefulness of the proposed cascode compensation technique.

**key words:** operational transconductance amplifiers, cascode compensation, switched-capacitor circuits

## 1. Introduction

The realization of a CMOS operational amplifier that combines high dc gain with high unity gain bandwidth and output signal swing in low-voltage environments demands two-stage structures since cascoding is not possible due to the output voltage swing considerations. But the major concern of two-stage OTAs is the speed of this type of amplifiers due to their additional poles and zeros in their signal transfer function where without any frequency compensation, they are prone to instability. Several frequency compensation methods have been proposed to design a stable two-stage OTA such as Miller and cascode compensation schemes [1]–[4].

The Miller compensation scheme has a pole splitting effect which moves one pole to a lower frequency and the other one to a high frequency in order to make a dominant pole frequency [1], [2]. The main drawbacks of Miller compensation scheme are the low speed and low power supply rejection ratio (PSRR) compared to the cascode compensation. In Miller compensation, a compensating resistor is also needed to be placed in series with compensating capacitor in order to move the right half plane zero to the left half plane. The value of this resistor is affected by temperature and other variations of device fabrication which results in more variation in OTA's frequency performance. Mainly MOS transistors in the triode region are used to implement such resistors where their design can be another concern in low-voltage applications [5]. Of course, in sampled data

circuits some techniques such as clock boosting and bootstrapping can be used. But, they suffer from the design and implementation complexities.

Cascode compensation scheme alleviates the above-mentioned problems. In this technique, a capacitor is located between a low-impedance node of the first stage and the second stage output node [3], [6]. It achieves higher speed and higher PSRR compared to Miller compensation at the cost of complex design and analysis procedure [3], [4], [7].

A novel cascode compensation scheme called hybrid cascode compensation has been introduced in [8] by the author. In this method, two distinct capacitors are used between two low-impedance nodes of the first stage and the output node. In turn, this compensation technique merges Ahuja [3] and improved Ahuja style [9] compensation methods. This scheme of compensation yields a higher amplifier bandwidth compared to the standard Miller and conventional cascode compensation techniques at the cost of more complex design procedure for the settling behavior of the amplifier. This technique also offers all advantages of the cascode compensation technique such as high PSRR, etc.

In [8] a closed loop analysis of hybrid cascode compensation has been introduced and also a closed loop design procedure has been proposed. In order to get more insight in the design of this compensation scheme and also show its usefulness further, its open loop signal transfer function is obtained here to estimate accurately its poles and zeros.

The paper is organized as follows. Section 2 presents the open loop analysis of a two-stage opamp employing the hybrid cascode compensation method to obtain the poles and zeros, accurately. In this section, the open loop poles and zeros of the other two cascode compensation schemes are also obtained. In Sect. 3 simulation results are given to show the accuracy of the obtained relations for the poles and zeros of the hybrid cascode compensation and also its usefulness compared to the other cascode compensation methods. Section 4 concludes the paper.

## 2. Open Loop Analysis

### 2.1 Hybrid Cascode Compensation

Figure 1 shows a two-stage OTA composed of the folded-cascode as the first stage and the common-source amplifier as the second stage that employs the hybrid cascode compensation. Such opamps are employed in the switched-

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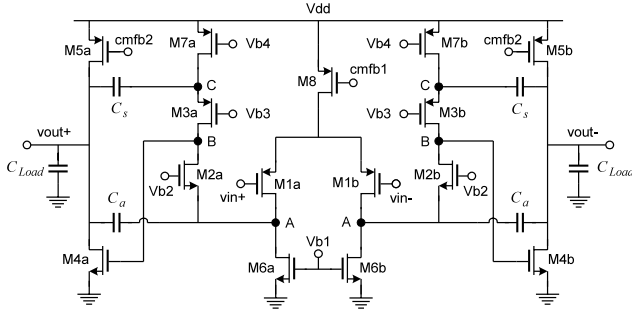


Fig. 1 A two-stage OTA with hybrid cascode compensation.

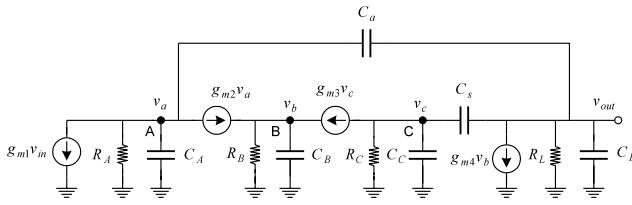


Fig. 2 Open-loop small signal equivalent circuit.

capacitor circuits and the other applications that the rail-to-rail input stage is not needed. It is worth mentioning that this OTA structure has been chosen for its simplicity and the compensation method can be applied to both rail-to-rail and non rail-to-rail input stage two-stage OTAs. As shown in Fig. 1 two separate capacitors,  $C_a$  and  $C_s$ , have been used for compensation of the opamp where  $C_a$  is used in a signal path and  $C_s$  in a non-signal path. In Fig. 2 the small signal equivalent circuit for differential inputs is shown.

The small signal equations of the circuit shown in Fig. 1 can be written as follows:

$$g_{m1}v_{in} + \frac{v_a}{R_A} + sC_A v_a + g_{m2}v_a + sC_a(v_a - v_{out}) = 0 \quad (1)$$

$$\frac{v_b}{R_B} + sC_B v_b - g_{m2}v_a - g_{m3}v_c = 0 \quad (2)$$

$$\frac{v_c}{R_C} + sC_C v_c + g_{m3}v_c + sC_s(v_c - v_{out}) = 0 \quad (3)$$

$$g_{m4}v_b + sC_s(v_{out} - v_c) + \frac{v_{out}}{R_L} + sC_L v_{out} + sC_a(v_{out} - v_a) = 0 \quad (4)$$

where  $R_A, R_B, R_C, R_L$  and  $C_A, C_B, C_C, C_L$  are the resistances and capacitances seen at the nodes A, B, C, and output, respectively and are given as follows:

$$R_A = r_{ds1} || r_{ds6} || \frac{g_{m3}r_{ds3}r_{ds7}}{1 + g_{m2}r_{ds2}} \quad (5)$$

$$R_B = g_{m2}r_{ds2}(r_{ds1} || r_{ds6}) || g_{m3}r_{ds3}r_{ds7} \quad (6)$$

$$R_C = r_{ds7} || \frac{g_{m2}r_{ds2}(r_{ds1} || r_{ds6})}{1 + g_{m3}r_{ds3}} \quad (7)$$

$$R_L = r_{ds4} || r_{ds5} \quad (8)$$

$$C_A = C_{db1} + C_{gs2} + C_{db6} + C_{sb2} + C_{gd6} \quad (9)$$

$$C_B = C_{db2} + C_{db3} + C_{gs4} + C_{gd2} + C_{gd3} \quad (10)$$

$$C_C = C_{gs3} + C_{sb3} + C_{gd7} + C_{db7} \quad (11)$$

$$C_L = C_{Load} + C_{db4} + C_{db5} + C_{gd5} \quad (12)$$

After solving Eqs. (1)–(4), the open loop signal transfer function is obtained as follows:

$$A_v(s) = \frac{v_{out}}{v_{in}} = g_{m1} \left( g_{m3} + R_C^{-1} + s(C_s + C_C) \right) \times \frac{(g_{m2}g_{m4} - sC_a R_B^{-1} - s^2 C_a C_B)}{s^4 d_4 + s^3 d_3 + s^2 d_2 + s d_1 + d_0} \quad (13)$$

where  $d_4 - d_0$  can be obtained in terms of the circuit parameters. However, obtaining the exact values of these coefficients will be very complicated and will not give any intuitive approach in the circuit design. On the other hand, the exact solution of the above-mentioned equation, (13), analytically could not give simple relations for the poles of the system. So, it is assumed that the parasitic capacitances of the nodes A, B, and C are much smaller than the compensation capacitors  $C_a, C_s$  and the load capacitance  $C_L$ . It is also assumed that the transconductance of transistors,  $g_{mi}$ , is much greater than the conductances seen at the nodes A, B, C, and output. Hence, the denominator of the signal transfer function can be approximated as follows:

$$D(s) \approx s^4 d'_4 + s^3 d'_3 + s^2 d'_2 + s d'_1 + d'_0 \quad (14)$$

where

$$d'_4 = C_B C_L C_a C_s \quad (15)$$

$$d'_3 = g_{m2} C_s C_B (C_a + C_L) + g_{m3} C_a C_B (C_s + C_L) \quad (16)$$

$$d'_2 = g_{m2} g_{m3} C_B (C_a + C_s + C_L) + g_{m4} C_a C_s (g_{m2} + g_{m3}) \quad (17)$$

$$d'_1 = g_{m2} g_{m3} g_{m4} (C_a + C_s) \quad (18)$$

$$d'_0 = R_L^{-1} R_B^{-1} g_{m2} g_{m3} \quad (19)$$

As it is seen from (13), the system has three zeros and four poles. The zeros are simply obtained as follows:

$$s_{z1} = -\frac{g_{m3} + R_C^{-1}}{C_s + C_C} \approx -\frac{g_{m3}}{C_s + C_C} \quad (20)$$

$$s_{z2,3} = -\frac{C_B R_B^{-1} \pm \sqrt{C_B^2 R_B^{-2} + 4C_a C_B g_{m2} g_{m4}}}{2C_a C_B} \approx \pm \sqrt{\frac{g_{m2} g_{m4}}{C_a C_B}} \quad (21)$$

Two zeros are at the left half plane and one is located at the right half plane. But, since the right half plane zero is at a high frequency, it does not affect the system behavior.

To obtain the dominant real pole, it is assumed that its value is much smaller than the other poles. So, it is given by:

$$s_{p1} \approx -\frac{d'_0}{d'_1} = -\frac{1}{g_{m4} (C_a + C_s) R_L R_B} \quad (22)$$

The dominant pole is the same as that of the conventional Miller and cascode compensation schemes with a small difference. The sum of the two compensation capacitors is replaced with one that is used in the Miller and/or cascode

compensations.

Assuming a dominant pole and considering  $|s_{p1}| \ll |s|$ ,  $d'_0$  will be negligible and the denominator of (14) becomes:

$$D(s) \approx s^4 d'_4 + s^3 d'_3 + s^2 d'_2 + s d'_1 \quad (23)$$

To derive the second real pole, it is assumed that its value is much smaller than the other two non-dominant poles. Hence, the value of the second real pole will be obtained as follows:

$$\begin{aligned} s_{p2} &\approx -\frac{d'_1}{d'_2} \\ &= -\frac{g_{m2}g_{m3}g_{m4}(C_a + C_s)}{g_{m2}g_{m3}C_B(C_a + C_s + C_L) + g_{m4}C_a C_s(g_{m2} + g_{m3})} \\ &\approx -\frac{g_{m2}g_{m3}(C_a + C_s)}{C_a C_s(g_{m2} + g_{m3})} \end{aligned} \quad (24)$$

Therefore, the other two non-dominant poles are obtained as follows:

$$\begin{aligned} s_{p3,4} &= -\frac{d'_3 \pm \sqrt{d_3'^2 - 4d'_2 d'_4}}{2d'_4} \\ &= -\frac{g_{m2}C_s(C_a + C_L) + g_{m3}C_a(C_s + C_L)}{2C_L C_a C_s} \\ &\quad \pm j\sqrt{\frac{g_{m4}(g_{m2} + g_{m3})}{C_B C_L}} \end{aligned} \quad (25)$$

## 2.2 Conventional Cascode Compensation

For the conventional cascode compensation, i.e. when only the  $C_a$  capacitors are used in Fig. 1, the open loop poles and zeros are obtained similar to the used approach for the hybrid cascode compensation and the following results are obtained:

$$s_{p1} = -\frac{1}{g_{m4}C_a R_L R_B} \quad (26)$$

$$|s_{p2,3}| \approx \sqrt{\frac{g_{m2}g_{m4}}{C_L C_B}} \quad (27)$$

$$s_{z1,2} \approx \pm \sqrt{\frac{g_{m2}g_{m4}}{C_a C_B}} \quad (28)$$

## 2.3 Improved Cascode Compensation

Another cascode compensation method that employs the compensating capacitor in a non-signal path which is called the improved cascode compensation has been proposed in [9]. The similar analysis results in the open loop poles and zeros as follows.

$$s_{p1} = -\frac{1}{g_{m4}C_s R_L R_B} \quad (29)$$

$$\begin{aligned} s_{p2,3} &= -\frac{g_{m3}}{2(C_s \parallel C_L)} \\ &\quad \pm 0.5\sqrt{\frac{g_{m3}^2}{(C_s \parallel C_L)^2} - \frac{4g_{m3}g_{m4}}{C_B C_L}} \end{aligned} \quad (30)$$

$$s_{z1} \approx -\frac{g_{m3}}{C_s + C_C} \quad (31)$$

It is worth mentioning that the analysis of the improved cascode compensation has been performed in [10]. But, since  $g_{m3}$  has been considered infinite, the obtained results are inaccurate for a real circuit such as shown in Fig. 1.

## 2.4 Comparison of Open Loop Poles and Zeros of Cascode Compensation Schemes

As it is seen from the above obtained relations, the first pole of all three cascode compensation methods and also the Miller compensation is the same. It is worth mentioning here that the value of the compensation capacitor in a two-stage OTA is determined by its input referred noise budget. In the hybrid cascode compensation scheme the addition of two capacitors are assumed to be equal with a single capacitor that is used in the other compensation methods to achieve the comparable input noise power. So, the value of each capacitor,  $C_a$  and  $C_s$  used in Fig. 1 are sized half that of  $C_a$  and  $C_s$  used in the relations (26)–(31) for the conventional and improved cascode compensations. Hence, if  $C_s = C_a = 0.5C_m$  is assumed in the relations (20)–(25), the poles and zeros of the hybrid cascode compensation as obtained above, are simplified as follows:

$$s_{p1} = -\frac{1}{g_{m4}C_m R_L R_B} \quad (32)$$

$$s_{p2} \approx -\frac{4g_{m2}g_{m3}}{C_m(g_{m2} + g_{m3})} \quad (33)$$

$$\begin{aligned} s_{p3,4} &= -\frac{(g_{m2} + g_{m3})(C_m + 2C_L)}{2C_L C_m} \\ &\quad \pm j\sqrt{\frac{g_{m4}(g_{m2} + g_{m3})}{C_B C_L}} \\ &\Rightarrow |s_{p3,4}| \approx \sqrt{\frac{g_{m4}(g_{m2} + g_{m3})}{C_B C_L}} \end{aligned} \quad (34)$$

$$s_{z1} = -\frac{g_{m3} + R_C^{-1}}{0.5C_m + C_C} \approx -\frac{2g_{m3}}{C_m} \quad (35)$$

$$s_{z2,3} \approx \pm \sqrt{\frac{2g_{m2}g_{m4}}{C_m C_B}} \quad (36)$$

Therefore, the main advantages of the hybrid cascode compensation scheme can be summarized as follows.

1. As it is seen from the above relations, it has one extra zero and pole compared to the conventional cascode compensation. But with considering  $g_{m2} = g_{m3}$  and  $C_a = C_s$  the first zero is cancelled with the second pole and the order of system is reduced to three.
2. The value of its non-dominant poles and also zeros are larger by a factor of about 1.4 compared to the conventional cascode compensation. This results in enhancement of the unity-gain bandwidth of the OTA with the same phase margin as demonstrated by the simulation results in the next section.

3. The first zero of the hybrid cascode compensation is about two times that of the improved cascode compensation. This demands a higher transconductance for the cascode transistor in the improved cascode compensation where its realization can be a main problem to achieve a good settling behavior. In the case of  $g_{m2} = g_{m3}$  and  $C_a = C_s$  the zeros of the hybrid cascode compensation are much greater than that of the improved cascode compensation since the first zero of the hybrid cascode compensation is cancelled with its second pole.

### 3. Simulation Results

To verify the accuracy of the obtained relations for the poles and zeros of the hybrid cascode compensation, an OTA with the structure shown in Fig. 1 was designed using a 0.25  $\mu\text{m}$  BSIM3v3 level 49 mixed-signal CMOS models with HSPICE for a switched-capacitor integrator with sampling and integrating capacitors of 2.5-pF and 5-pF, respectively. The load capacitance was 6-pF and 2.5-pF in the AC open loop and transient closed loop simulations, respectively. The designed device dimensions are shown in Table 1. The common mode input voltage was 0.2 V. The body terminal of all NMOS and PMOS transistors were connected to the  $V_{SS}$  and  $V_{DD}$ , respectively. Table 2 shows the simulated and calculated poles and zeros of the hybrid cascode compensation. In Fig. 3 the open loop frequency response of all three cascode compensation methods is shown. Figure 4 shows the settling performance of all three cascode compensation schemes. A summary of the simulation results is shown in Table 3. In these simulations, equal values for the transistors' dimensions and bias currents have been used except the input transistor sizes of the conventional cascode compensation have been designed to get the same phase margin for both hybrid and conventional cascode compensation circuits and also the input and non-signal path cascode transistors of the improved cascode compensation have been

sized to achieve a better settling performance.

Simulation results show that the hybrid cascode compensation scheme achieves unity-gain bandwidth of about 1.7 times that of the conventional cascode compensation which results in the small settling time. Simulation results of the improved cascode compensation show that its zero is so close to the unity-gain bandwidth which results in a large phase margin and so degraded settling behavior. To improve its settling performance the dimensions of its input and non-signal path cascode transistors, M1 and M3, have been sized about one of sixth and three times those of the hybrid cascode compensation method, respectively. The hybrid cascode compensation also achieves about 3.7-dB DC gain greater than the conventional cascode compensation if both circuits are designed for the same phase margin. The

Table 1 Device sizes and circuit parameters.

Device	(W/L)	$g_m$	Parameter	Value
M1a, M1b	150/0.25	4.45mA/V	$R_A$	2.27 k $\Omega$
M2a, M2b	30/0.25	3.72mA/V	$R_B$	37.6 k $\Omega$
M3a, M3b	60/0.25	3.04mA/V	$R_C$	1.55 k $\Omega$
M4a, M4b	60/0.25	8.54mA/V	$R_L$	2.35 k $\Omega$
M5a, M5b	120/0.25	6.81mA/V	$C_A$	0.35pF
M6a, M6b	50/0.4	5.57mA/V	$C_B$	0.25pF
M7a, M7b	60/0.25	3.1mA/V	$C_C$	0.25pF
M8	100/0.25	5.37mA/V	$C_L$	6pF
			$C_{as}, C_s$	3pF

Table 2 Simulated and calculated poles and zeros values.

Parameter	Simulation	Calculation
$f_{p1}$ (kHz)	37.85	35.2
$f_{p2}$ (MHz)	215.1	177.5
$f_{p3,4}$ (MHz)	976	987.4
$f_{z1}$ (MHz)	195.1	161.3
$f_{z2,3}$ (MHz)	1011	1036

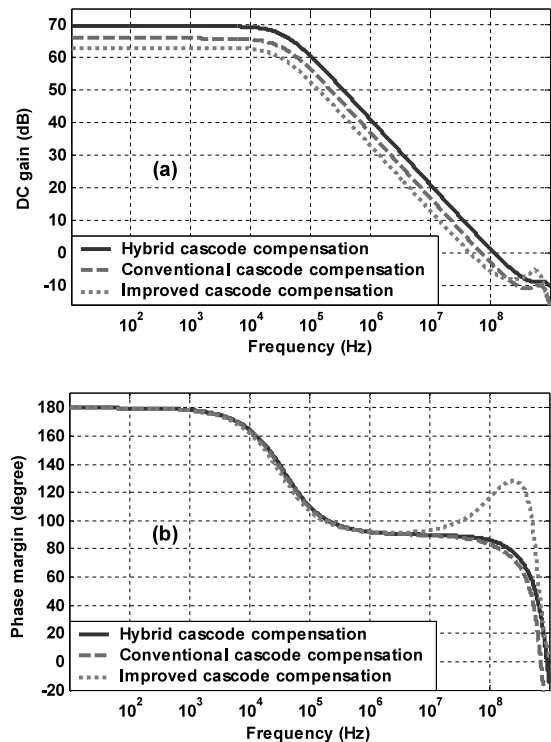


Fig. 3 Frequency response simulation results: (a) DC gain and (b) Phase margin.

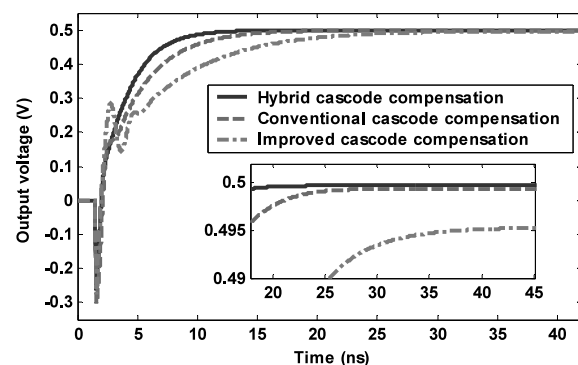


Fig. 4 Settling simulation results.

**Table 3** Simulation results summary.

Parameter	HC	CC	IC
$V_{DD}$	1.5V	1.5V	1.5V
Unity-gain bandwidth	119 MHz	71.6 MHz	47 MHz
Phase margin	85.6 °	85.4 °	103.3 °
DC gain	69.5 dB	65.8 dB	63 dB
0.01% settling time	20.1 ns	26.8 ns	43.2 ns
Power dissipation	5.5 mW	5.5 mW	5.5 mW

HC: Hybrid Cascode  
 CC: Conventional Cascode  
 IC: Improved Cascode

DC gain of the improved cascode compensation is about 6.5 dB less than that of the hybrid cascode compensation due to its small input transistors' transconductance. The slew rate and input referred thermal noise of all three cascode compensation schemes are approximately the same.

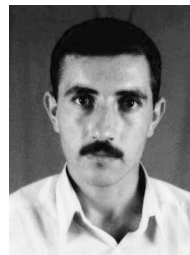
#### 4. Conclusions

In this paper an open loop analysis for the hybrid cascode compensation method has been presented to obtain simple and accurate relations for its poles and zeros. The obtained relations show that the hybrid cascode compensation technique has a large unity-gain bandwidth compared to the conventional cascode compensation with the same phase margin. This results in fast settling in switched-capacitor applications or less power dissipation with the same settling time as demonstrated by the simulation results.

In the case of equal transconductance for the cascode transistors and equal compensation capacitors, i.e.  $g_{m2} = g_{m3}$  and  $C_a = C_s$ , the first zero of the hybrid cascode compensation is cancelled with its second pole. So in this case, the system's order is reduced to three and the zeros and non-dominant poles are greater than those of the conventional cascode compensation by about 1.4 times. The zero of improved cascode compensation is much less than the other two cascode compensation schemes which results in a degraded settling performance.

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