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Low-Voltage Sigma-Delta Modulator Topologies for Broadband Communications Applications

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SUMMARY This paper presents a novel class of sigma-delta modulator topologies for low-voltage, high-speed, and high-resolution applications with low oversampling ratios (OSRs). The main specifications of these architectures are the reduced analog circuit requirements, large out-of-band gain in the noise transfer function (NTF) without any stability concerns to achieve high signal to noise ratio (SNR) with a low OSR, and unity-gain signal transfer function (STF) to reduce the harmonic distortions resulted from the analog circuit imperfections. To demonstrate the efficiency of the proposed modulator architectures a prototype with HSPICE is implemented. A low-power two-stage class A/AB OTA with modified common mode feedback (CMFB) circuit in the first stage is used to implement the fourth order modulator. Simulation results with OSR of 16 give signal to noise plus distortion ratio (SNDR) and dynamic range (DR) of 90-dB and 92.5-dB including the circuit noise in the 1.25-MHz signal bandwidth, respectively. The circuit is implemented in a 0.13-μm standard CMOS technology. It dissipates about 40-mW from a single 1.2-V power supply voltage.

key words: *sigma-delta modulation, low-voltage analog circuits, operational transconductance amplifiers, switched-capacitor circuits, class AB operation, IIR filters*

1. Introduction

Demands for low voltage power supply in mixed-signal designs are growing due to portable equipment capable of operating with minimum number of battery cells to reduce volume and weight with longer operating periods and also voltage limitations resulted from smaller feature sizes of modern IC technologies. Also with the recent developments in both wired and wireless communications, there is a need to design analog-to-digital converters (ADCs) at MHz speeds with high linearity.

Sigma-delta modulators and pipelined ADCs are the two main candidates for high-resolution and high-speed applications. Pipelined converters need some type of calibration or error correction techniques to achieve accuracies beyond 12-bits, resulting in increased complexity and power dissipation [1]. Several sigma-delta ADCs have been reported in the MHz range with resolutions of about 14-bits and beyond [2]–[7]. However, all of them operate on supply voltages greater than 1.8-V. In this paper a novel class of sigma-delta modulator architectures suitable for very low-voltage and high-resolution applications in the MHz ranges is proposed. To show the usefulness of the proposed modulator topologies a prototype is implemented with HSPICE using a 0.13-μm BSIM3v3 level 49 CMOS technology.

Section (2) reviews some sigma-delta modulator architectures and discusses what type of them is suitable for low-voltage applications. The proposed class of modulator architectures is presented in Sect. (3). This section also provides system level design and simulation results. In Sect. (4) the proposed fourth order modulator is implemented in the circuit level. Design of modulator building blocks are described in this section and the simulation results are also presented. Section (5) concludes the paper.

2. Modulator Topologies

The main sigma-delta modulator topologies are classified as single-loop and cascaded architectures [8]. Cascaded architectures use combination of inherently stable first and second order modulators to achieve higher order noise shaping. But, they need high dc gain opamps to implement the used integrators to prevent the quantization noise leakage of the first stage ADCs which limit their usefulness in the low-voltage applications [4], [5]. Single-loop modulators demand lower dc gain opamps. Besides, their other circuit requirements are more relaxed compared to their cascaded counterparts at the expense of being more prone to instability and reduced signal-to-noise ratio. In order to guarantee the stability in single-loop modulators, their NTFs must provide a low out-of-band gain [9]. This, in turn, results in a low SNR. Another concern in sigma-delta modulators is the distortions resulted from the circuit non-idealities such as opamp finite dc gain. In [10] it has been proven that the distortions caused by circuit non-idealities can be greatly reduced by setting the STF gain at unity.

Both single-loop and cascaded architectures can utilize either single-bit or multibit quantizers. In the design of sigma-delta modulators for high-speed applications a low oversampling ratio (OSR) must be used where this weakens the advantages of oversampling. To compensate for this loss in resolution a high order with a multibit modulator can be used. It worth to mention that the impact of increasing the modulator order on the dynamic range (DR) diminishes as the oversampling ratio is reduced. In contrast, the effectiveness of increasing the internal quatizer resolution (using a multibit modulator) is independent of the OSR. Each extra bit of quantizer increases the modulator resolution about one bit independent of OSR. The other advantages of multi-

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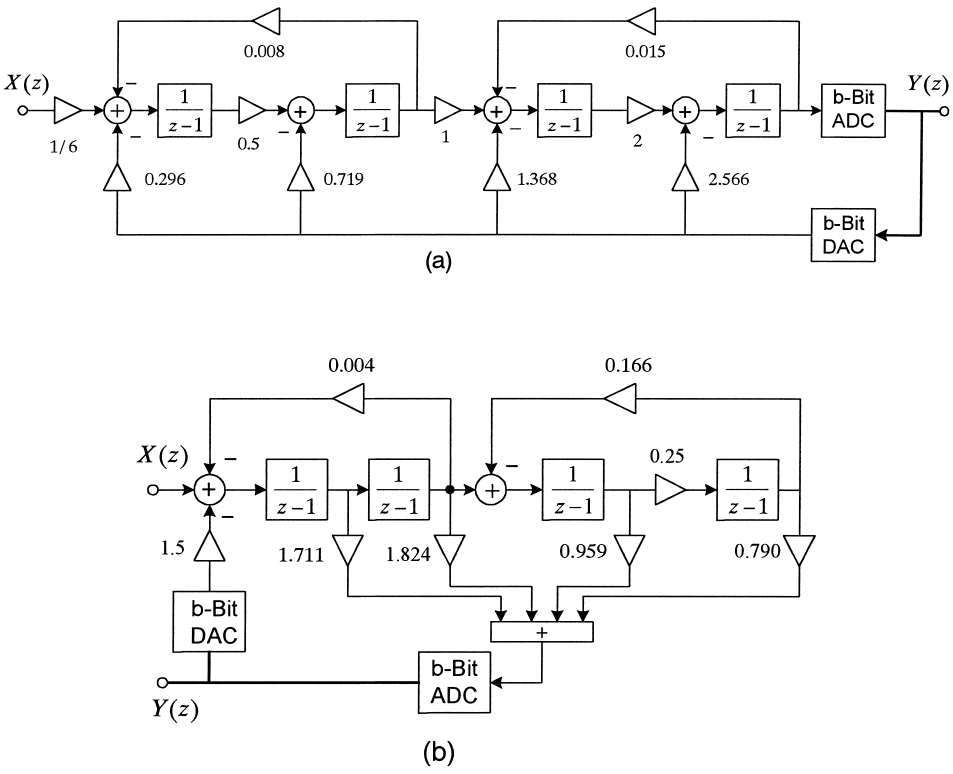

Fig. 1 Fourth single-loop sigma-delta modulators with (a) distributed feedback, (b) weighted feedforward architectures.

bit quantization include reduced analog circuit requirements such as the OTA settling and enhanced modulator stability especially in high order single loop architectures. Multibit quantization improves the modulator stability and its input signal range. With multibit quantization one can achieve aggressive noise shaping and/or wide input signal range in high order modulator structures compared to their single bit quantization counterparts [11], [12]. However, errors due to non-idealities in the feedback DAC add directly to the input signal and hence are not shaped by the modulator. Thus, the resolution of a multibit modulator is limited by the linearity of its multibit DAC unit elements. The matching of the DAC unit elements can be improved by special fabrication processes or laser trimming. But these techniques are expensive and time consuming. Two signal processing techniques have been developed to correct the DAC non-idealities: dynamic element matching (DEM) and calibration or correction.

Calibration of a multibit sigma-delta modulator requires the measurement and compensation of the feedback DAC errors [13]. However, the complexity of these techniques is larger than the DEM techniques. Dynamic element matching such as data weighted averaging (DWA) selects different DAC unit elements to represent a given digital code at different times; thereby translating the element mismatch from a dc error into a wideband high-pass shaped noise [14]. This shaped mismatch noise can be filtered out by the decimation filter following the modulator. The main drawback of DWA is introduction of the harmonic distortions. Some techniques have been proposed to alleviate this problem of DWA such as bi-directional data weighted averaging (BDWA) [4] at the cost of increasing the noise floor. In this paper both DWA and BDWA are used to correct the DAC errors.

The two well-known high order single-loop modulators are distributed feedback (DFB) and weighted feedforward (WFF) architectures with local resonators [8], [15]–[17]. Figure 1 shows their fourth order modulator structures. By adding a small negative feedback around pairs of integrators it is possible to move the NTF's zeros from dc to inband frequencies. This causes the inband frequencies of infinite noise attenuation and hence improves the modulator's SNDR. This technique is more useful in the wideband applications to enhance the accuracy compared to the low bandwidth counterparts. In order to have the NTF's zeros at a non-zero frequency one of the integrators must have a sample delay and the other no delay. A slightly less effective resonator can be built with both one sample delaying integrators as shown in Fig. 1. It is worth to mention that the switched-capacitor (SC) implementation of delaying integrators is somewhat simpler and does not require double opamp sampling. Both these architectures can implement inverse Chebyshev NTFs which results in higher SNR compared to their Butterworth counterparts [8].

One drawback of the DFB topology shown in Fig. 1(a) is that the integrators output contain significant amount of the input signal as well as the shaped quantization noise. In SC implementations, the output swings must be limited

to stay within the available supply range by proper scaling of the modulator coefficients. This results in large modulator coefficients spread and small integrators gain. Small integrator gain increases the integrating capacitance because the sampling capacitor is determined by kT/C noise and/or matching requirements. So, the circuits used in distributed feedback topologies tend to be larger and more power hungry than those needed for the feedforward topologies. Similarly, large coefficients spread results in large capacitor requirement.

Stability is the main concern in the design of high order single loop modulators which relates to the NTF's out-of-band gain directly. Increasing the modulator's NTF's out-of-band gain enhances its resolution at the cost of degradation of its stability likelihood. On the other hand, reducing NTF's out-of-band gain increases the likelihood of success, but reduces the magnitude of the quantization noise attenuation provided by NTF and thus the theoretical resolution of the modulator. As a rule of thumb proposed by Lee [9] a modulator with NTF's out-of-band gain less than 2 should yield a stable modulator with a single bit quantizer. This is not true for modulator orders higher that three as demonstrated in [18] and is also more conservative for second order structure. A more rigorous justification of stability test proposed in [19] uses first norm of NTF's impulse response to judge the stability condition. According to this test none of the stable modulators were been explored in [18] pass the stability condition. So, as proposed in [18] in this paper computer simulations are also used to design stable modulators with aggressive noise shaping.

In order to compare the proposed modulator architectures with conventional single loop structures introduced in this paper several simulation results were provided. Fourth order DFB and WFF modulator architectures were designed using Schreier's Delta-Sigma toolbox [20] for both optimal wide input signal range and high NTF's out-of-band gain. Their NTF's out-of-band gain was considered 12 dB which results in stable input range of −4.2 dBFS and −3.2 dBFS, for DFB and WFF structures, respectively. Figure 2 shows the dynamic range (DR) of the designed fourth order DFB and WFF modulators. The resultant maximum SNDR are 94 dB and 98 dB for DFB and WFF architectures, respectively. Modulators coefficients after signal scaling are shown in Fig. 1 for OSR=16 and $b = 4$. The integrators output were scaled within the 75% of the feedback reference levels to ensure the implementation capability with actual

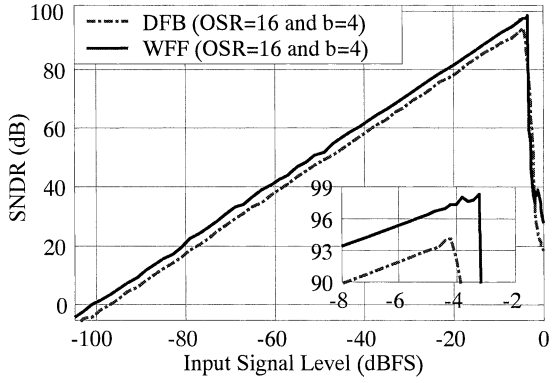

Fig. 2 Dynamic range: SNDR versus input signal level of conventional fourth order DFB and WFF single loop modulators.

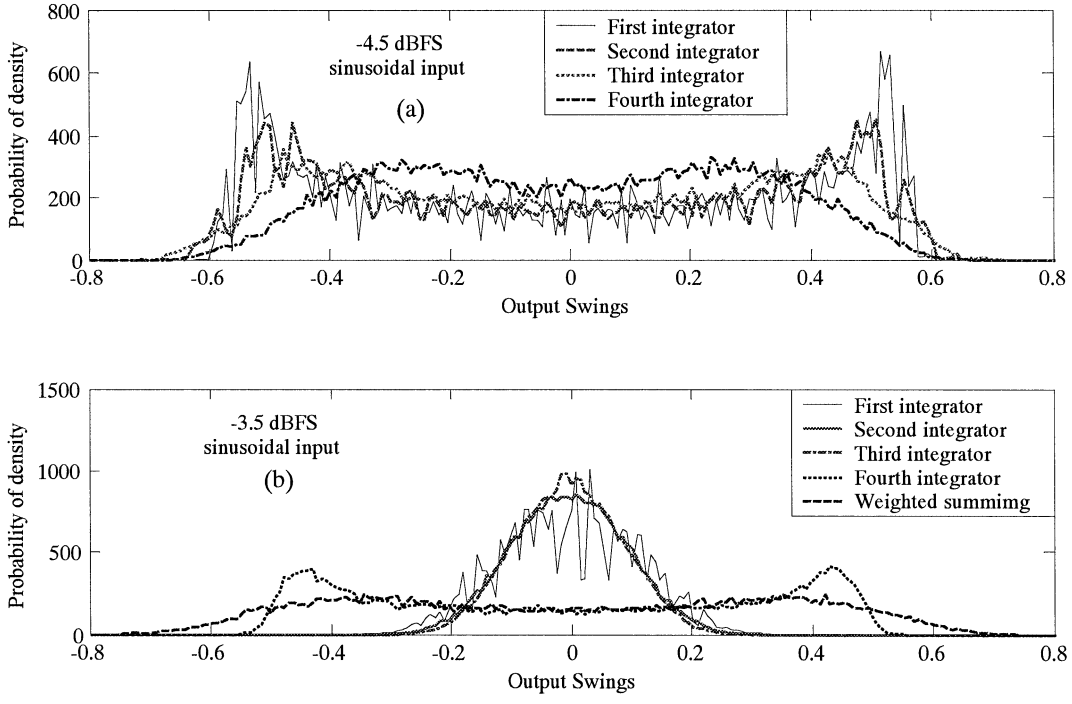

Fig. 3 Histogram of the integrators output swing: (a) distributed feedback and (b) weighted feedforward architectures.

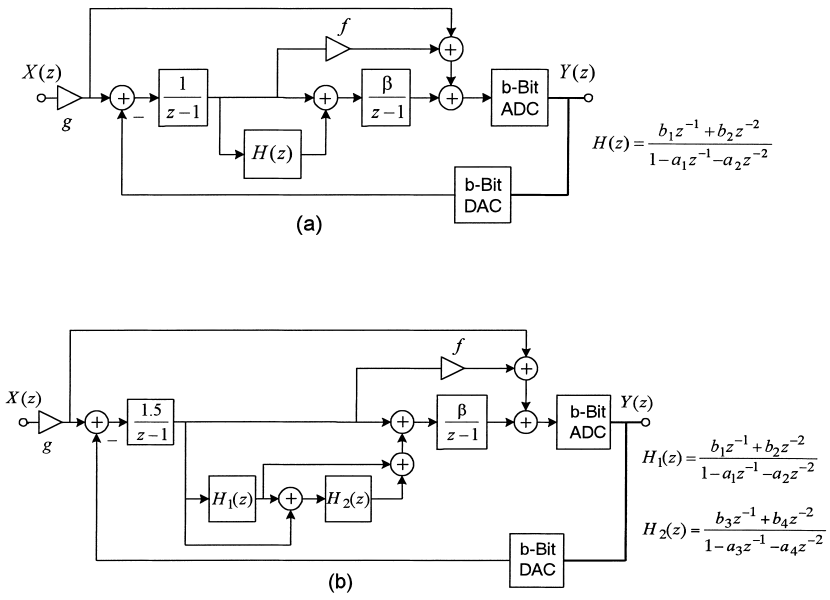

Fig. 4 The proposed (a) fourth order and (b) sixth order sigma-delta modulator topologies.

circuits. In Fig. 3 the histogram of integrators output swing for a sinusoidal input signal are shown. The main drawbacks of the DFB and WFF architectures are as follows:
1) One of the aggressive noise shaping and wide input signal range can be obtained only by using the multibit quantization.
2) Large integrators output swing which demands large swing OTAs for implementation.
3) High modulator coefficients spread: this is 321 for DFB and 456 for WFF structures. As will be discussed in the next section the coefficients spread of the proposed fourth order architecture is less than 8. High coefficients spread not only leads to more power and area consumption, but it is also an indication of high coefficient sensitivity and poor stability.

Another high order single loop modulator architecture proposed in [21] uses FIR based NTF to achieve aggressive noise shaping. This architecture can have a high NTF's out-of-band gain which enhances its noise shaping ability. But, it has some main drawbacks. First, its aggressive noise shaping is a result of using multibit quantization, not the modulator architecture. So, this modulator structure is instable for single bit quantization. Also, according to our simulation results its fourth order structure is stable only with a quantizer greater than three bits and its input signal range is very small with a four bit quantizer. Second, it uses both delaying and non-delaying integrators. Non-delaying integrators need longer time period to settle compared to delaying integrators for the same accuracies. Third, it has large coefficients spread.

3. Proposed Topologies

The proposed single loop modulator architectures in this paper can have aggressive noise shaping with wide input signal range that have not been possible using the previously reported high order single loop structures. Also, the needed circuits for implementation of the proposed architectures are more relaxed compared to the existing single loop architectures.

Figure 4 shows the proposed fourth and sixth order modulator topologies, where f is the gain of a feedforward path, g and β are the gains of the first and last integrators, respectively, and $H(z)$ is an infinite impulse response (IIR) filter with the following transfer function:

$$H(z) = \frac{b_1 z^{-1} + b_2 z^{-2}}{1 - a_1 z^{-1} - a_2 z^{-2}}. \quad (1)$$

It is worth to mention that the order of the modulator can be extended to even higher orders with a straightforward extension. For example the eighth order will use three IIR filters with two integrators.

The main features of the proposed modulator architectures are as follows. 1) Using IIR filters instead of conventional integrators in the middle of modulator architecture to implement an aggressive noise shaping NTF. Only two integrators are used: one at the input and the other at the end. 2) Unity gain STF to reduce the imperfections resulted from analog circuits non-idealities and eliminate the drawbacks resulted from phase nonlinearity of IIR filters and also to extend the stable input signal range to enhance the modulator's dynamic range. 3) Low output swing integrators and IIR blocks. 4) Simple relation between noise transfer function and its zeros. 5) Very low coefficients spread compared to the existing high order single loop modulators.

In the proposed architectures IIR filters are used to achieve a high out-of-band gain in the modulator's NTF similar to [2], resulting in aggressive noise shaping and hence the increased SNR and reduced tones at the modulator's output spectrum without any concern to instability. The major concern to select IIR filters in sigma-delta modula-

tors is their nonlinear phase properties which results in harmonic distortion particularly notable at the presence of two strong tones at the modulator's input. In the proposed architectures, the phase nonlinearity was resolved making use of a unity-gain STF. Choosing a unity-gain STF not only reduces the harmonic distortions resulted from analog circuit imperfections such as finite dc gain opamps [10] but also the integrators and IIR blocks process only quantization noise which results in low output swing integrators and IIR blocks. Also unity gain STF extends the modulator's dynamic range through a direct path to the quantizer input. Simulation results indicate that about 4-dB improvement in DR is achieved by making the STF gain at unity. The proposed architectures use only one DAC which greatly reduces the circuit complexity at low-voltage applications. The forward paths terminated to the input of quantizer can be implemented using a passive switched-capacitor circuit as proposed in [10]. But, it can reduce the least significance bit (LSB) of quantizer whose design can be very complex in very low-voltage applications. Unlike the DFB modulator structure, the quantizer input in the proposed architectures senses input signal from two another lower delay paths: one directly and another through the f feedforward path. This causes that the quantizer senses the input signal jumps directly and stabilizes the modulator through the negative feedback fast, hence to enhance the modulator dynamic range.

It can be shown that the NTF of the proposed fourth and sixth order modulators are as follows:

$$H_{Q4}(z) = \frac{(z-1)^2(z^2 - a_1 z - a_2)}{z^4 + d_3 z^3 + d_2 z^2 + d_1 z + d_0} \tag{2}$$

$$d_3 = -a_1 + f - 2 \tag{3}$$

$$d_2 = -a_2 + 2a_1 + \beta - f a_1 + 1 - f \tag{4}$$

$$d_1 = 2a_2 - a_1 - \beta a_1 + \beta b_1 - f a_2 + f a_1 \tag{5}$$

$$d_0 = -a_2 - \beta a_2 + \beta b_2 + f a_2 \tag{6}$$

$$H_{Q6}(z) = \frac{(z-1)^2(z^2 - a_1 z - a_2)(z^2 - a_3 z - a_4)}{z^6 + d_5 z^5 + d_4 z^4 + d_3 z^3 + d_2 z^2 + d_1 z + d_0} \tag{7}$$

$$d_5 = -(a_1 + a_3 + 2) + 1.5f \tag{8}$$

$$d_4 = 1 + (2 - 1.5f)(a_1 + a_3) - (a_2 + a_4 - a_1 a_3) - 1.5f + 1.5\beta \tag{9}$$

$$d_3 = (2 - 1.5f)(a_2 + a_4 - a_1 a_3) + (a_1 a_4 + a_2 a_3) + (1.5f - 1.5\beta - 1)(a_1 + a_3) + 1.5\beta(b_1 + b_3) \tag{10}$$

$$d_2 = a_2 a_4 + (1.5f - 2)(a_1 a_4 + a_2 a_3) + (1.5f - 1.5\beta - 1)(a_2 + a_4 - a_1 a_3) + 1.5\beta(b_2 + b_4 - b_1 a_3 - a_1 b_3 + b_1 b_3) \tag{11}$$

$$d_1 = (1 + 1.5\beta - 1.5f)(a_1 a_4 + a_2 a_3) + a_2 a_4(1.5f - 2) + 1.5\beta(b_2 b_3 + b_1 b_4 - b_1 a_4 - b_2 a_3 - a_1 b_4 - a_2 b_3) \tag{12}$$

$$d_0 = a_2 a_4(1 + 1.5\beta - 1.5f) + 1.5\beta(b_2 b_4 - a_2 b_4 - a_4 b_2) \tag{13}$$

Table 1 Simulated modulators coefficients.

Sixth order modulator coefficients					
a1	a2	b1	b2	f	g
1.937	-1	0.580	-0.500	2.539	0.5
a3	a4	b3	b4	β	
1.868	-1	0.288	-0.102	4.203	

Fourth order modulator coefficients						
a1	a2	b1	b2	β	f	g
1.973	-1	0.531	-0.406	3.184	2.893	0.5

where $H_{Q4}(z)$ and $H_{Q6}(z)$ are the NTFs of proposed fourth and sixth order modulators, respectively. To obtain the modulators coefficients MATLAB with Schreier's Delta-Sigma toolbox [20] was used. Sixth and fourth order modulators were designed with OSR=8 and $b = 5$ and OSR=16 and $b = 4$, respectively. It is worth to mention here that the OSR and number of quantizer bits were selected arbitrary to show the efficiency of proposed modulators. Designed modulators' NTFs for fourth and sixth order architectures are as follows:

$$H_{Q4}(z) = \frac{(z-1)^2(z^2 - 1.973z + 1)}{z^4 - 1.080\,z^3 + 0.530\,z^2 + 0.035\,z + 0.022} \tag{14}$$

$$H_{Q6}(z) = \frac{(z-1)^2(z^2 - 1.937z + 1)(z^2 - 1.868z + 1)}{D(z)}$$

$$D(z) = z^6 - 1.996\,z^5 + 2.231\,z^4 - 1.467\,z^3 + 0.671\,z^2 - 0.179\,z + 0.030 \tag{15}$$

Table 1 shows the modulators coefficients which were obtained with solving the equations (2–15) with MATLAB. Figure 5 shows the output spectrum of the proposed fourth and sixth order modulators. The resultant maximum SNDR's are 103-dB and 101-dB for the sixth and fourth order modulators, respectively. The NTF's out of band gain of designed modulators is about 18-dB and 16-dB for the sixth and fourth order architectures, respectively, as opposed to the conventional single-loop DFB and WFF modulators designed in this paper that is about 12-dB as shown in Fig. 6.

In Fig. 7 SNDR versus input signal level of the proposed modulators is shown. The resultant DR's are 102 dB and 103 dB for the fourth and sixth orders, respectively. The overload level factor of the sixth order is above 0-dBFS where the fourth order is stable for input signals about 1.5 dB higher than the feedback reference levels. This is due to a direct path from the input signal to the quantizer input which results in a wide input signal range.

Figure 8 shows the histogram of the building blocks output swing of the proposed fourth and sixth order modulators. The proposed architectures have small output swings compared to the DFB and WFF architectures as shown in Figs. 3 and 8. Also the coefficients spread of the proposed architectures as shown in Table 1 is much less than the conventional DFB and WFF structures.

Figure 9 shows the SNDR degradation versus mis-

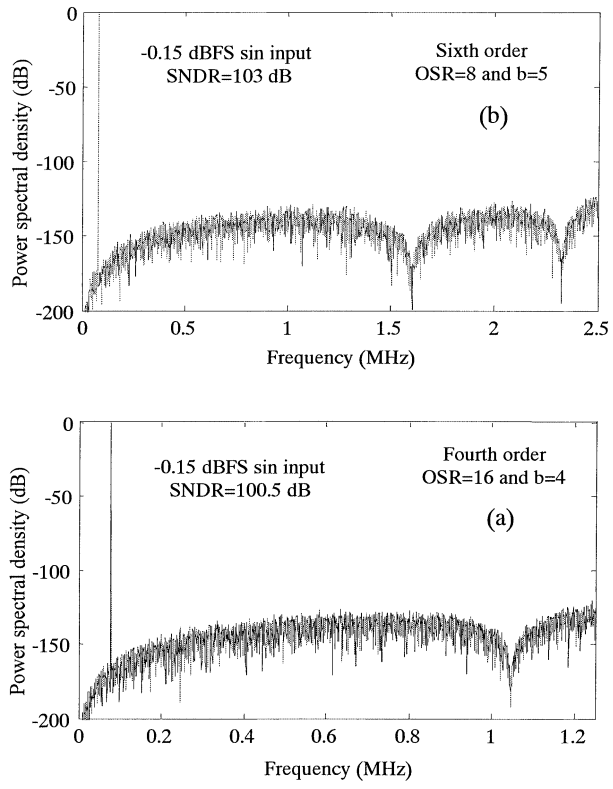

Fig. 5 Output power spectral density of the proposed (a) fourth order and (b) sixth order modulators.

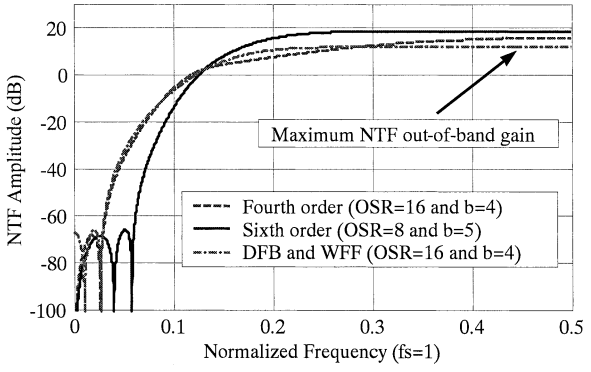

Fig. 6 Noise transfer function amplitude of the proposed, conventional DFB and WFF modulators.

match error of modulator coefficients. To obtain this plot the modulator coefficients were considered independent Gaussian random variables with mean values shown in Table 1 and variances as a variable indicating the mismatch error. The mismatch was considered as three time of standard deviation of these Gaussian random distributions. For each mismatch value two hundred simulations were performed and average SNDR was considered. As shown in Fig. 8 SNDR degradation is negligible with coefficient mismatches less than 1% which is well achievable with existing modern CMOS technologies. In these simulations ideal DAC elements have been used. In order to account the DAC errors in the simulations a mismatch of 0.1% between DAC unit elements was considered. This matching requirement can be achieved using large capacitors for DAC arrays. It is worth to mention that only one DAC is used in the proposed modulators and it is located at the input of first integrator. The values of sampling and feedback capacitors of this integrator are determined due to kT/C noise considerations and their sizes are large in the high-resolution applications. Figure 10 shows the effect of DAC mismatch errors on the proposed modulators performance. The SNDR degradation is about 18.5-dB and 15-dB for the fourth and sixth order modulators, respectively. Also strong tones appeared at the outputs which greatly decreases the SFDR. Both DWA and BDWA were used to compensate this degradation. As shown in Fig. 10 the loss of SNDR is at most 1-dB and 3.5-dB using DWA DAC linearization technique for fourth and sixth orders and the tones are removed nearly completely. Figure 11 shows SNDR degradation versus the DAC mismatch errors including the effects of DWA and BDWA on the correction of DAC errors.

The other circuit requirements of the proposed architectures such as amplifier finite dc gain are more relaxed and simulation results show that the 40 dB dc gain for the first integrator as shown in Fig. 12 is sufficient to prevent any SNDR degradation with enough margin.

4. Modulator Design Prototype

To demonstrate the efficiency of the proposed sigma-delta modulator architectures a design prototype is implemented with HSPICE. The fourth order modulator shown in

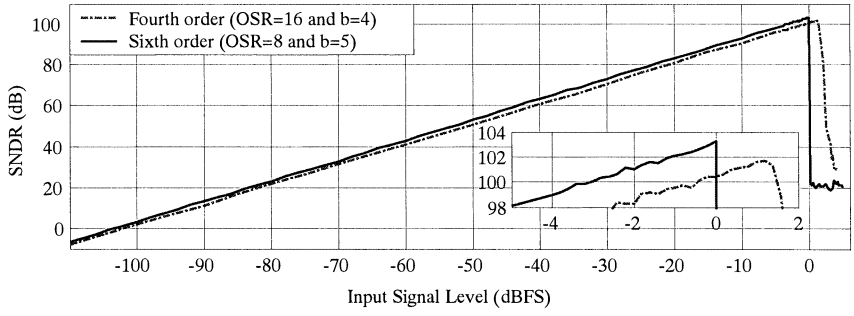

Fig. 7 Dynamic range: SNDR versus input signal level of the proposed modulators.

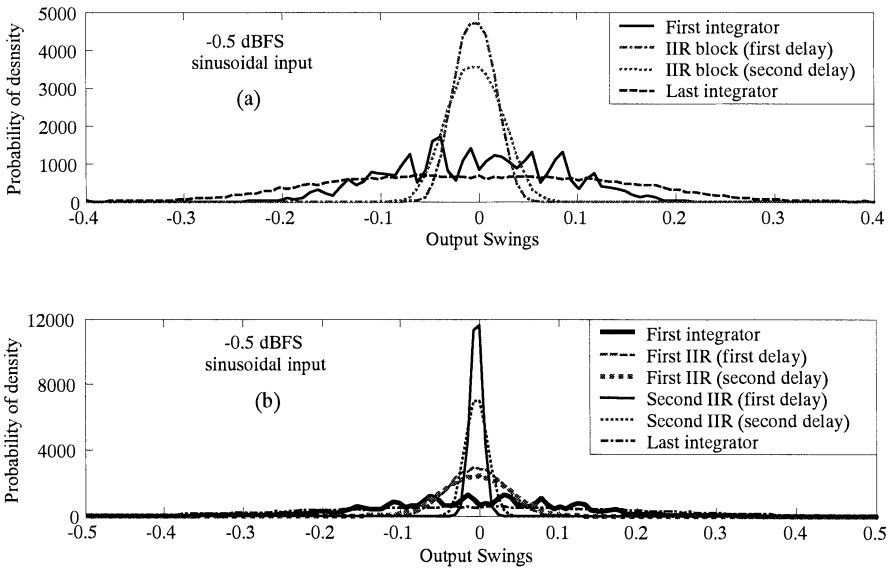

Fig. 8 Histogram of the integrators output swing: (a) fourth order and (b) sixth order architectures.

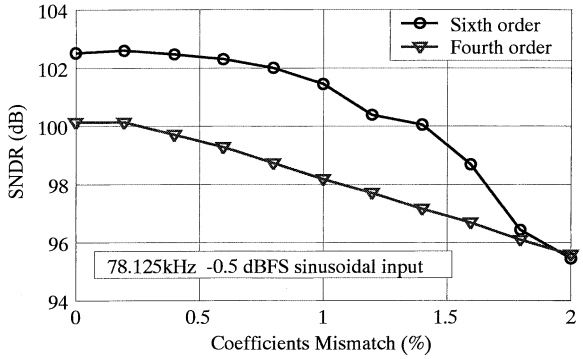

Fig. 9 SNDR versus the modulators coefficients mismatch errors.

Fig. 4(a) was designed with OSR=16 and $b = 4$. The modulator coefficients were shown in Table 1. Circuit requirements for implementation of this modulator are presented in this section. The ideal resultant system level maximum SNDR and DR are 101-dB and 102-dB, respectively.

4.1 Operational Transconductance Amplifiers

A fully differential two-stage class A/AB OTA similar to [22], [23] as shown in Fig. 13 is used to implement the required building blocks. This OTA combines a folded-cascode as the first stage with active current mirrors as the second stage. PMOS input differential pair allows the use of near ground op-amp common mode input, V_{cmi}. This, in turn, allows the use of relatively small NMOS transistors to design the switches that are connected to V_{cmi}. The second stage is a class AB amplifier with active current mirrors. Due to class AB operation of this stage, slew limiting only occurs in the first stage. So, the second stage currents are chosen so that the non-dominant poles are sufficiently high in frequency to ensure stability. Because of push-pull operation, the lowest non-dominant pole in the class A/AB design is governed by the time constant formed by approximately the addition of trans-conductance of the output transistors, M9 and M11, and the parasitic capacitances seen at the first stage output [24]. Thus the output branch current can be about half that used in the two-stage class A circuit for the same non-dominant pole frequency. When this fact is exploited together with the use of gain in the second stage current mirrors, a significant reduction in power dissipation can be achieved relative to the two-stage class A topology. However, the mirror pole and zero will eventually degrade the phase margin of the circuit. To increase the mirror pole and zero frequencies in the active current mirrors NMOS current mirrors with a low current gain are used in this design. The two-stage amplifier shown in Fig. 13 employs the cascode compensation scheme which creates one dominant pole and two complex poles at a higher frequency with two high frequency zeros in a closed-loop configuration [24], [25]. This scheme of compensation yields a higher amplifier bandwidth compared to the standard miller compensation at the cost of more complex design procedure for the settling behavior of the amplifier.

Common-mode feedback (CMFB) circuit is required in fully differential amplifiers to define the voltages at the high-impedance output nodes. The CMFB circuit of the first stage has been replaced by the cross-coupled connection of transistors M7a, M7b, M8a, and M8b similar to [26]. The conductance seen at the gate of transistors M8a and M8b is cancelled by the opposite action of the parallel transistors M7a and M7b, respectively. This positive feedback connection causes the differential signal at the output of the first stage to see a high load impedance. On the other hand for the common mode signal, the output conductance is limited by $g_{m7} + g_{m8}$. This is a low impedance and thus the first stage does not require an additional CMFB circuit. For the second stage a simple switched-capacitor CMFB circuit is used.

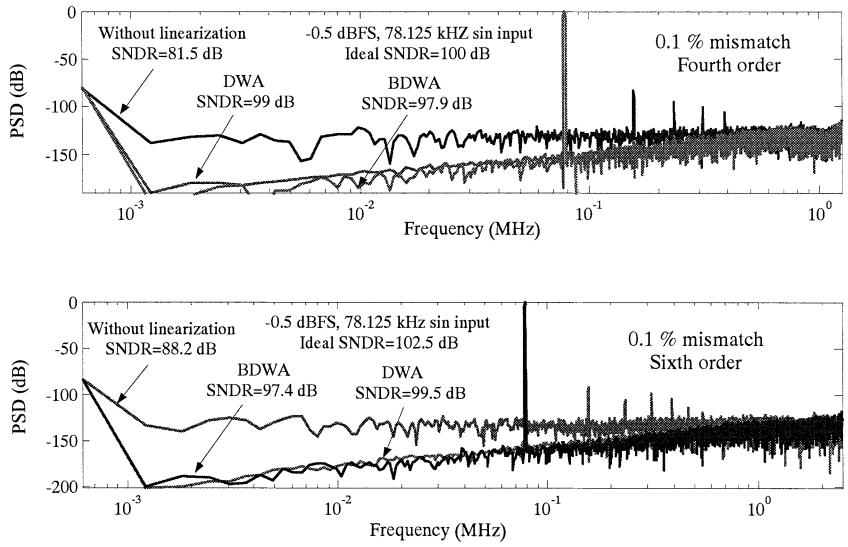

Fig. 10 DAC errors effect on SNDR and its linearization with DWA and BDWA.

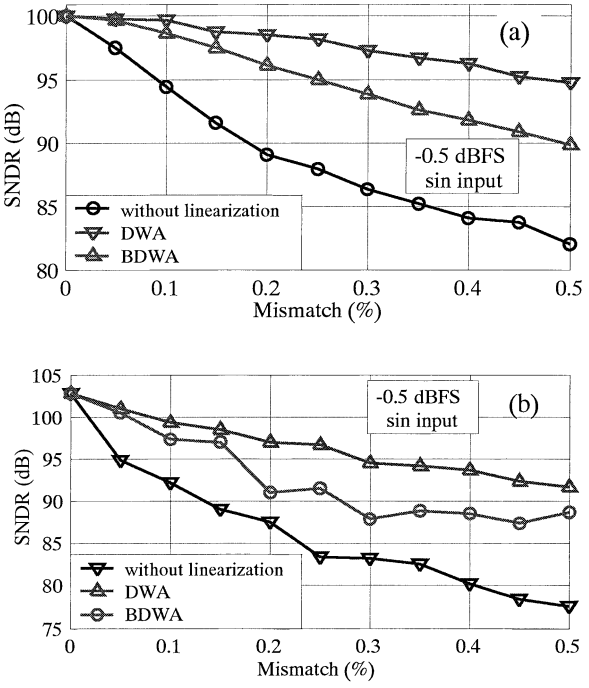

Fig. 11 SNDR versus DAC mismatch errors of the proposed (a) fourth and (b) sixth order modulators.

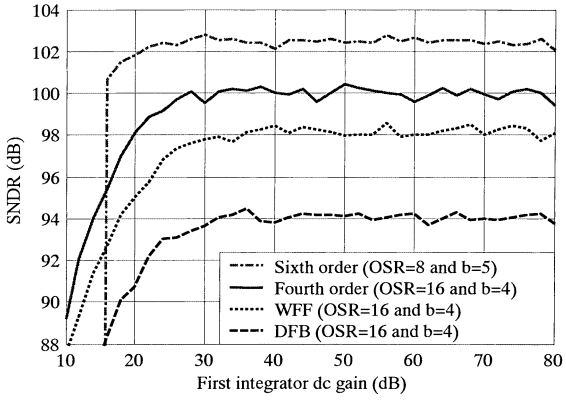

Fig. 12 SNDR versus the first integrator dc gain.

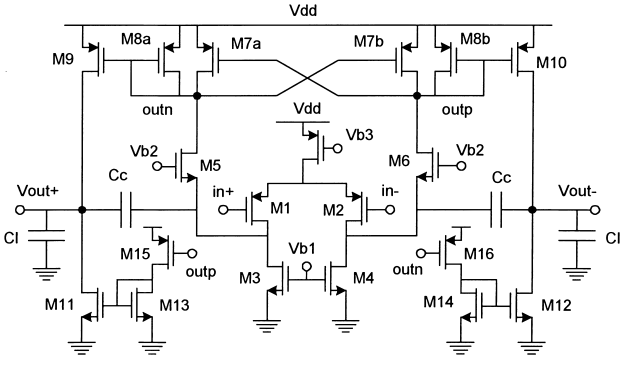

Fig. 13 Fully differential two-stage class A/AB OTA.

4.2 First Integrator and DAC

Figure 14 shows the circuit employed to implement the first integrator and DAC. It uses 16 parallel sampling and feedback capacitors for each positive and negative input branches. During phase ϕ_1 the input signal is stored on sampling capacitors, C_{s1-s8}, while capacitors C_{f1-f8} are connected to the OTA common mode voltage, V_{cmo}. During the next phase, ϕ_2, capacitors C_{s1-s8} transfer the stored charge to the integrating capacitor, C_{I1}. Also during this phase one plates of the capacitors C_{s1-s8} and C_{f1-f8} connects to negative or positive reference voltages depending on the value of quantizer output bits, D1-D16, and transfer the charge to the integrating capacitor, hence these capacitors implement the multibit DAC. Each of these capacitors is selected to be 0.5-pF which results in a kT/C input referred noise of −95.7 dB in room temperature. So, the SNDR due to

kT/C noise becomes about 94.3 dB. The value of integrating capacitor is 8-pF, so, the gain of half and one in the input signal branch and feedback path are implemented, respectively. To decrease the kT/C noise the feedback voltage references are placed on negative and positive power supply voltages, i.e. 0 and 1.2-V. Switches that are connected in one side to input common mode voltage are implemented as simple NMOS transistors while the switches have rail to rail operation use bootstrapping technique as proposed in [27]. The other switches employ CMOS configuration. To avoid the modulator performance degradation due to the DAC capacitor mismatches data weighted averaging (DWA) is used [14].

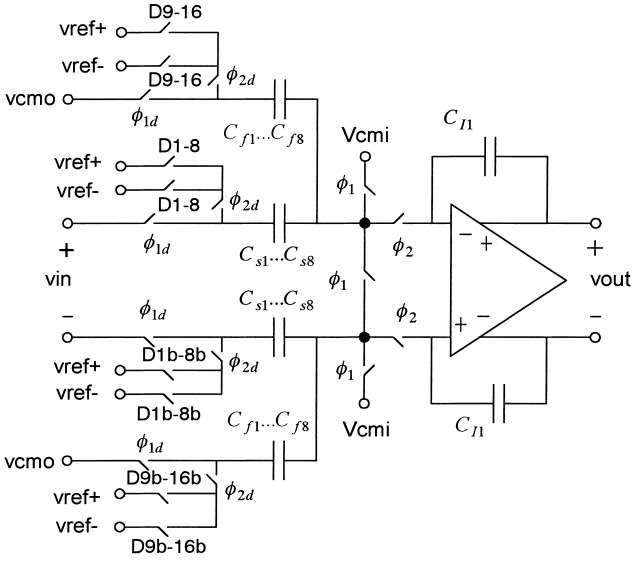

Fig. 14 First integrator and DAC circuit.

4.3 IIR Filter Implementation

IIR blocks use analog delays instead of integrators which can be implemented with a generic low-Q biquad architecture as shown in Fig. 15. It can be shown that its transfer function is as follows:

$$H(z) = \frac{V_{out}(z)}{V_{in}(z)} = \frac{\frac{C_3}{C_{f2}}z^{-1} - \frac{C_1}{C_{f1}}z^{-2}}{1 - \frac{C_4 + C_{f2}}{C_{f2}}z^{-1} + \frac{C_2}{C_{f1}}z^{-2}} \tag{16}$$

4.4 Comparators

Figure 16 shows the comparator circuit used to implement the 4-bit ADC. It uses a preamplifier to reduce its input offset voltage and two regenerative latches to speed up its conversion [28]. This circuit operates as follows. During phase ϕ_1, the differential input signal is amplified by PMOS input differential pair, M1 and M2. The transistors M3 and M4 are operated in linear region as load resistors. During the

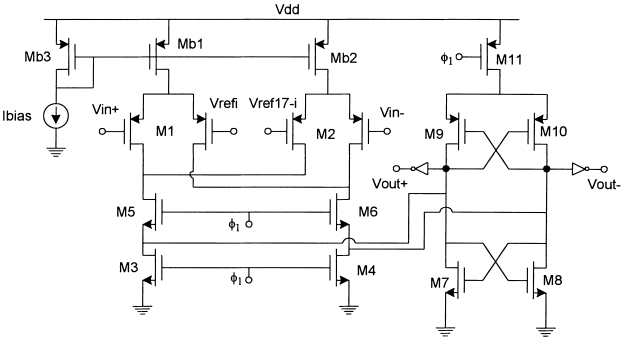

Fig. 16 Comparator circuit.

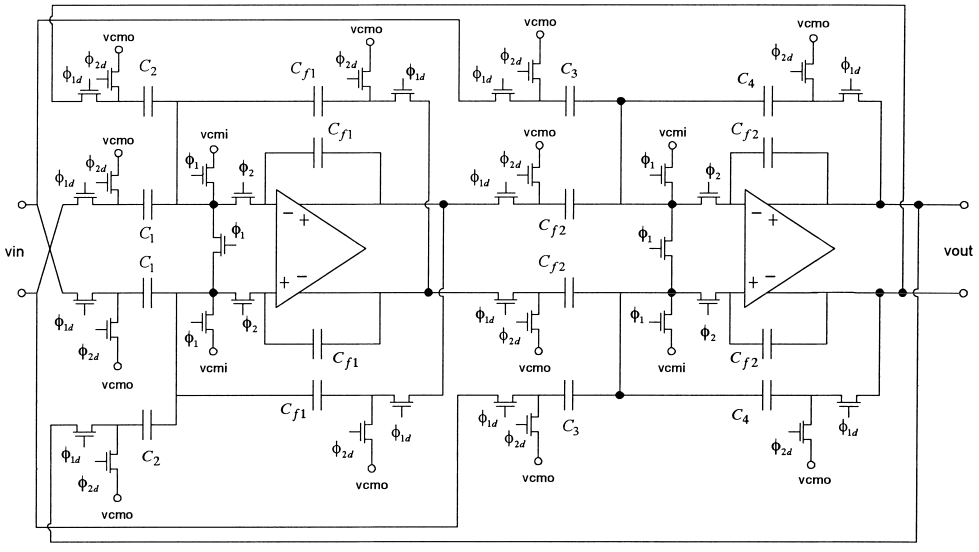

Fig. 15 IIR filter circuit.

next phase, ϕ_2, the non-overlapping version of ϕ_1, the output nodes are disconnected from the drain of input transistors and the triode resistors are also switched off. The PMOS latch starts to regenerate the voltage difference at the output nodes, and then NMOS latch start to help PMOS latch to enhance the regeneration speed. Transistors M5 and M6 are used to reduce the kickback noise from the output nodes to the inputs of comparator. In order to reduce the power dissipation of the comparator, the input transistors are switched off during the regeneration phase. Also in the phase ϕ_1 both latches are turned off.

4.5 Flash ADC

A 4-bit flash ADC was used to implement the quantizer. The outputs of the comparators in the flash ADC are inverted and stored in SR latches that are implemented with CMOS NAND gates. The outputs of the SR latches drive NMOS switches connected to the negative reference voltage and PMOS switches connected to the positive reference voltage of digital to analog converter. Two separate ladders are used to generate the reference voltages. The value of ladder resistors is considered to be 100 Ω in order to reduce the feedthrough voltage of input signals to the reference voltages [29], [30].

4.6 Clock Phases

The integrators need a two phase non-overlapping clock and their delays to minimize signal dependent charge injection errors. It is worth to mention that delay is only needed for the falling edge of clocks. So, in order to avoid the wasting of available OTAs' settling time and also the input sampling period, the rising edge of clocks is designed to be the same with a simple circuit shown in [25]. The period of sampling is 25 ns where 88% of it is allocated to sampling and integrating phases. The remaining 12% of clock period is used to separate the different clock edges so as to overlap the phases.

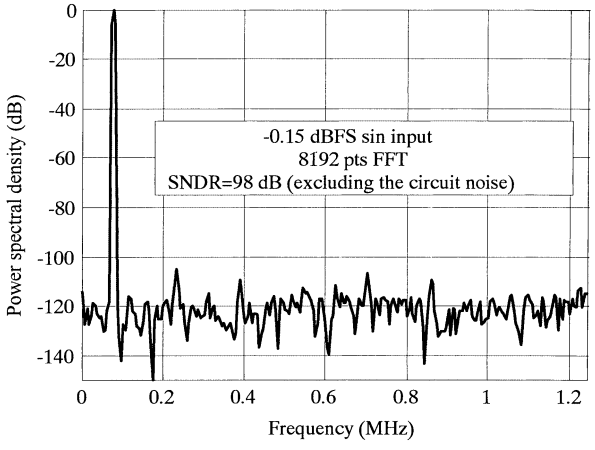

Fig. 17 Power spectral density.

4.7 Simulation Results

The proposed fourth order single loop multibit sigma delta modulator in this paper was simulated in a 0.13-μm standard CMOS technology. The threshold voltages of this process are 0.54 V and −0.56 V for NMOS and PMOS transistors excluding the body effect, respectively. The modulator samples at 40-MHz with 1.25-MHz signal bandwidth with oversampling ratio of 16. All of the simulations were performed with HSPICE including 20% bottom plate parasitic capacitance over −40°C to 85°C temperature variations in all process corners. Plots of SNDR and DR are shown in Figs. 17 and 18 where their resultant values are 90-dB and 91-dB, respectively including the circuit noise. Table 2 summaries the performance of the simulated modulator. It is worth to mention that the modulator's power spectral delay shown in Fig. 17 does not include the circuit noise, showing 98 dB due to only quantization noise. Also SNDR's due to the switches thermal noise and OTA's input referred noise are 94-dB and 96-dB, respectively. So, the overall SNDR including all of

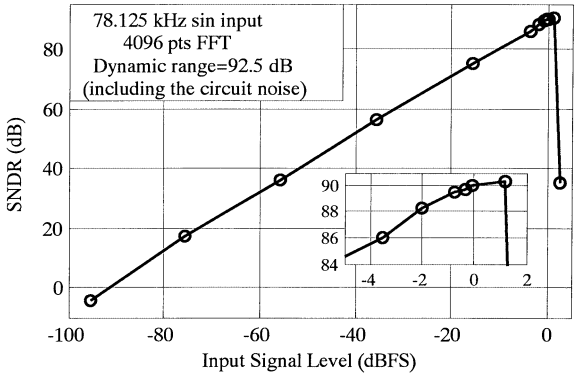

Fig. 18 Dynamic range.

Table 2 Simulated modulator performance summary.

Parameter	Value
Dynamic range	92.5 dB
Peak SNDR	90 dB
Overload level factor	+1.2 dBFS
Sampling rate	40 MHz
OSR	16
Signal bandwidth	1.25 MHz
Power supply voltage	1.2 V
Total power consumption	40 mW
First integrator	11 mW
IIR block	10 mW
Fourth integrator	5 mW
Gain stage	4 mW
Quantizer	7 mW
Other blocks	3 mW
Technology	0.13μm, Digital CMOS, 1-Poly, 8-Metal (1P8M)

the above-mentioned noises is about 90-dB including 1-dB degradation due to the substrate noise.

5. Conclusions

In this paper a new class of single-loop multibit sigma-delta modulator topologies suitable for low-voltage and high-resolution applications in the MHz ranges was proposed using only a low OSR. They have unity-gain STF to alleviate the SNDR degradation due to circuit imperfections and high maximum out of band gain in their NTFs without any stability concerns to achieve the high SNDR with only a low OSR. Only one multibit DAC is needed in the feedback loop which greatly decreases the implementation complexity. To compensate the errors resulted from DAC unit elements both DWA and BDWA can be used. To show the usefulness of the proposed modulator structures a circuit design prototype of the proposed fourth order modulator with OSR=16 and $b = 4$ was provided. A two-stage class A/AB OTA was employed to implement the building blocks of the modulator. The class AB operation of the second stage of a two-stage OTA confines the slew limiting only to its first stage, which reduces the power consumption of the OTA in switched capacitor applications with large capacitance loads. A 4-bit quantizer was implemented using a flash architecture with a low-power, very low-voltage and high-speed comparator. DWA was employed to correct the DAC errors. This modulator was simulated in a standard CMOS 0.13-μm technology. The simulated SNDR and DR are 90 dB and 92.5 dB, respectively with a signal bandwidth of 1.25 MHz. The overall modulator dissipates about 40-mW from a single power supply voltage of 1.2-V.

Acknowledgments

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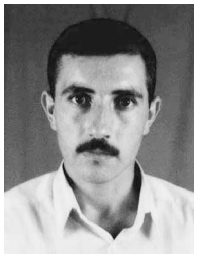

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