Low-voltage low-power fast-settling CMOS operational transconductance amplifiers for switched-capacitor applications

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Abstract: The authors present a new fully differential operational transconductance amplifier (OTA) for low-voltage and fast-settling switched-capacitor circuits in pure digital CMOS technology. The proposed two-stage OTA is a hybrid class A/AB that combines a folded cascode as the first stage with active current mirrors as the second stage. Owing to the class AB operation in the second stage, slew limiting occurs only in the first stage, resulting in low power dissipation for switched-capacitor circuits. It employs a novel hybrid cascode compensation scheme, merged Ahuja and improved Ahuja style compensations, for fast settling. A design procedure for the minimum settling time of the proposed OTA is described. To demonstrate the efficiency of the proposed OTA and its compensation method three design examples are also provided.

1 Introduction

The trend towards lower operating supply voltages and lower power consumption in mixed signal integrated circuits (ICs) has three strong motivations: (i) portable equipment capable of operating with a minimum number of battery cells to reduce volume and weight; (ii) voltage limitations resulting from smaller feature sizes of modern IC technologies; and (iii) longer operating periods without battery recharging or replacement.

Design of high-performance analogue circuits is becoming increasingly challenging with the persistent trend toward reduced supply voltages. The main bottleneck in the design of an analogue circuit is the operational amplifier. The realisation of a CMOS operational amplifier that combines high DC gain with high unity gain bandwidth has proven to be a difficult problem, especially in low-voltage circuits. The high DC gain requirement leads to multistage designs or cascoding of transistors with long channel devices biased at low current levels, whereas the high unity gain frequency requirement calls for a single-stage design with short channel devices biased at high bias current levels [1]. Cascoding is a well known means to enhance the DC gain of an amplifier without degrading its high-frequency performance [2]. But cascoding is not possible in low-voltage circuits owing to output voltage swing considerations. Another technique to achieve both high DC gain and unity gain bandwidth is to employ gain boosting [1, 3]. But in this technique at least four transistors should be cascoded at the output, which decreases the output voltage swing drastically. Two-stage OTAs can be used to achieve high DC gain. The major concern is the speed of this type of amplifier due to the additional poles and zeros in their signal transfer functions, where, without any frequency compensation, they are prone to instability. Fortunately, some frequency compensation methods have been proposed for designing a stable two-stage OTA such as Miller and cascode compensation schemes [4, 5]. So, two-stage OTAs can be used to achieve both the high DC gain and high-speed demands.

The Miller compensation scheme has a pole splitting effect which moves one pole to a lower frequency and the other to a higher frequency in order to make a dominant pole frequency [4]. The main drawbacks of Miller compensation are the low speed and low power supply rejection ratio (PSRR) compared to cascode compensation. In this compensation method, a compensating resistor is also needed, located in series with a compensating capacitor in order to move the right half-plane zero to the left half-plane. The value of this resistor is affected by temperature and other variations in device fabrication, and this results in greater variation in OTA frequency performance. Mainly MOS transistors are used to implement such resistors in the triode region where their design can be of concern in low-voltage applications. Of course, in sampled data circuits some techniques such as clock boosting and bootstrapping can be used, but they suffer from design and implementation complexities. Cascode compensation schemes alleviate the above-mentioned problems. In this technique a capacitor is located between a low-impedance node in the first stage and the second stage output node. It achieves high speed and high PSRR compared to Miller compensation at the cost of complex design and analysis procedures [5, 6].

Each stage of a two-stage op-amp can be a class A or class AB. A two-stage class A amplifier in switched-capacitor circuits has some drawbacks. First, its slew rate can be limited by currents in both first and second stage branches, which results in large power dissipation in switched-capacitor circuits due to large load capacitance. Second, they have a lower second pole frequency compared to class A/AB op-amps as will be discussed in the paper. To alleviate the above-mentioned problems, recently several class A/AB op-amps have been proposed [7, 8]. Choosing class AB operation for the second-stage results in slew

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limiting only in the first stage. This greatly reduces the power dissipation of the OTA used in switched-capacitor circuits because of existing large load capacitances. To build a class AB operation in the second stage, several techniques have been reported [7, 9, 10]. The simplest approach is to employ DC level shifting. Despite its simplicity, it suffers from some drawbacks. First, the output voltage swing is reduced because certain conditions must be satisfied for the circuit to work properly. Secondly, another frequency pole is generated through the DC level shifting transistors, which degrades the frequency performance of the OTA. To alleviate this problem high currents are required in the DC level shifting transistors, which results in high power dissipation.

Another method of obtaining class AB operation is to use dynamic level shifting. In this technique, capacitors are used to generate the signal level shifting needed for class AB operation [9]. The main drawback of this approach is the large capacitance requirement needed to establish a floating voltage source, which demands large silicon area. Also the PSRR is significantly degraded through the paths generated by the level shifting capacitors.

The third approach is to employ active current mirrors to create class AB operation as proposed in [7]. This approach has the highest PSRR among the above-mentioned approaches and is also better than the two-stage class A topology. The main drawback of this method is the pole and zero frequencies resulting from the current mirrors. It is worth mentioning here that other techniques, such as that reported in [10], have been used to build class AB output stages. However, they suffer from the added complexity needed to control the quiescent current, and generation of other poles and zeros in the signal transfer functions, which limits their speed. In this work an active current mirror scheme is used to build class AB operation in the second stage of the proposed OTA. To alleviate the affect of the current mirrors' pole and zero on the frequency performance, NMOS transistors are used to realise the active current mirrors.

In this paper a two-stage OTA with a new compensation technique is proposed to satisfy the high DC gain requirement for high-speed applications [8]. The proposed two-stage OTA has a class A/AB structure with a new hybrid cascode compensation scheme.

2 Proposed operational transconductance amplifier

Figure 1 shows the proposed OTA structure. The first stage is a folded cascode amplifier with PMOS input transistors. The PMOS input differential pair allows the use of near ground V_{cmi}, as the op-amp input common mode voltage. This allows the use of relatively small NMOS transistors to design the switches that are connected to V_{cmi}. This greatly increases the switch linearity in very low-voltage circuitry without any complex area and power consuming techniques such as bootstrapping and clock boosting. The second stage is a class AB amplifier with active current mirrors similar to [7]. The class AB operation of this stage ensures that slew limiting occurs only in the first stage. The second stage current is chosen to set the non-dominant poles at an adequately high frequency to guarantee stability. Because of the push–pull operation, the lowest non-dominant pole in the class A/AB design is governed by the time constant formed by the approximate sum of transconductance of the output transistors, M4 and M5 and the parasitic capacitances at the first stage output [5, 7]. Thus the output branch current can be about half that used in the two-stage class A circuit for the same non-dominant pole frequency. When this fact is exploited together with the use of gain in the second stage current mirrors, a significant reduction in power dissipation can be achieved relative to the two-stage class A topology. The mirror pole and zero will eventually degrade the phase margin of the circuit and finally its settling performance. To increase the mirror pole and zero frequencies in the active current mirrors, NMOS transistors are used in this design, where their transconductance can be about three times greater than PMOS transistors with the same overdrive voltages and gate dimensions due to the higher electron mobility compared to holes.

Common mode feedback (CMFB) is required in fully differential amplifiers to define the voltage at high impedance output nodes [4]. The common mode output voltage of the first stage is not coupled to the common mode output of the second stage. Therefore, two independent feedback circuits are needed to set up the common mode voltages at the outputs of the first and second stages. The second-stage CMFB circuit shown in Fig. 2 senses the common mode output voltage with a switched capacitor network. The output common mode voltage is then used to control two common source amplifiers, Mc1 and Mc2, that drive the output nodes. A simple switched-capacitor CMFB circuit is used in the first stage. It should be noted that it is possible to use a single CMFB circuit in a two-stage amplifier where an inversion stage is needed. However, due to the large bandwidth requirement for this inversion stage in a CMFB network it can be a power hungry circuit with power consumption comparable with the main amplifier.

Frequency compensation is used to maintain stability in a two-stage amplifier. The two-stage amplifier shown in Fig. 1

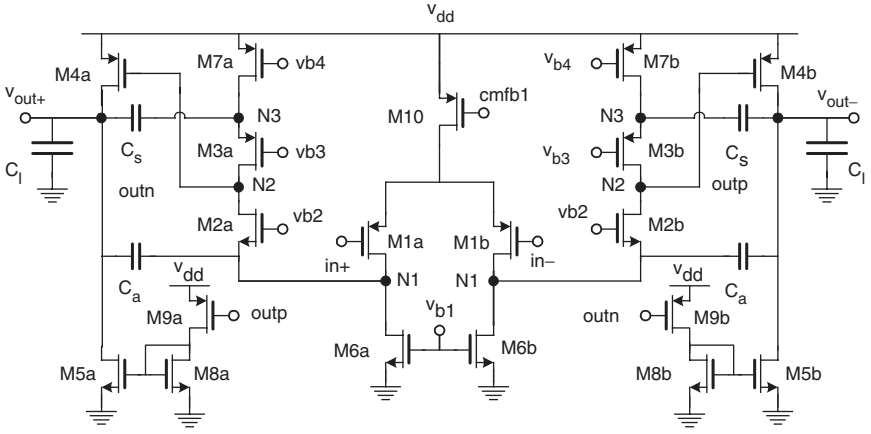

Fig. 1 *Proposed OTA structure*

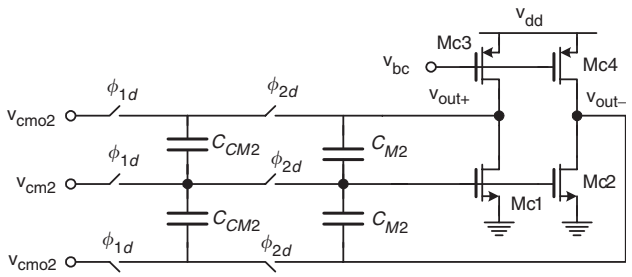

Fig. 2 *Second-stage CMFB circuit*

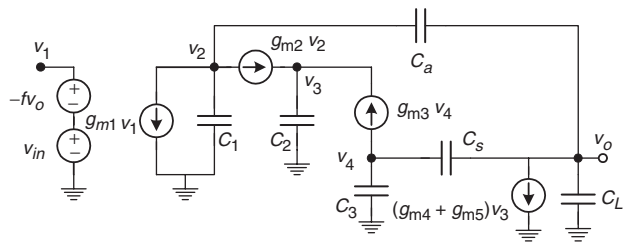

Fig. 3 *Closed-loop small-signal equivalent circuit*

employs a novel cascode compensation scheme where two capacitors are used between two low-impedance nodes in the first stage and the output node. In turn, this novel compensation approach merges Ahuja [5] and improved Ahuja style [11] compensation methods, to create two real poles, two complex poles at higher frequency, and three zeros. This compensation scheme yields a higher amplifier bandwidth than the standard Miller and conventional cascode compensation techniques at the cost of a more complex design procedure for the settling behaviour of the amplifier. Since the proposed compensation scheme creates an amplifier with four closed-loop poles and three zeros, the design equations become significantly more complicated than those of a single-stage OTA or conventional Miller and cascode compensated two-stage amplifier. This implies that for practical designs some form of computer optimisation constrained by trade-offs in the design equations will be necessary.

Figure 3 shows the closed-loop small-signal equivalent circuit for pole and zero analysis of the proposed OTA shown in Fig. 1, where C_1, C_2, C_3, and C_L represent the parasitic capacitances of nodes N_1, N_2, N_3, and the output node of the circuit shown in Fig. 1, respectively. f is the feedback factor. To simplify analysis, the output resistances of the devices are assumed to be infinite. It should be noted that the effect of finite device resistance is to move the amplifier poles slightly to the left, which will slightly increase the bandwidth of the amplifier [12, 13]. The node equations of this circuit are as follows:

$$g_{m1}v_1 + (sC_1 + g_{m2})v_2 + sC_a(v_2 - v_o) = 0 \quad (1)$$

$$sC_2v_3 - g_{m2}v_2 - g_{m3}v_4 = 0 \quad (2)$$

$$(sC_3 + g_{m3} + sC_s)v_4 - sC_sv_o = 0 \quad (3)$$

$$(sC_L + sC_a + sC_s)v_o - sC_av_2 + (g_{m4} + g_{m5})v_3 - sC_sv_4 = 0 \quad (4)$$

$$v_1 = v_{in} - fv_o \quad (5)$$

So, the transfer function will be:

$$\frac{v_o}{v_{in}} = \frac{g_{m1}(s^2C_aC_2 - g_{m2}g_m)(g_{m3} + sC_3 + sC_s)}{s^4d_4 + s^3d_3 + s^2d_2 + sd_1 + d_0} \quad (6)$$

where

$$g_m = g_{m4} + g_{m5} \quad (7)$$

$$d_4 = C_a^2C_2(C_3 + C_s) + C_s^2C_2(C_1 + C_a) - C_2(C_L + C_a + C_s)(C_1 + C_a)(C_3 + C_s) \quad (8)$$

$$d_3 = C_aC_2fg_{m1}(C_3 + C_s) + C_a^2C_2g_{m3} + C_2C_s^2g_{m2} - g_{m2}C_2(C_L + C_a + C_s)(C_s + C_3) - g_{m3}C_2(C_L + C_a + C_s)(C_1 + C_a) \quad (9)$$

$$d_2 = fg_{m1}g_{m3}C_aC_2 - g_{m2}g_mC_a(C_3 + C_s) - g_{m3}g_mC_s(C_1 + C_a) - g_{m2}g_{m3}C_2(C_L + C_a + C_s) \quad (10)$$

$$d_1 = -fg_{m1}g_{m2}g_m(C_3 + C_s) - g_{m2}g_{m3}g_mC_a - g_{m2}g_{m3}g_mC_s \quad (11)$$

$$d_0 = -fg_{m1}g_{m2}g_{m3}g_m \quad (12)$$

To verify the usefulness of the proposed compensation technique, the settling times of Ahuja style, improved Ahuja style, and the proposed compensation techniques are shown as functions of the total compensation capacitance in Fig. 4. In these simulations the small-signal parameters shown in Table 1 have been used. According to Fig. 4, the proposed compensation technique gives a lower settling time than the other alternatives.

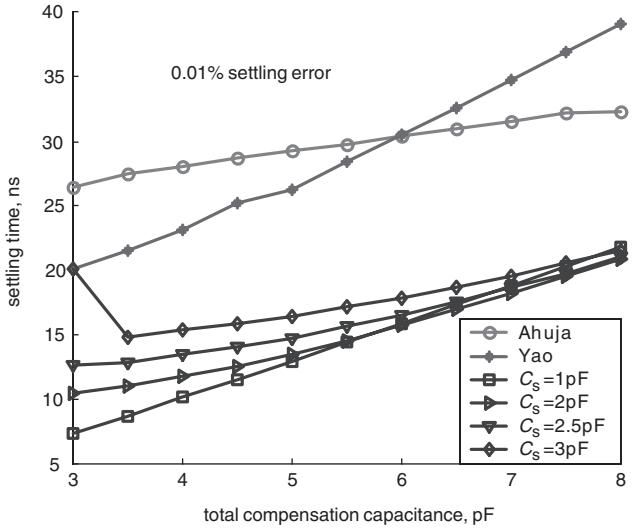

Fig. 4 *Settling time with different compensation techniques*

Table 1: Small-signal parameters

Parameter	Value	Parameter	Value
g_{m1}	4 mA/V	C_1	0.206 pF
g_{m2}	4.7 mA/V	C_2	0.627 pF
g_{m3}	4.2 mA/V	C_3	0.267 pF
g_{m4}	5.7 mA/V	C_L	4 pF
g_{m5}	7.4 mA/V	f	0.8

3 Design procedure

To investigate the settling behaviour of the proposed compensation technique a standard fourth-order system

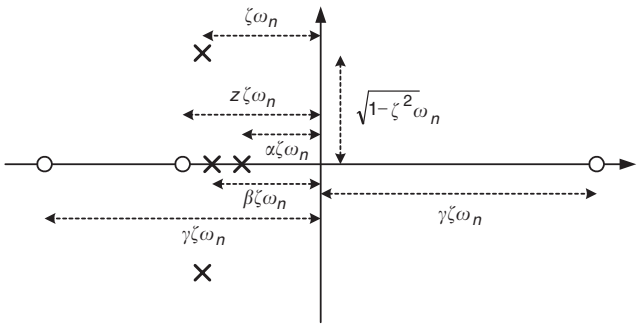

Fig. 5 *Closed-loop pole and zero locations*

with the following transfer function is considered:

$$H(s) = \frac{k(z_p^2 - s^2)(s + c)}{(s + a)(s + b)(s^2 + 2\zeta\omega_n s + \omega_n^2)}$$

$$= \frac{k(\gamma^2\zeta^2\omega_n^2 - s^2)(s + z\zeta\omega_n)}{(s + \alpha\zeta\omega_n)(s + \beta\zeta\omega_n)(s^2 + 2\zeta\omega_n s + \omega_n^2)} \quad (13)$$

where $a = \alpha\zeta\omega_n$, $b = \beta\zeta\omega_n$, $c = z\zeta\omega_n$ and $z_p = \gamma\zeta\omega_n$.

There are six system parameters, α, β, γ, ω_n, ζ and z in the transfer function. ω_n and ζ are called the natural frequency and damping factor, respectively. Figure 5 shows a description of these six system parameters in terms of the location of poles and zeros of the proposed compensation technique in a practical implementation.

In switched-capacitor circuits, the step response determines the amplifier settling performance in the time domain [14]. It can be shown that the step response of the above-mentioned fourth-order system is as follows:

$$s(t) = A_{cl}\{1 - a_1 \times e^{-\alpha\zeta\omega_n t} - a_2 \times e^{-\beta\zeta\omega_n t} + a_3 \times e^{-\zeta\omega_n t}\left(a_4 \times \cos(\omega_n t\sqrt{1-\zeta^2})\right) - a_3 \times e^{-\zeta\omega_n t}\left(a_5 \times \sin(\omega_n t\sqrt{1-\zeta^2})\right)\} \quad (14)$$

where A_{cl} is the closed-loop gain and

$$a_1 = \frac{\beta(z - \alpha)}{z(\beta - \alpha)(1 - 2\alpha\zeta^2 + \alpha^2\zeta^2)} \quad (15)$$

$$a_2 = \frac{\alpha(z - \beta)}{z(\alpha - \beta)(1 - 2\beta\zeta^2 + \beta^2\zeta^2)} \quad (16)$$

$$a_3 = \frac{\alpha\beta\zeta}{z(1 - 2\alpha\zeta^2 + \alpha^2\zeta^2)(1 - 2\beta\zeta^2 + \beta^2\zeta^2)} \quad (17)$$

$$a_4 = -z\zeta((\alpha - 1)(\beta - 1)\zeta^2 - 1 + \zeta^2) + (\alpha\zeta^2 - 1)(\alpha + \beta - 2)\zeta \quad (18)$$

$$a_5 = \{(z\zeta^2 - 1)((\alpha - 1)(\beta - 1)\zeta^2 - 1 + \zeta^2) + z\zeta^2(1 - \zeta^2)(\alpha + \beta - 2)\}\frac{1}{\sqrt{1 - \zeta^2}} \quad (19)$$

In the calculation of the step response it is assumed that γ tends to infinity since in practical cases the right- and left-plane z_p zero pair in the closed-loop transfer function will be at much higher frequencies than the other poles and zeros.

The settling error

$$\varepsilon_s = \frac{s(\infty) - s(t_s)}{s(\infty)}$$

is obtained as

$$\varepsilon_s = a_1 \times e^{-\alpha\zeta\omega_n t_s} + a_2 \times e^{-\beta\zeta\omega_n t_s} - a_3 \times e^{-\zeta\omega_n t_s}\left(a_4 \times \cos(\omega_n t_s\sqrt{1-\zeta^2})\right) + a_3 \times e^{-\zeta\omega_n t_s}\left(a_5 \times \sin(\omega_n t_s\sqrt{1-\zeta^2})\right) \quad (20)$$

This equation is very complex to intuitively explain how to choose the system parameters to optimise the settling error. Therefore, numerical calculations are used. Figure 6 shows the settling error of the proposed compensation technique for different values of the system parameters. For example, the system parameters obtained for -120 dB settling error are $\alpha = 0.95$, $\zeta = 0.9$, $z = 0.9$, $\beta = 0.95$, and $\omega_n t_s = 17$.

The system parameters obtained for a specific settling error in a defined time can be used to determine the device parameters using the following equations:

$$(\alpha + \beta + 2)\omega_n\zeta = \frac{d_3}{d_4} \quad (21)$$

$$(2(\alpha + \beta)\zeta^2 + \alpha\beta\zeta^2 + 1)\omega_n^2 = \frac{d_2}{d_4} \quad (22)$$

$$((\alpha + \beta)\zeta + 2\zeta^3\alpha\beta)\omega_n^3 = \frac{d_1}{d_4} \quad (23)$$

$$\alpha\beta\zeta^2\omega_n^4 = \frac{d_0}{d_4} \quad (24)$$

$$z\zeta\omega_n = \frac{g_{m3}}{C_s + C_3} \quad (25)$$

In these equations, the system parameters, α, β, z, ζ, and ω_n are known. The load and compensation capacitances, C_L, C_a, and C_s are determined based on circuit noise considerations. The parasitic capacitances, C_1, C_2, and C_3 are related to the device sizes. Also, all device transconductances can be determined by transistor size. So, these equations can be solved to determine device sizes using numerical calculations. However, these equations are very complex. In order to achieve a coarse design of the proposed op-amp, some approximations are considered to simplify solution of the above-mentioned equations and also give some practical insight. In (8)–(11) the parasitic capacitances, C_1, C_2, and C_3 are assumed to be much less than the other capacitances. In this case, (21)–(25) reduce to the following relations:

$$(\alpha + \beta + 2)\omega_n\zeta = -\frac{fg_{m1}}{C_L} + \frac{g_{m2}(C_L + C_a)}{C_aC_L} + \frac{g_{m3}(C_L + C_s)}{C_sC_L} \quad (26)$$

$$(2(\alpha + \beta)\zeta^2 + \alpha\beta\zeta^2 + 1)\omega_n^2 = -\frac{fg_{m1}g_{m3}}{C_sC_L} + \frac{(g_{m2} + g_{m3})g_m}{C_2C_L} + \frac{g_{m2}g_{m3}(C_L + C_a + C_s)}{C_aC_sC_L} \quad (27)$$

$$((\alpha + \beta)\zeta + 2\zeta^3\alpha\beta)\omega_n^3 = \frac{fg_{m1}g_{m2}g_m}{C_2C_aC_L} + \frac{g_{m2}g_{m3}g_m(C_a + C_s)}{C_2C_aC_sC_L} \quad (28)$$

$$\alpha\beta\zeta^2\omega_n^4 = \frac{fg_{m1}g_{m2}g_{m3}g_m}{C_2C_aC_sC_L} \quad (29)$$

$$z\zeta\omega_n = \frac{g_{m3}}{C_s} \quad (30)$$

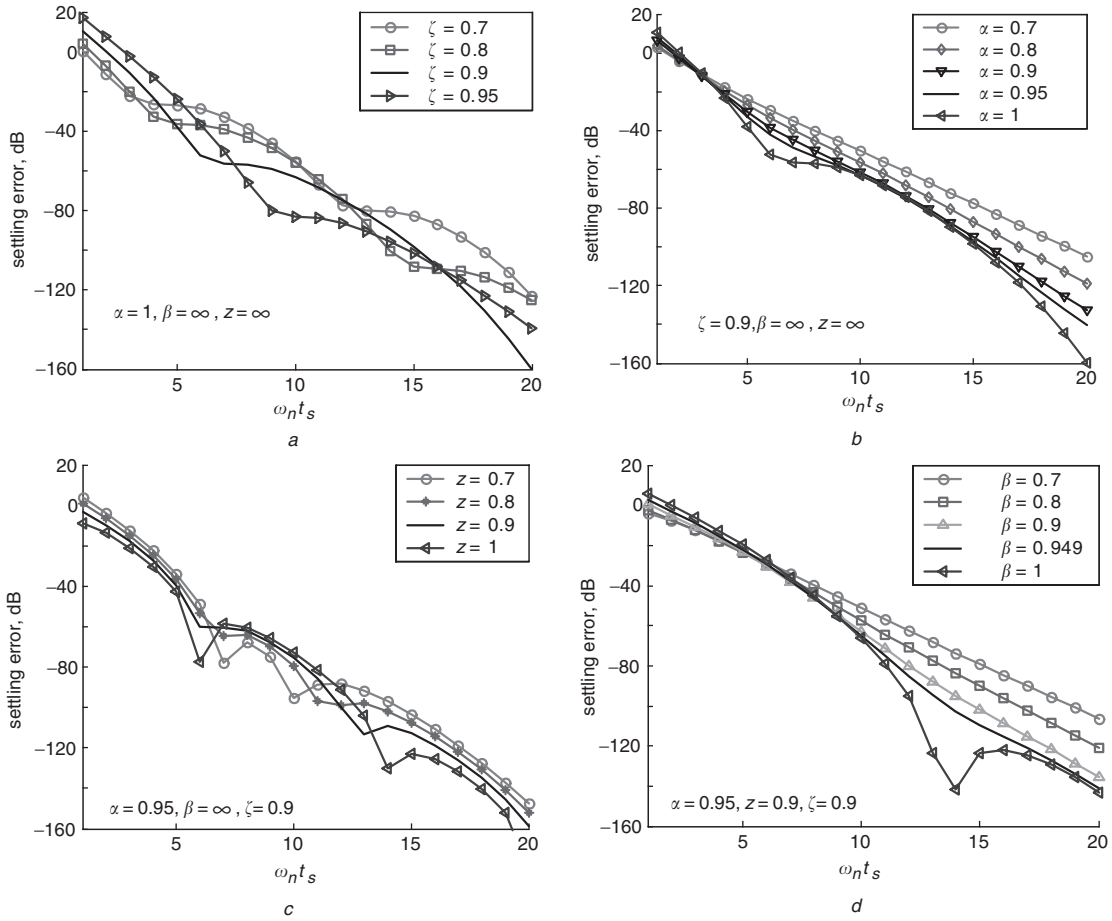

Fig. 6 *Settling errors as a function of* $\omega_n t_s$
a For different values of ζ
b For different values of α
c For different values of z
d For different values of β

In these equations, the transconductance of transistors M1, M2, M3, M4, and M5 and the parasitic capacitance C_2 at node N_2 are unknown and can be obtained by solving them. Then one can run circuit level simulations to refine the gate dimensions obtained from system level calculations to achieve the desired performance.

4 Simulation results

To demonstrate the usefulness of the proposed OTA and its compensation technique, three different design examples with Ahuja style, improved Ahuja style, and the proposed compensation techniques were considered at the circuit level. First, the system parameters of these design examples were obtained using their settling error equations with numerical calculations using MATLAB [15]. Then, circuits were simulated in a 0.25 µm BSIM3v3 level 49 mixed-signal CMOS model with HSPICE. The threshold voltages for this technology for NMOS and PMOS transistors are 0.55 V and −0.65 V, respectively excluding the body effect. This process has 2-poly 5-metal (2P5M) form. Poly–poly capacitors are available in this technology to implement high linear capacitors. In these simulations, the OTAs were designed for a switched-capacitor integrator as shown in Fig. 7. The bootstrapped switches proposed in [16] were used in these designs. Figure 8 shows the settling behaviour of the proposed OTA with three different compensation methods. Simulation results are given in Table 2. Table 3

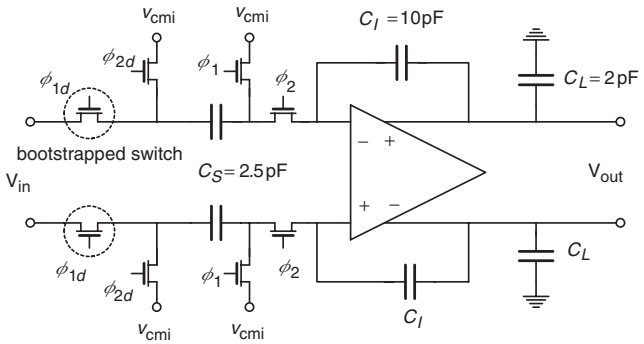

Fig. 7 *Switched-capacitor integrator*

shows the OTA design parameters used in the HSPICE simulations. Simulation results in Fig. 8 show that the proposed cascode compensation technique results in a faster settling performance compared to the Ahuja and improved Ahuja style compensation methods with the same power consumption. It is worth mentioning that for designs of the proposed OTA with different compensation methods having the same settling time, the proposed cascode compensation technique results in lower power dissipation. Also the PSRR, slew rate, and input referred noise of the three compensation methods are approximately the same.

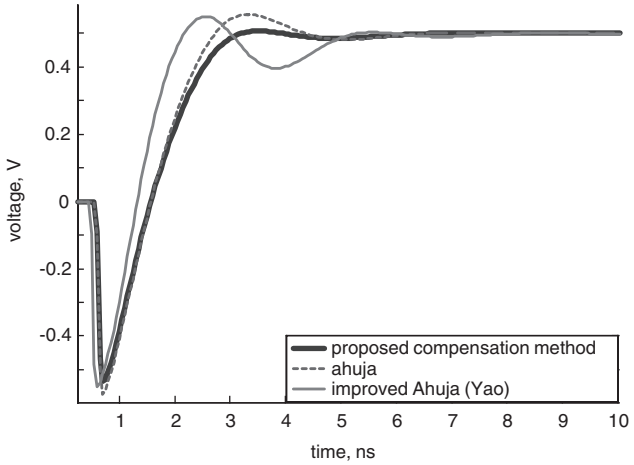

Fig. 8 *Transient simulation results (step response)*

Table 2: Simulation results

Parameter	Ahuja	Improved Ahuja	Proposed method
Power supply voltage, V	1.5	1.5	1.5
DC gain, dB	80.3	79	80
Unity gain bandwidth, MHz	137	151	167
Phase margin, deg	75.5	89	73.5
Settling time (0.01%), ns	10.1	12.4	7.1
Slew rate, V/μs	476	487	464
Output swing, V_{pp}	1.13	1.13	1.13
Input referred thermal noise, V^2/Hz	1.6×10^{-16}	1.5×10^{-16}	1.2×10^{-16}
Power consumption, mW	8.9	8.9	8.9

Table 3: Device sizes used in HSPICE simulations

Parameter	Ahuja	Improved Ahuja	Proposed method
$(W/L)_1$	80/0.5	80/0.5	120/0.5
$(W/L)_2$	50/0.35	70/0.35	50/0.35
$(W/L)_3$	180/0.35	300/0.25	150/0.35
$(W/L)_4$	200/0.35	200/0.35	200/0.35
$(W/L)_5$	100/0.35	100/0.35	100/0.35
$(W/L)_6$	80/0.5	80/0.5	80/0.5
$(W/L)_7$	200/0.5	200/0.5	200/0.5
$(W/L)_8$	50/0.35	50/0.35	50/0.35
$(W/L)_9$	100/0.35	100/0.35	100/0.35
$(W/L)_{10}$	250/0.25	250/0.25	250/0.25
C_s, pF	—	3	1.5
C_a, pF	3	—	1.5
C_L, pF	4	4	4

5 Conclusions

In this paper a new merged two-stage class A/AB OTA has been proposed. Because of the class AB operation of the second stage, the currents in this stage are determined so that the non-dominant poles and zeros are sufficiently large in frequency to maintain stability. Thus, the second-stage currents are not constrained by the slew rate limiting of the OTA, which results in power saving in the switched-capacitor circuits. To move the mirror pole and zero to a high frequency, NMOS transistors are used in the active current mirrors. The op-amp employs a novel cascode compensation technique in which two compensating capacitors are used between two distinct low-impedance nodes of the first stage and the output node of a two-stage OTA. This compensation approach results in faster settling performance than the conventional Miller, Ahuja style, and improved Ahuja style compensation techniques at the cost of a more complex design procedure. A design procedure was considered for the proposed OTA with its new compensation method. Circuit level simulations were also provided with HSPICE to demonstrate the efficiency of the proposed compensation technique.

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