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A fully-differential improved recycling folded-cascode amplifier for fast-settling switched-capacitor applications

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ABSTRACT

In this paper, a fully-differential class A single-stage CMOS operational transconductance amplifier (OTA) is presented for high-speed switched-capacitor (SC) applications. The main target is to improve both large and small signal parameters in order to achieve a fast-settling performance with sufficient accuracy in SC circuits without needing more power dissipation. Several techniques including the current recycling, phase margin enhancement using high-speed current mirrors, and cross-coupled local positive feedback transistors are employed in the traditional folded-cascode amplifier (FCA) to realize a multi-path single-stage OTA with increased unity-gain frequency, slew rate, and DC gain. Detailed analytical calculations and circuit level simulation results are collected to compare the suggested OTA with alternatives. Based on the analytical calculations, the proposed amplifier significantly outperforms the traditional folded-cascode OTA regarding both large-signal and small-signal parameters. The suggested OTA is simulated in TSMC 65 nm CMOS technology in a SC integrator configuration to verify its usefulness. According to the simulation results, the DC gain, unity-gain bandwidth, and slew rate of the proposed OTA are improved about 22.9 dB, 576 %, 241 %, respectively, compared to the conventional FCA with almost the same power dissipation and other similar simulation conditions. The proposed OTA can be utilized in fast-settling switched-capacitor circuits as well.

1. Introduction

The operational transconductance amplifiers (OTAs) are one of the most important blocks in microelectronic circuits. OTAs are extensively employed in mixed-signal and analog integrated circuits to drive the capacitive loads [1–4]. In switched-capacitor circuits, CMOS OTAs are widely used to transfer the charge between the capacitors with the targeted accuracy. In such applications, the principal function of the OTA is to make a simple virtual ground in the closed-loop configuration and the OTA is needed to settle with the required accuracy within a definite time period. The performance of CMOS OTAs is characterized by large-signal and small-signal metrics like the slew rate, unity-gain frequency, DC gain, etc.

The single-stage, two-stage, and multi-stage structures can be employed in OTAs. The DC gain is significantly increased in multi-stage amplifiers at the cost of degraded stability in the closed-loop configuration and also reduced signal bandwidth. Frequency compensation techniques and architectural improvements can be employed to design multi-stage amplifiers with sufficient stability headroom and enhanced performance [5–8]. Nevertheless, the frequency compensation methods considerably decrease the unity-gain frequency, and hence, the speed of the amplifier. Furthermore, the design of multi-stage OTAs is complex especially in fast-settling switched-capacitor circuits [9–13]. On the other hand, single-stage amplifiers are essentially stable in the feedback configuration owing to having just one high impedance signal node, and therefore, one real dominant frequency pole.

The telescopic-cascode, folded-cascode, and current-mirror amplifiers are three main single-stage OTAs [1,2]. In low-voltage applications, the folded-cascode amplifier (FCA) is widely utilized since it results in larger output swing and needs smaller power supply voltage compared to the telescopic-cascode OTA, although its other performance parameters like DC gain, input-referred noise, power consumption, and speed are not comparable. In the FCA, the PMOS input differential pair transistors are usually utilized instead of the NMOS one due to the lower input common-mode (CM) voltage, larger non-dominant frequency pole, and smaller input-referred flicker noise [1,2]. As depicted in Fig. 1, in the folded-cascode OTA, the transistors M_3 and M_4 draw the most DC current without their any action in the signal path. This is the main

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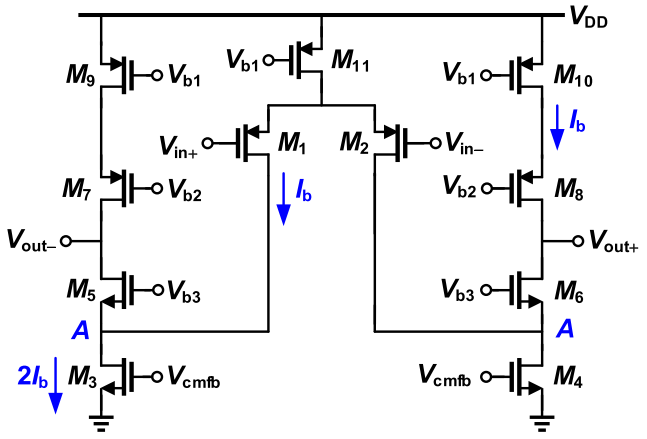

Fig. 1. Circuit schematic of the fully-differential FCA.

disadvantage of the FCA and several schemes have been suggested to enhance the operation of the conventional FCA [14–53].

In [14], additional transistors are employed to enhance the common-mode rejection ratio (CMRR) and DC gain without sacrificing the slew rate. In this OTA, a two-path amplifier with one FCA and one FCA followed by an active current-mirror are employed with the same input pair and the DC current of M_3 and M_4 transistors in traditional FCA are used to bias all cascode and input transistors. By this technique, the current source M_7-M_{10} transistors are also used in the signal path. In [15], complementarily NMOS and PMOS differential pairs are employed as the input transistors in the FCA to realize a two-path OTA.

In [16], using flipped voltage follower (FVF) cells [17], a FCA with class AB scheme in both output and input stages is suggested. The gate of FVF cell transistors is properly connected to the gate of current source M_{10} and M_9 transistors to bring them into the signal amplification path and also realize the class AB function at the output stage. In [18], a three-path amplifier is developed by using one FCA, one current-mirror amplifier, and one folded-cascode current-mirror amplifier. The input signal is capacitively coupled to the gate of current source output transistors in [19] to achieve the class AB scheme at the output stage without any static power consumption. In [20,21], in order to exploit the idle current source M_3 and M_4 transistors in the traditional FCA towards the signal path, the input transistors in Fig. 1 are split as M_1, M_2, M_{1a}, and M_{2a}. In comparison with the FCA, the unity-gain frequency, slew rate, and DC gain of the single-ended recycling folded-cascode amplifier (RFCA) are improved more than two times, three times, and twice, receptively, but with degraded phase margin owing to the added frequency poles and zeros.

In [22], based on the RFCA, a single-stage three-path class AB amplifier is suggested which consists of two current-mirror and one folded-cascode OTAs and the class AB function is implemented in input stage with the FVF cell. A small-signal transconductance enhancement method for singled-ended RFCA has been presented in [23] by using shunt current sources. A double recycling FCA has been presented in [24] by splitting the input transistors into three differential pairs. In [25], the current sources in [23] are substituted with cross-coupled transistors to realize a local positive feedback path. High-speed current mirrors are employed in [26] to boost the phase margin of the traditional RFCA. In [27], two current-mirror and one folded-cascode amplifiers with cross-coupled positive feedback transistors have been utilized to realize a three-path OTA. In [28], a new input path along with positive feedback technique have been used for increasing the unity-gain frequency and DC gain. Also, splitting the common-mode feedback and tail current source is employed to improve the adjustment of output common-mode voltage.

A left half plane (LHP) frequency zero has been realized in [29] using a fast signal path in the fully-differential RFCA for improved stability. Using the gain boosting method in both PMOS and NMOS output current sources and also high-speed current mirrors, an improved RFCA has been presented in [30]. Several techniques including double current recycling, shunt active current sources, and additional drivers have been used in [31] to realize a multi-path fully-differential OTA. A single-ended RFCA with local common-mode feedback is demonstrated in [32] for improved unity-gain frequency, slew rate, and DC gain. Using FVF cells, nonlinear current mirrors, and self-biasing techniques, a single-stage class AB amplifier with improved and balanced slew rate is suggested in [33]. To handle large capacitive loads, a single-ended class AB FCA has been suggested in [34] by using the adaptive biasing technique and FVF cells. A single-ended RFCA with adaptive class AB input stage has been demonstrated in [35]. Using the local common-mode feedback method and FVF cells, a single-ended super class AB OTA is suggested in [36]. In [37], the local common-mode feedback and adaptive biasing techniques are employed to enhance the slew rate and small-signal behavior.

In [38], in the traditional telescopic-cascode amplifier, the input transistors are divided to realize a two-path amplifier consisting of one telescopic-cascode amplifier and one FCA. In [39], a fully-differential RFCA with increased unity-gain frequency, slew rate, and DC gain is presented. An enhanced FCA using adaptive class AB input stage and nonlinear current recycling in output stage has been introduced in [40]. Using positive feedback method and self-biased cascode transistors, a bulk-driven double recycling FCA is suggested in [41] for biomedical applications. A fully-differential bulk-driven four-path OTA with class AB scheme in input stage has been demonstrated in [42]. An asymmetrical current division in differential input pair transistors of a single-ended RFCA is employed in [43] to enhance the DC gain and transconductance. In [44], a fully-differential class AB RFCA with enhanced DC gain has been presented using an auxiliary amplifier and adaptive input biasing. A double recycling FCA has been suggested in [45] for biopotential amplifiers. The local positive feedback method is utilized in input stage of the conventional FCA in [46] to increase the slew rate, gain bandwidth, and DC gain. In [47], a single-ended bulk-driven class AB amplifier has been demonstrated with two FVF cells in input pairs and a double recycling FCA. A fully-differential two-stage class AB amplifier is suggested in [48] where a floating battery is utilized to implement the first stage as a double RFCA. In [49], a super class AB OTA is realized using two nested negative and positive feedback loops in the active loads and also an adaptive biased input stage is employed.

Using two current recycling stages, an adaptive double recycling FCA has been proposed in [50]. In [51], a recycling FCA is proposed to boost the slew rate and small-signal transconductance using a local common-mode feedback circuit and nonlinear current mirrors. A super class AB OTA has been presented in [52] by employing current reuse technique. In [53], the proposed bulk driven OTA utilizes the FVF cell along with the auxiliary amplifier to realize an adaptive biasing input stage and the quasi-floating scheme to make the class AB output stage. In [54], in the traditional telescopic-cascode amplifier, the input transistors are divided to realize a two-path amplifier consisting of current-mirror and telescopic-cascode amplifiers. In scaling for sub 5 nm node technologies, the DC gain and CMRR of OTAs can be further improved using new device structures such as multi-bridge-channel FETs [55]. A complete review on the architectural improvements of the FCA has been recently presented in [56]. In overall, the main objective in this field is to improve both small and large performance of CMOS amplifiers without needing any more power consumption.

In this paper, an improved multi-path single-stage recycling folded-cascode class A amplifier is presented. The cross-coupled local positive feedback and high-speed current mirror techniques are utilized to considerably improve simultaneously large- and small-signal parameters containing slew rate, DC gain, and unity-gain frequency with a reasonable phase margin. The remainder of this paper is arranged as follows. In Section 2, the configuration of the suggested amplifier is explained following by the detailed analysis. Section 3 compares the

proposed amplifier with the traditional folded-cascode amplifier and IRFCA in [27]. In Section 4, some detailed circuit level simulation results are provided and the conclusion is given in Section 5.

2. Proposed improved recycling folded-cascode OTA

In this section, firstly the architecture of the suggested improved recycling folded-cascode (IRFC) OTA is described. Subsequently, the detailed analysis of the suggested amplifier is presented. As for CMOS amplifiers, here, the main target is to enhance DC gain, unity-gain bandwidth, and slew rate without using any extra current dissipation.

2.1. Structure of the suggested IRFC OTA

The schematic of the suggested IRFC OTA is depicted in Fig. 2. The transistors M_1-M_{11} form the traditional folded-cascode amplifier. The input transistors are divided into equal size M_1, M_2, M_{1a}, and M_{2a} transistors in order to utilize the current recycling method in the conventional FCA. Three wide-swing cascode active current mirrors comprising of M_3-M_6 with M_{3a}-M_{6a}, M_{3c}-M_{6c} with M_{3a}-M_{6a}, and M_7-M_{10} with M_{7a}-M_{10a} are utilized to realize two additional current mirror OTAs in the traditional FCA. The ratio of these active current mirrors is defined as (1). The proper selection of these current mirror ratios is needed to improve the performance of the proposed OTA as well while achieving a robust and stable operation in practical applications.

$$k=\frac{(W/L)_{3,4}}{(W/L)_{3a,4a}},\quad m=\frac{(W/L)_{3b,4b}}{(W/L)_{3a,4a}},\quad p=\frac{(W/L)_{3c,4c}}{(W/L)_{3a,4a}}$$
$$q=\frac{(W/L)_{9,10}}{(W/L)_{9a,10a}},\quad n=\frac{(W/L)_{9b,10b}}{(W/L)_{9a,10a}}. \tag{1}$$

The cross-coupled transistors M_{3b}-M_{6b} and M_{7b}-M_{10b} are employed to realize two local positive feedback paths at the lower and upper active current mirrors, respectively. By this technique, both large and small signal parameters of the suggested OTA are considerably improved.

The deep triode transistors M_{r1}-M_{r4}, are utilized to realize high-speed active current mirrors [26,30]. By this method, LHP zeros are added in the small-signal transfer function resulting in improved phase margin in the closed-loop configuration. According to Fig. 3(a), using wide-swing cascode current mirrors, a constant current biasing circuit provides V_{b1} – V_{b3} biasing voltages for the main amplifier. A simple CM feedback

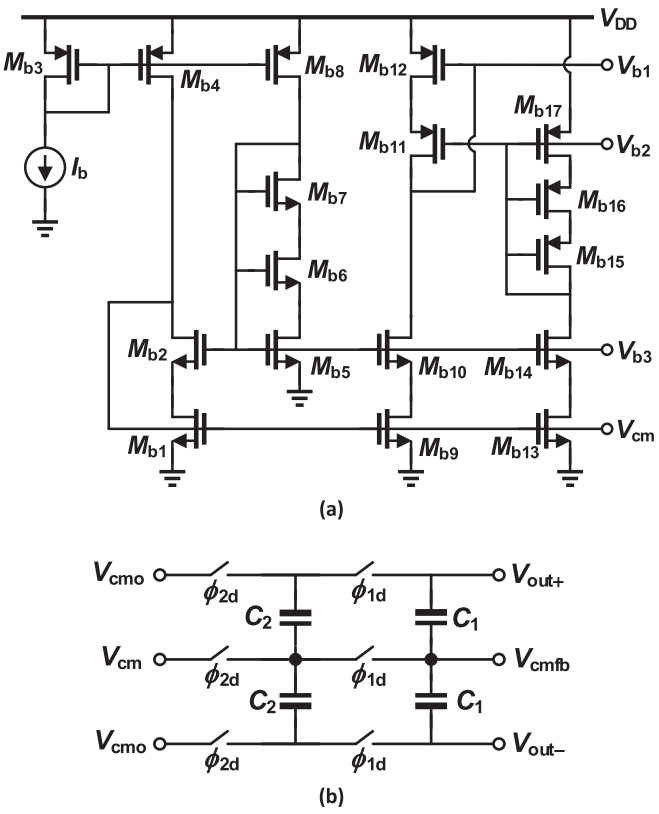

Fig. 3. (a) Bias circuit and (b) CMFB circuit.

(CMFB) circuit using switched-capacitor circuits is employed to adjust the CM voltage of the output nodes as illustrated in Fig. 3(b). The output of the CMFB circuit is connected to the gate of M_{3d}-M_{4d} transistors in the main amplifier so that to adjust the CM voltage of output nodes with less frequency poles and also without needing any additional inverting amplifier in the CMFB loop.

In comparison with [27], here, two additional techniques are utilized in the suggested OTA. First, the cross-coupled transistors are also employed in the upper current mirrors by adding transistors M_{7b}-M_{10b} to

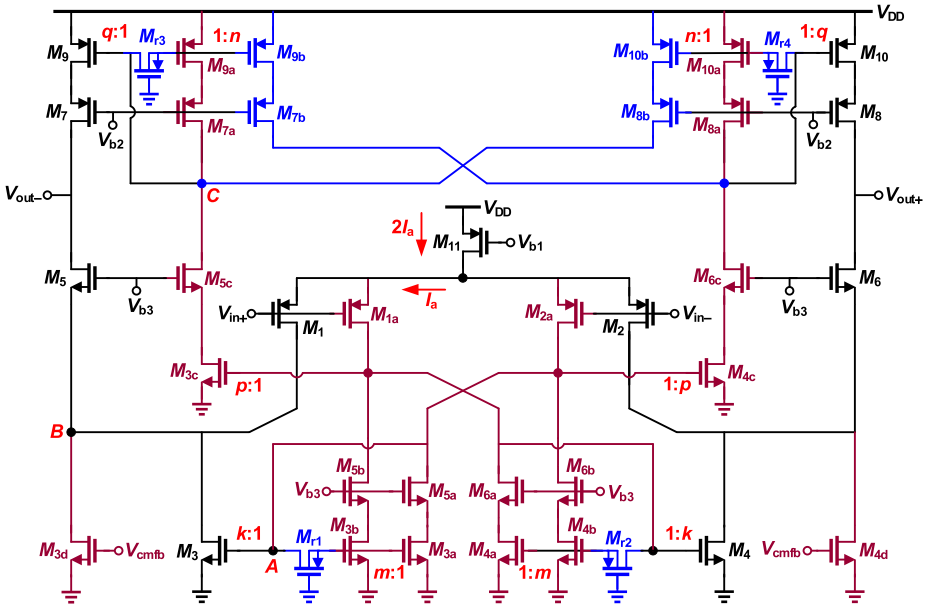

Fig. 2. Circuit schematic of the suggested improved recycling FCA.

further boost both small and large signal performance metrics including unity-gain frequency, DC gain, and slew rate. Second, high speed current mirrors are used in both lower and upper active current mirrors to create LHP zeros to alleviate the phase margin degradation owing to the added signal paths. This is realized using the deep triode region M_{r1}-M_{r4} transistors. In the next sub-sections, a detailed analysis of the suggested IRFC OTA specifications is reported.

2.2. DC analysis

With a simple DC analysis of the proposed OTA, some important results are obtained here. The parameters k, m, n, p, and q in the following equations are the ratios of the active current mirrors as defined in relation (1) and illustrated in Fig. 2. The DC drain current of transistors M_{3d} and M_{4d} is easily obtained as

$$I_{D3d} = I_{D4d} = I_a \left[\frac{(n+1)(m+1) + p\,q - k(n+1)}{2(m+1)(n+1)} \right]. \tag{2}$$

For NMOS transistors, this amount should be positive. So, the first biasing condition is obtained as

$$m+1+\frac{p\,q}{n+1} > k \quad => \quad (m+1)(n+1) + pq > k(n+1) \tag{3}$$

The total DC current of the suggested OTA excluding the biasing circuit is given by

$$\begin{aligned} I_{total} &= 2(I_{D1} + I_{D1a} + I_{D9} + I_{D9a} + I_{D9b}) \\ &= I_a \times \left[\frac{2(m+1)(n+1) + p(1+q+n)}{(m+1)(n+1)} \right]. \end{aligned} \tag{4}$$

Therefore, the total static power dissipation of the suggested OTA excluding the biasing circuit is obtained as

$$P_{static} = V_{DD} I_a \times \left[\frac{2(m+1)(n+1) + p(1+q+n)}{(m+1)(n+1)} \right]. \tag{5}$$

2.3. Slew rate

Whereas a large positive differential input signal ($V_{in+} \gg V_{in-}$) is applied to the proposed amplifier, M_1 and M_{1a} transistors goes into the cut-off region. Consequently, the transistors M_{4a}, M_{4b}, M_4, M_{3c}, M_{9a}, M_{9b} and M_9 turn off, too. The whole current of the transistor M_{11} flows into M_2 and M_{2a} drains. Since the drain current of M_{3b} transistor is zero, and therefore, it enters into the deep triode region. Hence, the drain current of the M_3 and M_{10} transistors are calculated as

$$I_{D3} = kI_{D2a}, \quad I_{D10} = pqI_{D2a}. \tag{6}$$

On the other hand, we have:

$$\begin{aligned} &\begin{cases} I_{D2} = I_{D4d} = cte \\ I_{D2} + I_{D2a} = 2I_a \end{cases} \quad => \quad I_{D2a} = 2I_a - I_{D4d} \\ &=> I_{D2a} = I_a \left[2 - \frac{(n+1)(m+1) + p\,q - k(n+1)}{2(m+1)(n+1)} \right] \\ &=> I_{D2a} = I_a \frac{3(m+1)(n+1) - p\,q + k(n+1)}{2(m+1)(n+1)}. \end{aligned} \tag{7}$$

So, the amount of negative and positive slew rates is acquired as

$$\begin{aligned} SR^- &= \frac{I_{D3d} + I_{D3}}{C_L} = \frac{I_{D3d} + kI_{D2a}}{C_L} \\ &= \frac{I_a}{C_L} \frac{[k^2 + k(3m+2) + (m+1)](n+1) - pq(k-1)}{2(m+1)(n+1)} \end{aligned} \tag{8}$$

$$\begin{aligned} SR^+ &= \frac{I_{D10}}{C_L} = \frac{pqI_{D2a}}{C_L} \\ &= \frac{pqI_a}{C_L} \times \frac{3(m+1)(n+1) - p\,q + k(n+1)}{2(m+1)(n+1)} \end{aligned} \tag{9}$$

where C_L is the output load capacitance between each output node and the ground. To achieve a balanced slew rate at the output nodes, the following condition is needed.

$$\begin{aligned} &k^2(n+1) + k[(n+1)(3m+2-pq) - pq] \\ &+ (n+1)(m+1) + pq[1 - 3(n+1)(m+1) + p\,q] = 0 \end{aligned} \tag{10}$$

By satisfying the relation (10), the amount of differential slew rate is acquired as

$$\begin{aligned} SR_{diff} &= SR^+ + SR^- = \frac{2pqI_{D2a}}{C_L} \\ &= \frac{2pqI_a}{C_L} \times \frac{3(m+1)(n+1) - p\,q + k(n+1)}{2(m+1)(n+1)} \end{aligned} \tag{11}$$

2.4. Unity-gain bandwidth and DC gain

The small-signal transconductance, G_m, which is the proportion of output short circuit current to the input signal voltage, is calculated as

$$G_m = g_{m1} + \frac{g_{m1a}}{g_{m3a} - g_{m3b}} \left[g_{m3} + \frac{g_{m3c}}{g_{m9a} - g_{m9b}} g_{m9} \right] \tag{12}$$

where g_{mi} is the transconductance of the related transistors. As it is known, the g_m ratio of the transistors in a current mirror is equal to the ratio of their drain current and/or the ratio of their aspect ratio. Therefore, G_m of the proposed OTA is given by

$$G_m = g_{m1} \left[\frac{(1-m)(1-n) + k(1-n) + pq}{(1-m)(1-n)} \right]. \tag{13}$$

Hence, the DC gain the proposed amplifier is calculated as

$$\begin{aligned} &\begin{cases} A_{dc} = G_m R_{out} \\ R_{out} \approx g_{m7} r_{ds7} r_{ds9} \| g_{m5} r_{ds5} (r_{ds1} \| r_{ds3} \| r_{ds3d}) \end{cases} \\ &=> A_{dc} = g_{m1} \left[\frac{(1-m)(1-n) + k(1-n) + pq}{(1-m)(1-n)} \right] \\ &\quad \times \left[g_{m7} r_{ds7} r_{ds9} \| g_{m5} r_{ds5} (r_{ds1} \| r_{ds3} \| r_{ds3d}) \right] \end{aligned} \tag{14}$$

where R_{out} is the output resistance between each output node and the ground and r_{dsi} is the drain-source resistance of the related transistors.

By taking into account the dominant frequency pole at the output node, the unity-gain bandwidth of the suggested amplifier is also calculated as

$$\begin{aligned} \omega_t &\approx A_{dc} \omega_{out} = G_m R_{out} \times \frac{1}{R_{out} C_L} = \frac{G_m}{C_L} \\ &= \frac{g_{m1}}{C_L} \left[\frac{(1-m)(1-n) + k(1-n) + pq}{(1-m)(1-n)} \right]. \end{aligned} \tag{15}$$

2.5. Frequency response

In this part, the frequency response of the differential gain of the suggested IRFC OTA is calculated. As it is evident, in the signal path of the proposed OTA, there are four nodes that we can assign one pole to each node. By using the compensation transistors and satisfaction of relation (16), the assigned poles of each node are obtained as relation (17).

$$R_1 = \frac{1}{g_{m3a}(1-m)} \quad k+p>1+m$$
$$R_2 = \frac{1}{g_{m9a}(1-n)} \quad q>1+n \tag{16}$$

$$\omega_{out} = \frac{-1}{R_{out}C_L}, \quad \omega_A = \frac{-1}{R_1 C_{gs,3a}(k+p)},$$
$$\omega_B = \frac{-g_{m5}}{C_B}, \quad \omega_C = \frac{-1}{R_2 C_{gs,9a} q} \tag{17}$$

where R_1 and R_2 are the equivalent resistance of $M_{r1,r2}$ and $M_{r3,r4}$ transistors, respectively. The frequency response of the differential gain is easily calculated as relations (18) and (19).

$$A_v(s) = \frac{A_1}{(1+s/\omega_B)(1+s/\omega_{out})} + \frac{A_2}{(1+s/\omega_A)(1+s/\omega_{out})} + \frac{A_3}{(1+s/\omega_A)(1+s/\omega_C)(1+s/\omega_{out})} \tag{18}$$

$$=> \quad A_v(s) = \frac{N(s)}{D(s)}$$
$$N(s) = A_1(1+s/\omega_A)(1+s/\omega_C) + A_2(1+s/\omega_C)(1+s/\omega_B) + A_3(1+s/\omega_B)$$
$$D(s) = (1+s/\omega_A)(1+s/\omega_B)(1+s/\omega_C)(1+s/\omega_{out}) \tag{19}$$

where the parameters A_1, A_2, A_3 are the DC gain of three distinct signal paths, and they are given by

$$A_1 = g_{m1}R_{out}, \quad A_2 = \frac{k}{(1-m)}A_1, \quad A_3 = \frac{pq}{(1-m)(1-n)}A_1. \tag{20}$$

3. Comparison with FCA and IRFCA in [27]

In this section, a detailed analytical comparison between the proposed OTA with conventional FCA and also the IRFCA in [27] is provided.

3.1. Comparison with FCA

Here, a fair comparison between the suggested IRFC amplifier and traditional FCA is provided. To make a fair comparison, the same power dissipation and input transistors with equal aspect ratios are considered. By assuming the same DC current in cascode and input transistors in a fully-differential FCA, its overall current consumption is given by

$$I_{total,fc} = 4I_{D1} \equiv 4I_c. \tag{21}$$

Therefore, according to the relations (4) and (21), we have

$$I_{total} = I_a \times \left[\frac{2(m+1)(n+1)+p(1+q+n)}{(m+1)(n+1)}\right] = 4I_c$$
$$=> \quad I_c = \frac{2(m+1)(n+1)+p(1+q+n)}{4(m+1)(n+1)}I_a. \tag{22}$$

On the other side, the slew rate of the FCA is as follows:

$$SR^+_{fc} = SR^-_{fc} = \frac{I_c}{C_L} \quad => \quad SR_{diff,fc} = \frac{2I_c}{C_L}. \tag{23}$$

Hence, considering the relations (11) and (23), slew rate of the suggested amplifier and FCA is related as

$$\frac{SR_{diff}}{SR_{diff,fc}} = \frac{2pq[3(m+1)(n+1)-pq+k(n+1)]}{2(m+1)(n+1)+p(1+q+n)} \tag{24}$$

By considering the equal aspect ratio of input transistors in the suggested and folded-cascode OTAs, the gm of the input transistors in the suggested OTA and FCA is related as

$$g_{m1} = g_{m1,fc}\sqrt{\frac{(m+1)(n+1)}{2(m+1)(n+1)+p(1+q+n)}}. \tag{25}$$

Hence, according to the relations (13) and (25), the overall transconductance of the suggested amplifier in terms of that of the FCA is given by

$$\frac{G_m}{G_{m,fc}} = \left[\frac{(1-m)(1-n)+k(1-n)+pq}{(1-n)(1-m)}\right] \times \sqrt{\frac{(m+1)(n+1)}{2(n+1)(m+1)+p(1+q+n)}}. \tag{26}$$

Therefore, the unity-gain frequency and DC gain of the suggested amplifier versus the FCA are obtained as

$$\frac{\omega_t}{\omega_{t,fc}} = \left[\frac{(1-n)(1-m)+k(1-n)+pq}{(1-n)(1-m)}\right] \times \sqrt{\frac{(n+1)(m+1)}{2(n+1)(m+1)+p(1+q+n)}}. \tag{27}$$

$$\frac{A_{dc}}{A_{dc,fc}} \approx \left[\frac{(1-n)(1-m)+k(1-n)+pq}{(1-n)(1-m)}\right] \times \sqrt{\frac{(n+1)(m+1)}{2(n+1)(m+1)+p(1+q+n)}}. \tag{28}$$

3.2. Comparison with IRFCA in [27]

A similar comparison is provided between the proposed OTA and the one in [27]. To do so, similar power dissipation and equal aspect ratio in input transistors in both OTAs are also considered. It is worth mentioning that the suggested OTA in [27] is a special case of the one proposed here with $n = 0$ and removing M_{r1}-M_{r4} transistors. So, the structure of the OTA in [27] is the same as depicted in Fig. 2 excluding the M_{7b}-M_{10b} positive feedback and M_{r1}-M_{r4} transistors. The following biasing condition is needed to make sure that the drain current of M_{3d} and M_{4d} transistors in [27] to be positive.

$$m+1+pq > k_{old}. \tag{29}$$

By assuming the DC current of the tail current source as $2I_b$ in [27], its total bias current excluding the biasing and CMFB circuits is given by

$$I_{total,IRFC,2014} = 2(I_{D1}+I_{D1a}+I_{D9}+I_{D9a}) = I_b\left[\frac{2(m+1)+p(1+q)}{m+1}\right]. \tag{30}$$

Therefore, according to the relations (4) and (30), we have

$$I_{total} = I_{total,IRFC,2014}$$
$$=> \quad I_b = I_a\frac{2(m+1)(n+1)+p(1+q+n)}{[2(m+1)+p(1+q)](n+1)}. \tag{31}$$

The differential and symmetric slew rate of the IRFCA in [27] is given by (32) provided that the condition in relation (33) is satisfied.

$$SR_{diff,IRFC,2014} = \frac{2pqI_b}{C_L} \times \frac{3(m+1)-pq+k_{old}}{2(m+1)} \tag{32}$$

$$k^2_{old} + k_{old}[(3m+2)-2pq] + (m+1) + pq[1-3(m+1)+pq] = 0. \tag{33}$$

Hence, according to the relations (11) and (32) and by assuming the same current mirrors' ratios for the proposed IRFC and IRFC 2014 amplifiers except k, which is separately calculated for symmetric slew rate

in each OTA, the slew rate of the suggested OTA and IRFCA in [27] is related as

$$\frac{SR_{diff}}{SR_{diff,IRFC,2014}} = \frac{I_a \times [3(m+1)(n+1) + k(n+1) - pq]}{I_b \times (n+1)[\,3(m+1) - pq + k_{old}\,]} \tag{34}$$

By considering the equal aspect ratio in input differential pair transistors in the suggested OTA and IRFCA in [27], the gm of their input transistors is associated as follows.

$$\frac{g_{m1}}{g_{m1,IRFC,2014}} = \sqrt{\frac{2\mu_p C_{ox}(W/L)_1 \frac{I_a}{2}}{2\mu_p C_{ox}(W/L)_{1,old} \frac{I_b}{2}}} = \sqrt{\frac{I_a}{I_b}} = \sqrt{\frac{[2(m+1)+p(1+q)](n+1)}{2(n+1)(m+1)+p(1+q+n)}} \tag{35}$$

Hence, according to the relations (13) and (35), the overall transconductance of the suggested OTA in terms of that of the IRFCA in [27] is as follows

$$\frac{G_m}{G_{m,IRFC,2014}} = \frac{k(1-n)+pq+(1-n)(1-m)}{(1-n)[(1-m)+k_{old}+pq\,]} \times \sqrt{\frac{(2(m+1)+p(1+q))(n+1)}{2(m+1)(n+1)+p(1+q+n)}}. \tag{36}$$

Therefore, the unity-gain bandwidth and DC gain of the suggested amplifier in terms of those of the IRFCA in [27] are obtained as

$$\frac{A_{dc}}{A_{dc,IRFC,2014}} \approx \frac{\omega_t}{\omega_{t,IRFC,2014}} \approx \frac{G_m}{G_{m,IRFC,2014}} = \frac{(1-m)(1-n)+k(1-n)+pq}{(1-n)[(1-m)+k_{old}+pq\,]} \times \sqrt{\frac{(2(m+1)+p(1+q))(n+1)}{2(n+1)(m+1)+p(1+q+n)}}. \tag{37}$$

4. Circuit level design and simulation results

To examine the performance of the suggested IRFC OTA, extensive circuit level simulation results are gathered using Cadence Spectre-RF with 1.2 V power supply and 65 nm TSMC CMOS technology. The conventional FCA and the IRFCA in [27], which is called here IRFCA-2014, have been also designed and simulated at the same conditions. All OTAs have been designed for a delayed switched-capacitor (SC) integrator with identical 5 pF integrating and sampling capacitors. The effective load capacitance of all designs was 5 pF in both AC and transient simulations. The OTAs are designed with almost equal power dissipation and similar aspect ratio in input differential pair transistors.

In designing the suggested IRFCA and the IRFCA-2014, the same current mirror ratios are chosen except k which is different to have a symmetric slew rate in both OTAs. The current mirror ratios are selected as $p = 1$, $q = 2.5$, $m = n = 0.5$ and k is chosen 2.25 and 2 in the proposed IRFCA and the IRFCA-2014, respectively. In selecting the ratio of different active current mirrors, several design issues should be considered. As shown in Fig. 2, there are five different parameters as k, m, n, p, and q which have been already defined in relation (1). These five parameters are dependent and only four of them are independent. The value of parameters m and n, which are the ratio of cross-coupled positive feedback transistors aspect ratio to the diode-connected ones, are chosen according to the related trade-off between the DC gain, unity-gain bandwidth, and stability. Besides, owing to the mismatch of transistors, some design margin should be considered here. The value of m and n should be less than one in order to prevent from any latching up. Larger values of m and n result in more DC gain and gain bandwidth, but it reduces the phase margin, and so, the stability in the closed-loop configuration. Therefore, their values should be selected by considering the trade-off between the stability and enhanced performance. So, $m = n = 0.5$ is considered here to compromise between the total small-signal transconductance (G_m) enhancement and sufficient stability.

The other ratio parameters, k, p, and q, are selected such that the total small-signal transconductance and slew rate are enhanced while achieving a symmetric slew rate by satisfying the relation (10) and also considering the DC biasing condition in relation (3). Therefore, the optimal selection of k, p, and q should be also considered by the existing trade-off between the performance improvement of the OTA and phase margin degradation while considering the DC biasing condition in (3) and balanced slewing behavior condition in (10).

All transistors with three times of the minimum channel length are chosen to increase the DC gain while achieving the high-speed operation. The same CMFB and biasing circuits have been utilized in the simulated OTAs. The input and output CM voltages are set to 0.5 V and 0.6 V, correspondingly. Table 1 summarizes the device values of the simulated amplifiers as well as the drain bias current of MOS transistors in the main amplifiers. The value of I_b in Fig. 3 is 5 μA.

The open-loop simulated frequency response of the targeted amplifiers is depicted in Fig. 4. The DC gain of the suggested IRFC OTA, IRFCA-2014 and conventional folded-cascode OTA is 68.9 dB, 61.8 dB,

Table 1
Size of devices in the simulated OTAs.

Device	Proposed IRFCA		IRFCA 2014 [27]		FCA	
	(M × W/L)	I_D (μA)	(M × W/L)	I_D (μA)	(M × W/L)	I_D (μA)
$M_{1,2}$	4 × 3.0 μm/180 nm	104.8	4 × 3.0 μm/180 nm	91.63	8 × 3.0 μm/180 nm	194.1
$M_{1a,2a}$	4 × 3.0 μm/180 nm	99.36	4 × 3.0 μm/180 nm	86.12	–	
$M_{3,4}$	9 × 1.0 μm/180 nm	162.4	8 × 0.7 μm/180 nm	122.6	8 × 3.0 μm/180 nm	393.1
$M_{3a,4a}$	4 × 1.0 μm/180 nm	67.67	4 × 0.7 μm/180 nm	58.65	–	
$M_{3b,4b}$	2 × 1.0 μm/180 nm	31.69	2 × 0.7 μm/180 nm	27.46	–	
$M_{3c,4c}$	4 × 1.0 μm/180 nm	67.97	4 × 0.7 μm/180 nm	58.90	–	
$M_{3d,4d}$	5 × 1.0 μm/180 nm	56.52	5 × 0.7 μm/180 nm	117.2	–	
$M_{5,6}$	9 × 1.8 μm/180 nm	114.1	8 × 1.5 μm/180 nm	148.1	8 × 2.0 μm/180 nm	197.2
$M_{5a,6a}$	4 × 1.8 μm/180 nm	67.67	4 × 1.5 μm/180 nm	58.65	–	
$M_{5b,6b}$	2 × 1.8 μm/180 nm	31.69	2 × 1.5 μm/180 nm	27.46	–	
$M_{5c,6c}$	4 × 1.8 μm/180 nm	67.97	4 × 1.5 μm/180 nm	58.90	–	
$M_{7,8}$	10 × 6.0 μm/180 nm	114.1	10 × 8.0 μm/180 nm	148.1	10 × 10 μm/180 nm	197.2
$M_{7a,8a}$	4 × 6.0 μm/180 nm	45.36	4 × 8.0 μm/180 nm	58.89	–	
$M_{7b,8b}$	2 × 6.0 μm/180 nm	22.60	–	–	–	
$M_{9,10}$	10 × 1.4 μm/180 nm	114.1	10 × 1.8 μm/180 nm	148.2	10 × 2.8 μm/180 nm	197.2
$M_{9a,10a}$	4 × 1.4 μm/180 nm	45.36	4 × 1.8 μm/180 nm	58.90	–	
$M_{9b,10b}$	2 × 1.4 μm/180 nm	22.60	–	–	–	
M_{11}	18 × 7.7 μm/0.5 μm	408.3	16 × 7.6 μm/0.5 μm	355.5	18 × 7.3 μm/0.5 μm	388.2
$M_{r1,r2}$	1 × 1.20 μm/60 nm	–	–	–	–	–
$M_{r3,r4}$	1 × 1.20 μm/60 nm	–	–	–	–	–

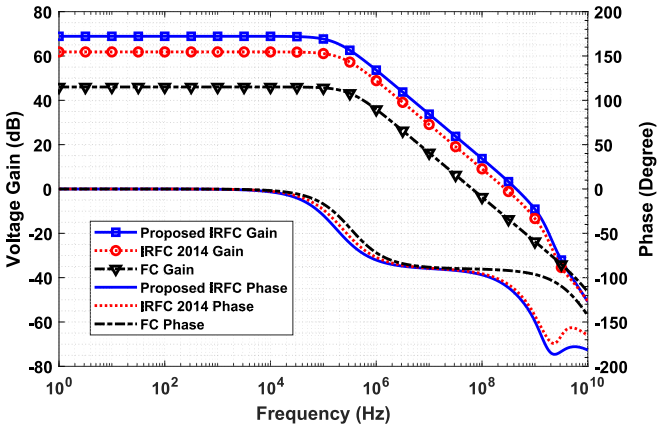

Fig. 4. Open-loop simulated frequency response of the amplifiers.

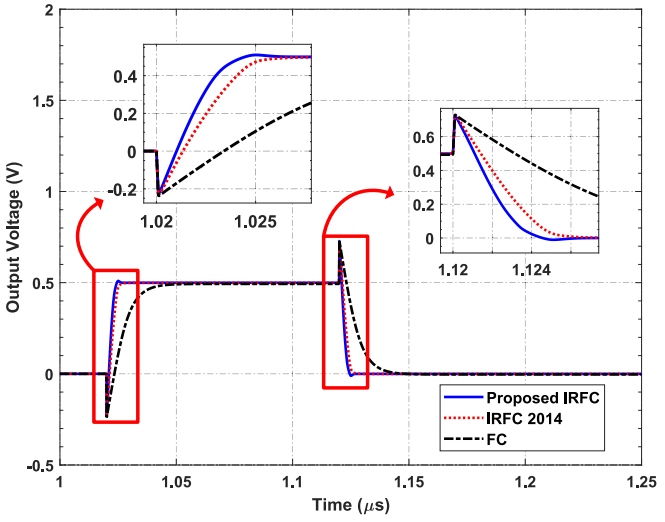

Fig. 5. Simulated transient response of the amplifiers (switching period = 100 ns).

Table 2
Simulation results summary in typical process condition.

Parameter	Proposed IRFCA	IRFCA-2014 [27]	FCA
Power dissipation including bias circuit (μW)	977.6	981.8	982.6
Current consumption including bias circuit (μA)	814.7	818.2	818.8
DC gain (dB)	68.9	61.8	46.0
Unity-gain bandwidth (MHz)	443.4	278.8	65.6
Phase margin (degree)	61.0	74.4	89.9
Average slew rate (V/μs)	255.1	194	74.7
Positive settling time (ns)	7.3	10.9	57.8
Negative settling time (ns)	7.4	10.9	58.8
Average settling time (ns)	7.4	10.9	58.3
Noise PSD (nV/√Hz) @ 100 kHz	32.0	31.0	32.3
FoM_1 (MHz × pF/mA)	2721	1704	401
FoM_2 ((V/μs) × pF/mA)	1566	1186	456
Technology	65 nm TSMC CMOS		
V_{DD} (V)	1.2 V		
Effective load capacitance, C_L (pF)	5 pF		

and 46.0 dB, correspondingly. Also, the phase margin of the proposed IRFCA, IRFCA-2014 and FCA is 61.0°, 74.4° and 89.9°, respectively. This simulation shows a DC gain improvement about 7.1 dB and 22.9 dB in comparison with IRFCA-2014 and FCA, respectively. The unity-gain

Table 3
Calculated and simulated parameters of the proposed IRFC respected to the FCA and IRFCA 2014.

Parameter	Respect to			
	IRFCA 2014 [27]		FCA	
	Calculation	Simulation	Calculation	Simulation
I_a	$1.15 \times I_b$	$1.13 \times I_b$	$1.06 \times I_c$	$1.05 \times I_c$
A_{dc}	$1.66 \times A_{dc,IRFC,2014}$	$2.26 \times A_{dc,IRFC,2014}$	$8.49 \times A_{dc,fc}$	$13.96 \times A_{dc,fc}$
ω_t	$1.66 \times \omega_{t,IRFC,2014}$	$1.59 \times \omega_{t,IRFC,2014}$	$8.49 \times \omega_{t,fc}$	$6.76 \times \omega_{t,fc}$
SR	$1.46 \times SR_{IRFC,2014}$	$1.32 \times SR_{IRFC,2014}$	$4.48 \times SR_{fc}$	$3.41 \times SR_{fc}$

Table 4
Suggested IRFCA simulated results in diverse process and temperature conditions.

Parameter	TT @ 27 °C	SS @ 85 °C	FF @ −40 °C
Power dissipation (μW)	977.6	963.7	987
DC gain (dB)	68.9	67.6	69.5
Unity-gain frequency (MHz)	443.4	386.5	551.0
Phase margin (degree)	61.0	60.8	61.5
Average slew rate (V/μs)	255.1	241.3	265.2
Positive settling time (ns)	7.3	8.0	6.8
Negative settling time (ns)	7.4	8.0	6.9
Average settling time (ns)	7.4	8.0	6.9
Noise PSD (nV/√Hz) @ 100 kHz	32.0	33.4	29.7
FoM_1 (MHz × pF/mA)	2721	2406	3350
FoM_2 ((V/μs) × pF/mA)	1566	1502	1612

bandwidth of the suggested IRFCA, IRFCA-2014 and FCA is 443.4 MHz, 278.8 MHz and 65.6 MHz, respectively. In overall, the DC gain, unity-gain frequency, and slew rate of the proposed OTA are improved about 22.9 dB, 6.8 times, and 3.4 times, respectively, compared to the traditional FCA. In comparison with IRFCA-2014, these improvements are 7.1 dB, 1.6 times, 1.3 times, respectively.

The transient step response of the simulated amplifiers is illustrated in Fig. 5. In this simulation, the average settling time of the OTAs is 7.4 ns, 10.9 ns and 58.3 ns for the proposed OTA, IRFCA in [27], and conventional FCA, respectively. The simulation results of designed OTAs are presented in Table 2. For a fair comparison, two small-signal and large-

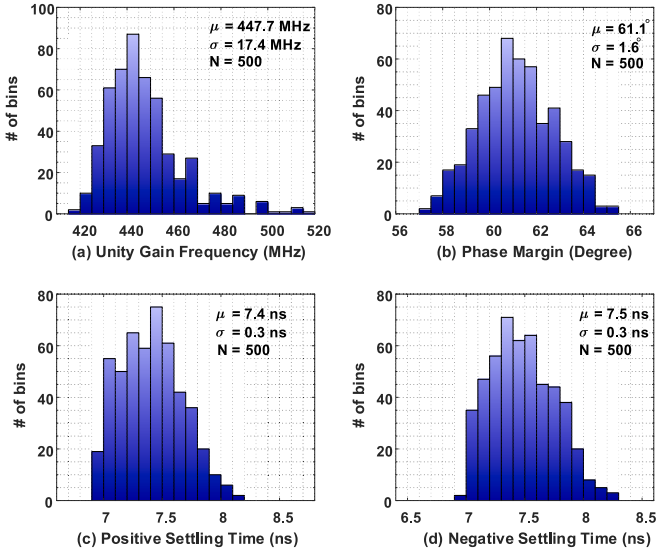

Fig. 6. Statistical distribution of (a) unity-gain bandwidth, (b) phase margin, (c) positive settling time, and (d) negative settling time of the suggested OTA in Monte Carlo simulations with 500 runs.

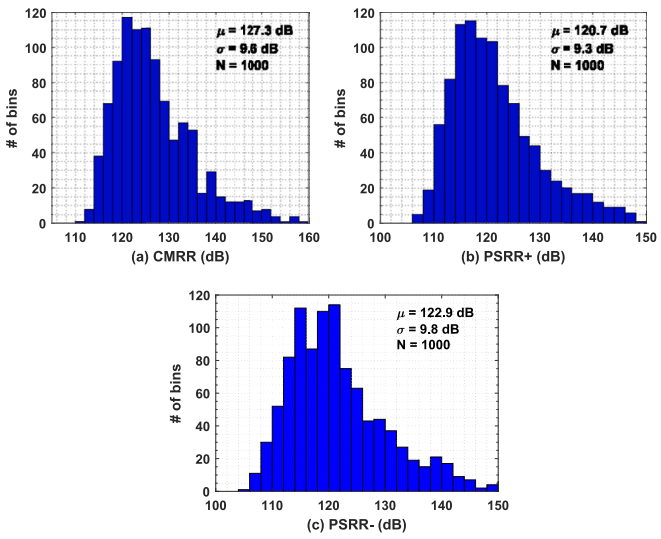

Fig. 7. Monte Carlo simulation results of (a) CMRR, (b) positive PSRR, (c) and negative PSRR of the proposed OTA at DC.

signal figures of merits (FoMs) defined as

$$FoM_1 = \frac{UGF\,(MHz) \times C_L(pF)}{I_T(mA)} \tag{38}$$

$$FoM_2 = \frac{SR(V/\mu s) \times C_L(pF)}{I_T(mA)} \tag{39}$$

are employed where I_T is the total current dissipation of OTA including the biasing circuit. To provide a more tangible view, the performance enhancement resulting from simulation and analytical calculations are shown in Table 3. Also, the simulated results of the suggested IRFCA in diverse temperature and process corner cases are illustrated in Table 4.

To examine the stability and robustness performance of the suggested OTA, several Monte Carlo simulations with 500 runs have been done. In these simulations, the process variations and device mismatches have been considered. Fig. 6 shows the statistical distribution of unity-gain frequency, phase margin, positive and negative settling time of the suggested OTA. As it is observed, the suggested IRFC OTA has sufficient robustness.

The Monte Carlo simulation results of CMRR and both positive and negative power supply rejection ratios (PSRR) of the proposed OTA are illustrated in Fig. 7. In these simulations, the effects of both process variations and device mismatches have been considered using the foundry process design kit. The achieved values of CMRR, PSRR+, and PSRR- are about 127.3 dB, 120.7 dB, 122.9 dB, respectively.

In Table 5, a comparison with several class A amplifiers, which are based on improvements of the folded-cascode OTA, is provided. As it is clear, in overall, the proposed OTA has outstanding results. It is also worth mentioning that the proposed amplifier has been designed for switched-capacitor applications with small settling error while in most of works listed in Table 5, the settling error is much larger and it is around 1 % which is not applicable in high accuracy SC circuits such as integrators and gain stages that are utilized in high-resolution sigma-delta modulators and pipelined analog-to-digital converters (ADCs). Actually, our goal of the simulated design prototype was not to achieve the highest performance among the current state-of-the-art OTAs. Instead, this design has been done to verify the analysis and usefulness of the proposed OTA structure and its improvements compared to the simulated OTAs in this paper. Indeed, the comparison of OTAs should be done in similar design conditions as we did in this paper for three different OTAs. The proposed OTA can be also designed in similar conditions such as [36] with much more improved FoMs than reported here.

5. Conclusions

An improved recycling FCA has been suggested in this paper. The local positive feedback, current recycling, and high speed active current mirror techniques are used to realize a three-path single-stage OTA with improved large and small signal behaviors. The analytical calculations and simulated results prove the substantial benefit and improved results of the suggested OTA. According to the simulation results, DC gain, unity-gain bandwidth, and slew rate of the proposed OTA are substantially improved compared to the traditional FCA resulting in 688 % smaller settling time with almost the same power consumption, capacitive load, feedback factor, and settling error. The suggested IRFCA would be employed in high sampling frequency ADCs where a fast-settling OTA is needed. For future research, a systematic design

Table 5
Performance comparison of the proposed OTA with several works.

Parameter	Proposed	[21]	[24]	[27]	[31]	[39]	[41]	[28]	[47]	[50]	[53]
Publication Year	2024	2009	2012	2014	2015	2019	2019	2020	2020	2022	2024
Supply voltage (V)	1.2	1.8	1	1.2	1.2	1.2	0.6	1.2	±0.25	1.8	0.8
Technology (nm)	65	180	65	90	90	180	180	90	180	180	180
Load capacitance (C_L), (pF)	5	5.6	10	5	5	10	15	10	15	10	10
DC gain (dB)	68.9	53.6	54.5	59.8	59.1	75	71	68.6	79.5	80.1	76.6
Unity-gain frequency (MHz)	443.4	134.2	203.2	348.1	650	185	0.018	360	0.037	47.0	6.78
Phase margin (degree)	61.0	70.6	66.2	62.2	50	71	74	77	64	69.1	72.1
Average slew rate (V/μs)	255.1	94.1	87.85	173	115.2	99	0.0066	61	0.011	66.4	3.48
Average settling time (ns)	7.4	11.2	10.1	10.1	9.6	5	835,500	10	N/A	31.4	86.5
δ = Settling Error	$\delta = 0.01$ %	$\delta = 1$ %	$\delta = 1$ %	$\delta = 0.01$ %	$\delta = 0.1$ %	$\delta = 1$ %	$\delta = 0.01$ %	$\delta = 1$ %		$\delta = 1$ %	$\delta = 1$ %
Input-referred noise voltage	32.0 nV/√Hz @ 100 kHz	48.5 μVrms	25.8 μVrms	34.9 nV/√Hz @ 100 kHz	42.7 nV/√Hz @ 100 kHz	54 μVrms	257 nV/√Hz @ 0.1 Hz	64 μVrms	910 nV/√Hz @ 1 kHz	13.2 nV/√Hz @ 1 MHz	66.4 nV/√Hz @ 100 kHz
Power dissipation (μW)	977.6	1440	1440	851.9	580	840	0.144	1440	0.06	433	27.2
Current consumption (μA)	814.7	800	800	709.9	483.3	700	0.24	1200	0.12	240.5	34
FoM_1 (MHz × pF/ mA)	2721	939	2540	2452	6725	2643	1125	3000	4625	1954	1994
FoM_2 (V/μs × pF/ mA)	1566	659	1098	1218	1192	1414	413	508	1350	2760	1023

procedure can be developed to optimize the selection of different active current mirror ratios in order to further improve both small and large signal performance of the proposed OTA.

CRediT authorship contribution statement

Mohammad Yavari: Writing – review & editing, Writing – original draft, Visualization, Validation, Supervision, Software, Resources, Project administration, Methodology, Investigation, Funding acquisition, Formal analysis, Conceptualization. **Mohammadamin Mohtashamnia:** Validation, Software, Formal analysis.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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