ELectronics EXpress

IEICE Electronics Express, Vol.6, No.7, 395–402

A new class AB folded-cascode operational amplifier

Mohammad Yavari[a)]

Integrated Circuits Design Laboratory, Department of Electrical Engineering, Amirkabir University of Technology, Tehran, Iran

a) *myavari@aut.ac.ir*

Abstract: This paper presents a new class AB folded-cascode operational amplifier in standard CMOS technology for fast-settling switched-capacitor circuits. The proposed amplifier employs the class AB operation in both nMOS and pMOS output current source transistors by employing only a few passive components without any extra static power dissipation and results in large slew rate, enhanced unity-gain bandwidth and DC gain, and reduced input-referred noise compared to the conventional folded-cascode amplifier. Circuit level analysis and simulation results are provided to verify the effectiveness of the proposed amplifier.

Keywords: operational amplifiers, class AB, switched-capacitor circuits

Classification: Integrated circuits

References

[1] M. Taherzadeh-Sani, R. Lotfi, and O. Shoaei, "Pseudo-class-AB telescopic cascode operational amplifier," *Electron. Lett.*, vol. 40, no. 4, Feb. 2004.

[2] R. G. Carvajal, A. Torralba, J. Ramirez-Angulo, J. Tombs, and F. Monuz, "Low-voltage class AB output stages for CMOS op-amps using floating capacitors," *IEEE Int. Symp. Circuits Syst.*, vol. 1, pp. 13–16, 2001.

[3] J. Ramirez-Angulo, R. G. Carvajal, J. A. Galan, and A. Lopez-Martin, "A free but efficient low-voltage class AB two-stage operational amplifier," *IEEE Trans. Circuits Syst. II, Expr. Briefs*, vol. 53, no. 7, pp. 568–571, July 2006.

[4] M. Yavari, "Hybrid cascode compensation for two-stage CMOS opamps," *IEICE Trans. Electron.*, vol. E88-C, no. 6, pp. 1161–1165, June 2005.

1 Introduction

Operational amplifiers are widely used in analog and mixed-signal integrated circuits such as switched-capacitor (SC) integrators, gain-stages, etc. In high accuracy SC circuits, they must drive large capacitive loads especially when operating from a low supply voltage. On the other hand, in high-speed applications the amplifier is needed to settle within a definite short time period. In such applications, a class A operational amplifier needs high dc current in order to achieve large slew-rate as well as high unity-gain bandwidth. However,

DOI: 10.1587/elex.6.395
Received January 15, 2009
Accepted February 20, 2009
Published April 10, 2009

in class AB amplifiers since the slew rate does not depend on the quiescent current and large currents are generated during slewing, a fast-settling circuit is achieved with low static power dissipation. Therefore, unlike the class A amplifiers, there is no tradeoff between the static power dissipation and slewing behavior in class AB amplifiers.

The general structure of a class AB output stage is shown in Fig. 1 (a) where a floating DC voltage source is connected between the gate terminals of transistors M1 and M2 operating as common source amplifiers. In this circuit, when a small input signal is applied, both transistors operate at the saturation region and hence the effective transconductance is $g_{m1}+g_{m2}$ where g_{m1} and g_{m2} are the transconductance of M1 and M2, respectively. Therefore, both DC gain and unity-gain bandwidth of a class AB output stage amplifier are greater than those of a class A one by $(1+g_{m2}/g_{m1})$ ratio with the same static power dissipation.

Nonetheless, the main advantage of a class AB amplifier is its high current driving capability during slewing and hence its large slew rate. When a large input signal is applied to the circuit shown in Fig. 1 (a), the bias current of one of the output transistors is considerably increased and the other transistor turns off. For example, in the presence of a large positive input step, the bias current of M1 is increased while M2 enters the cut-off region. Hence, the load capacitor is discharged by a current that is much greater than the quiescent current of the amplifier.

The class AB output stage shown in Fig. 1 (a), however, needs an extra circuit to realize the floating DC voltage source. One solution is shown in Fig. 1 (b) [1]. In this circuit, the gate of M2 is connected to a bias voltage, $V_{\rm b}$, when the amplifier is idle and a capacitor is used to implement the floating voltage source. This is possible in the circuits where the amplifier is reset in one of two non-overlapping clock phases such as SC gain-stages. However, this solution cannot be employed in SC circuits where the amplifier is not idle in any of clock phases such as SC integrators which are widely used in sigma-delta modulators.

Figure 1 (c) illustrates another solution called the dynamic level shifting to implement the output stage class AB operation [2]. In this circuit, the capacitor $C_{\rm b1}$ is used to realize the floating DC voltage source. To define and refresh the DC voltage across the capacitor $C_{\rm b1}$, a simple SC circuit comprising of the capacitor $C_{\rm b2}$ and the switches controlled by two non-overlapping clock phases, ϕ_1 and ϕ_2, is utilized. Although, this circuit can be employed in all of the switched-capacitors circuits, however, it needs another extra capacitor and two non-overlapping clock phases. Alternatively, the static DC level shifting can be employed to build the class AB output stage where a voltage buffer is used to realize the floating voltage source [2]. However, this technique adds a low frequency pole and zero pair to the system and hence results in a degraded small signal settling behavior. To move the added pole and zero to high frequencies a large bias current is needed in DC level shifting transistors.

To define the gate DC voltage of M2 a large resistor can be used as shown

DOI: 10.1587/elex.6.395
Received January 15, 2009
Accepted February 20, 2009
Published April 10, 2009

in Fig. 1 (d) [3]. In this circuit, the gate bias voltage of M2 is always connected to $V_{\rm b}$ since there is no DC current through $R_{\rm b}$ and the DC voltage across the capacitor $C_{\rm b}$ is also properly defined. The value of $R_{\rm b}$ must be large enough to prevent any signal attenuation from $V_{\rm in}$ to the gate of M2. Although this technique adds a low frequency pole and zero pair to the circuit, however, by employing a very large resistor they are located at very low frequencies (on the order of a few hertzs or lower) and hence the amplifier can also be used in very wideband applications.

In this paper, a novel single-stage class AB folded-cascode operational amplifier is proposed. The class AB operation is utilized in the output current source transistors by employing a floating capacitor and a very large resistor.

2 Conventional class A folded-cascode amplifier

In order to compare the performance of the proposed amplifier with the conventional single-stage class A folded-cascode amplifier shown in Fig. 1 (e), several analysis results are provided here. The DC gain, unity-gain bandwidth, non-dominant pole, and slew rate of this amplifier are respectively given by:

$$A_{dc} = g_{m1}R_{out}, \quad \omega_t = \frac{g_{m1}}{C_L}, \quad \omega_{p2} = \frac{g_{m5}}{C_P}, \quad SR = \frac{2I_{D1}}{C_L} \tag{1}$$

where g_{m1} and g_{m5} are the transconductance of M1 and M5, respectively. R_{out} is the resistance seen from each output node to the ground. C_L is the load capacitor and C_P is the total parasitic capacitor at the source of M5. I_{D1} is the bias current of the input transistors, M1 and M2. It is worth mentioning that in driving the slew rate, an equal bias current for input and cascode transistors was assumed. This is necessary to achieve a fast-settling folded-cascode amplifier since in this case the drain voltage of input transistors do not change considerably during slewing. The total input-referred thermal noise voltage per unit bandwidth of the conventional folded-cascode amplifier is given by:

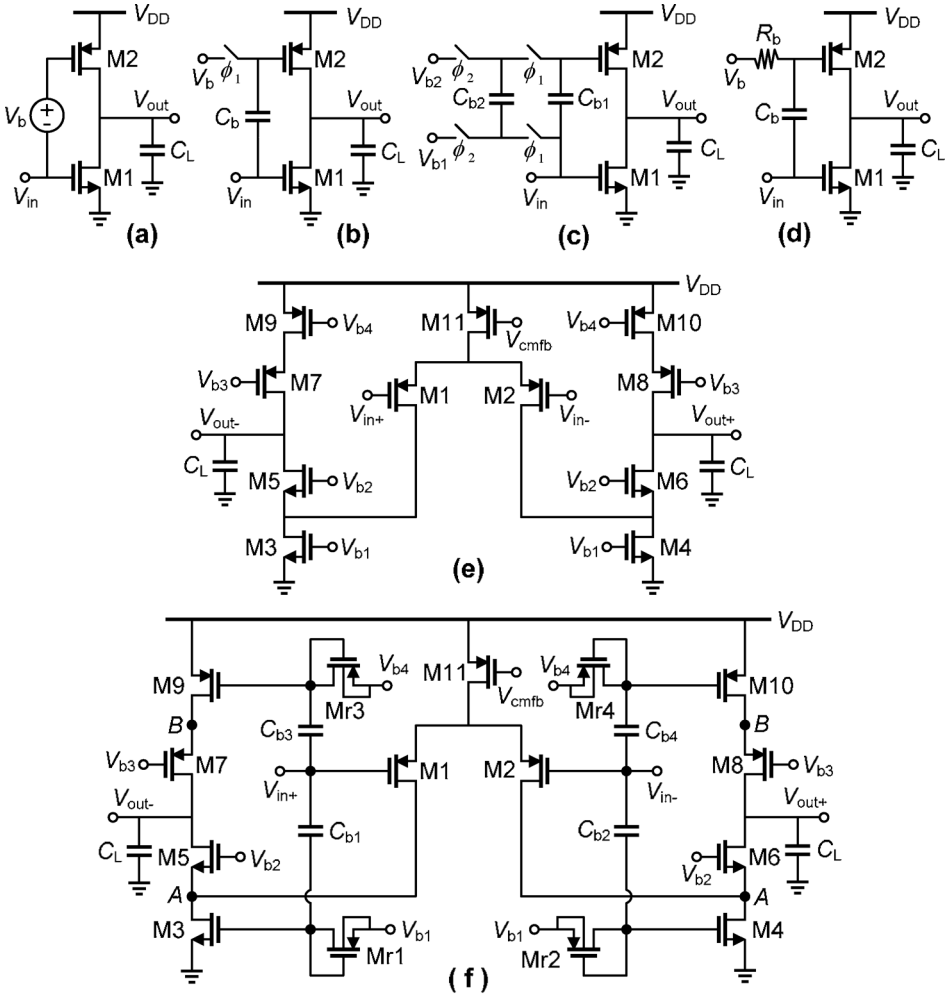
$$v_n^2 = 8\,kT\gamma\frac{1}{g_{m1}}\left(1 + \frac{g_{m3}}{g_{m1}} + \frac{g_{m9}}{g_{m1}}\right) \tag{2}$$

where γ is the noise enhancement factor of short channel transistors.

3 Proposed class AB folded-cascode amplifier

Figures 1 (f) shows the proposed single-stage class AB folded-cascode amplifier. To build the class AB operation, the solution presented in Fig. 1 (d) was used. The input signal is coupled through capacitors C_{b1}, C_{b2}, C_{b3} and C_{b4} to the gate of both nMOS and pMOS output current source transistors. The gate bias voltage of output current source transistors, and hence the DC voltage across the floating capacitors, are determined by connecting them to the proper bias voltage sources through large resistors realized by diode-connected pMOS transistors Mr1-Mr4. These transistors are biased in the cut-off region and provide a very large resistor with a small aspect ratio.

DOI: 10.1587/elex.6.395
Received January 15, 2009
Accepted February 20, 2009
Published April 10, 2009



Parameter	Value	Parameter	Value
$(W/L)_{1,2}$	10×8μm/0.18μm	$(W/L)_{9,10}$	10×6μm/0.18μm
$(W/L)_{3,4}$	10×6μm/0.18μm	$(W/L)_{11}$	10×10μm/0.2μm
$(W/L)_{5,6}$	10×4μm/0.18μm	$(W/L)_{r1\text{-}4}$	1μm/2μm
$(W/L)_{7,8}$	10×6μm/0.18μm	$C_{b1\text{-}b4}$	2 pF

(g)

Fig. 1. (a) General structure of a class AB output stage, implementation of class AB output stage by (b) a switch and capacitor, (c) dynamic level shifting, (d) a large resistor and capacitor, (e) conventional class A folded-cascode amplifier, (f) proposed class AB folded-cascode amplifier, and (g) simulated device parameters.

The proposed amplifier has a very large slew-rate that is independent of the bias current. Under the quiescent conditions, the current of input and cascode transistors are determined by the bias voltages denoted by $V_{b1} - V_{b4}$ in Fig. 1 (f). These bias voltages are generated by employing a constant current or constant G_m biasing circuitry like any other operational amplifier. However, in the slewing region the drain current of cascode transistors are considerably increased. If for instance $V_{\text{in}+}$ to be much greater than $V_{\text{in}-}$,

DOI: 10.1587/elex.6.395
Received January 15, 2009
Accepted February 20, 2009
Published April 10, 2009

the transistor M2 carries all of the bias tail circuit and forces M1 to enter the cut-off region. Since, the large input signal step is directly coupled to the gate of the output current source transistors; they are subject to a large variation in their gate-source voltage. Therefore, transistors M4 and M9 enter to the cut-off region and the drain current of both M3 and M10 increase significantly. Hence, a large current flows into the positive output node through M10, and on the other hand, the negative output node is discharged by a large current provided by M3. Therefore, a large positive slew rate is achieved that depends on the input signal amplitude and is independent of the bias current. During negative slewing, a similar improvement in the value of slew rate is also obtained. It is worth mentioning that both large and small input signal changes are directly coupled to the gate of the output current source transistors, M3 – M4 and M9 – M10, almost without any delay since between them there is an equivalent lossy capacitive divider network comprising of the capacitors $C_{b1} - C_{b4}$ and the parasitic capacitors seen at the gate terminals of transistors M3, M4, M9, and M10 paralleled with very large resistors realized by transistors Mr1 – Mr4. These RC equivalent circuits generate a DC frequency zero and a low frequency pole which is given by $\omega_p = 1/[R_b(C_b + C_p)]$ where R_b, C_b, and C_p are the resistance realized by each Mr1 – Mr4 transistors, each of the $C_{b1} - C_{b4}$ capacitors, and the total parasitic capacitor at the gate terminal of each M3, M4, M9, and M10, respectively. Since R_b is very large, the resulting frequency response is flat beyond a few hertzs. Therefore, the gate terminals of output current source transistors change similarly as the output nodes, but, with a ratio determined by the feedback factor of the closed-loop circuit which uses the amplifier.

The small-signal transfer function of the proposed amplifier can readily be obtained as follows:

$$A(s) \approx \frac{(g_{m1} + g_{m3})\ R_{out}}{(1 + s/\omega_{out})(1 + s/\omega_A)} + \frac{g_{m9}\, R_{out}}{(1 + s/\omega_{out})(1 + s/\omega_B)} \tag{3}$$

where

$$\omega_{out} = \frac{1}{R_{out}C_L}, \quad \omega_A = \frac{g_{m5}}{C_A}, \quad \omega_B = \frac{g_{m7}}{C_B}.$$

C_A and C_B are the total parasitic capacitors seen at the nodes A and B, respectively. R_{out} is the output resistor. As is seen the proposed amplifier has an extra pair of pole and zero compared to the conventional folded-cascode amplifier. This is because in the proposed amplifier there are three small-signal paths from input to the output where all paths comprise of a cascode configuration (the combination of a common source and a common gate amplifier). Nevertheless, two of these signal paths are common in all nodes and hence do not generate any extra frequency pole and zero. However, the third path constituting from the nodes B and output results in an extra pole and zero where the extra zero is given by:

$$\omega_z = -\frac{(g_{m1} + g_{m3} + g_{m9})\omega_A\omega_B}{(g_{m1} + g_{m3})\omega_A + g_{m9}\omega_B}. \tag{4}$$

DOI: 10.1587/elex.6.395
Received January 15, 2009
Accepted February 20, 2009
Published April 10, 2009

However, by considering $\omega_A = \omega_B$, the small-signal transfer function is simplified as follows where the extra pole and zero cancel each other.

$$A(s) = \frac{(g_{m1} + g_{m3} + g_{m9})\, R_{out}}{(1 + s/\omega_{out})(1 + s/\omega_A)}. \quad (5)$$

It should be noted that the condition required to cancel the extra pole and zero with together can easily be satisfied by appropriate design of the amplifier. Besides, the amplifier is not sensitive to incomplete cancellation of the extra pole and zero because they are located well far away the unity-gain bandwidth provided the load capacitor is very larger than the parasitic capacitors seen at the nodes A and B. Hence, the DC gain, unity-gain bandwidth, and second non-dominant pole of the proposed amplifier are respectively given by:

$$A_{dc} = (g_{m1} + g_{m3} + g_{m9})\, R_{out}, \quad \omega_t = \frac{g_{m1} + g_{m3} + g_{m9}}{C_L}, \quad \omega_{p2} = \frac{g_{m5}}{C_A}. \quad (6)$$

Compared to the relations given in (1), the proposed amplifier has a DC gain and unity-gain bandwidth greater than those of the conventional folded-cascode amplifier by $(1 + g_{m3}/g_{m1} + g_{m9}/g_{m1})$ ratio although their non-dominant pole is the same.

The total input-referred thermal noise voltage per unit bandwidth of the proposed amplifier is given by:

$$v_n^2 = 8kT\gamma \frac{1}{g_{m1}} g_{m3} + g_{m9}. \quad (7)$$

As is seen from the relations (2) and (7), the input-referred noise voltage of the proposed amplifier is much less than that of the conventional folded-cascode amplifier. This is achieved because in the proposed amplifier the current source transistors behave also as the common source amplifiers.

The power supply voltage requirement of the proposed amplifier is the same as the conventional folded-cascode one. To get high output signal swing in low-voltage environments, a two-stage amplifier comprising the proposed class AB amplifier as the first stage can be used. In the second stage, a common-source class AB amplifier can be employed to achieve the highest output signal swing. Thus, a two-stage class AB amplifier with large slew rate and enhanced unity-gain bandwidth and DC gain is achieved. To further improve the linear settling performance of such a two-stage class AB amplifier, the hybrid cascode compensation can be utilized [4].

4 Simulation results

To prove the effectiveness of the proposed amplifier, HSPICE simulation results are performed using a 0.18-μm BSIM3v3 level 49 mixed-signal CMOS technology. The amplifier was designed for a switched-capacitor integrator with sampling and integrating capacitors of 5 pF and 10 pF, respectively. The load capacitor was 7 pF and 3.5 pF in AC open loop and transient closed loop simulations, respectively, which corresponds to an effective load capacitance of 7 pF in both simulations. The device parameters summarized in Fig. 1 (g)

DOI: 10.1587/elex.6.395
Received January 15, 2009
Accepted February 20, 2009
Published April 10, 2009

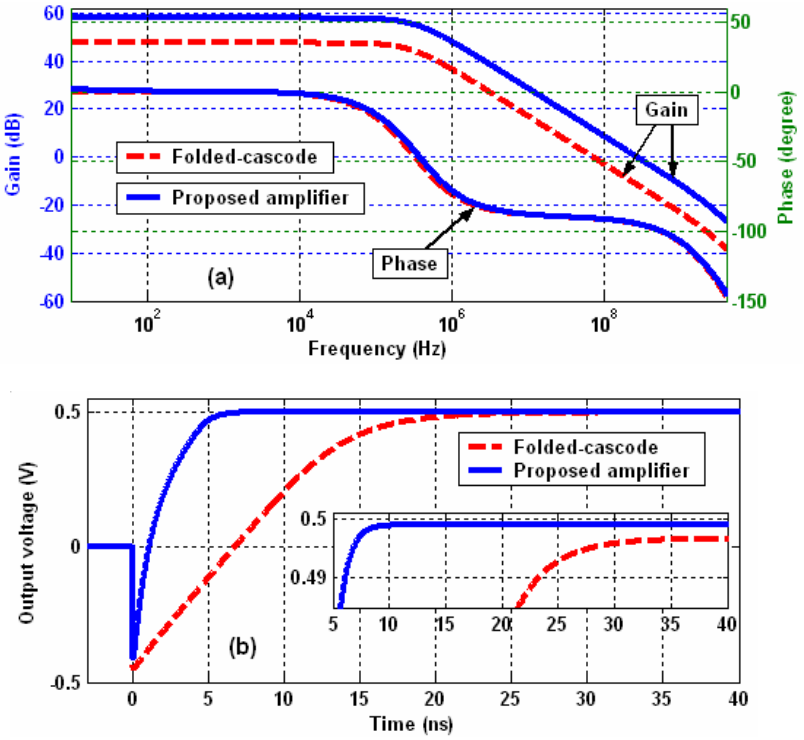


Fig. 2. (a) Open loop small-signal frequency response, and (b) settling response.

Table I. Simulation results summary.

Parameter	Folded-cascode	Proposed amplifier
DC gain	47.4 dB	57.8 dB
Unity-gain bandwidth	74.4 MHz	282.8 MHz
Phase margin (degree)	88.9	85.2
Slew rate (V/μs)	67	685
0.01% settling time (ns)	38.7 ns	10.5 ns
Input-referred noise density @ 100 kHz	89 nV/√Hz −141 $dBV_{rms}/\sqrt{Hz}$	23.1 nV/√Hz −152.7 $dBV_{rms}/\sqrt{Hz}$
Power supply voltage	1.5 V	
Static power dissipation (mW)	2.0 mW including bias circuitry	
Technology	0.18μm BSIM3v3 level 49 mixed-signal CMOS	

was used in the simulations. The conventional folded-cascode amplifier shown in Fig. 1 (e) was also simulated with the same device parameters in order to provide a fair comparison.

Figure 2 illustrates the circuit level simulation results where in Fig. 2 (a) the simulated open loop frequency response is shown. In Fig. 2 (b) the large-signal transient response of both simulated amplifiers to an input step of 1 V differential height is shown. Table I summarizes the simulated results. The proposed amplifier achieves 10.4 dB higher DC gain, 3.8 times larger unity-gain bandwidth and about one order of magnitude larger slew rate than the conventional folded-cascode amplifier as theoretically expected. The large slew rate and enhanced unity-gain bandwidth of the proposed amplifier makes it to settle more rapidly than the conventional folded-cascode amplifier in switched-capacitor circuits. The input-referred noise voltage of the pro-

DOI: 10.1587/elex.6.395
Received January 15, 2009
Accepted February 20, 2009
Published April 10, 2009

posed amplifier is also much less than that of the conventional folded-cascode amplifier.

5 Conclusions

In this paper a novel class AB folded-cascode operational amplifier was proposed. The proposed amplifier achieves large slew rate, increased DC gain and unity-gain bandwidth, and reduced input-referred noise by employing only a few passive components without any extra static power dissipation. It can be used in high-resolution and fast-settling switched-capacitor circuits where driving the large capacitive loads is required.

DOI: 10.1587/elex.6.395
Received January 15, 2009
Accepted February 20, 2009
Published April 10, 2009