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MIXED SIGNAL LETTER

A single-stage operational amplifier with enhanced transconductance and slew rate for switched-capacitor circuits

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Abstract In this paper, a single-stage multi-path operational amplifier for fast-settling switched-capacitor circuits is presented. The proposed amplifier uses all idle devices in the conventional folded-cascode amplifier in the signal path and the positive feedback cross-coupled transistors to enhance both the small-signal and large-signal parameters. It significantly improves the DC gain, unity-gain bandwidth, and slew rate compared to the conventional folded-cascode amplifier with the same power consumption and input parasitic capacitance. Extensive circuit level analysis and simulation results using a 90 nm CMOS technology are provided to evaluate the usefulness of the proposed amplifier.

Keywords CMOS operational amplifiers · Folded-cascode OTA · Switched-capacitor circuits · Fast-settling

1 Introduction

The operational transconductance amplifiers (OTAs) are widely used in the analog and mixed-signal integrated circuits such as switched-capacitor (SC) integrators, gain-stages, etc., to realize high-accuracy analog-to-digital (A/D) converters. In high-accuracy A/D converters, the operational amplifiers are needed to drive large capacitive loads especially when they are operating from a low supply voltage which is mandated in nano-meter CMOS technologies. On the other hand, in high-speed applications, the amplifier is needed to settle within a definite short time period with the required accuracy. In such applications, the amplifier needs to provide high DC gain and unity-gain bandwidth and large slew rate.

The folded-cascode amplifier (FCA) is usually employed in low-voltage applications either as a single-stage or as the first stage in multistage amplifiers since it achieves high DC gain and relatively large output signal swing. In addition, the pMOS input pair is preferred over the nMOS one due to its lower flicker noise, higher non-dominant pole, and lower input common-mode voltage [1]. Nonetheless, in FCA shown in Fig. 1, to achieve a symmetric slewing behavior, the equal bias current is needed in input and cascode transistors. As a result, the transistors M_3 and M_4 draw the most current while acting only as the current sources without any signal amplification.

Several techniques have been proposed to enhance the performance of folded-cascode amplifier such as the multi-path schemes [2, 3], the recycling folded-cascode amplifier [4, 5], and several modifications of the recycling folded-cascode amplifier [6–8]. In [2], the output current source active loads, M_7–M_{10}, are changed into active current mirrors. A complementary folded-cascode amplifier comprising of two input pairs is presented in [3] to exploit both nMOS and pMOS cascode transistors in the signal path. Moreover in [3], a three-path amplifier comprising of one folded-cascode, one current-mirror, and one current-mirror folded-cascode amplifier is presented.

In [4], the transistors M_1–M_4 are split and the added input pair drives M_3 and M_4 through diode-connected transistors to make a two-path amplifier comprising of one folded-cascode and one current-mirror amplifier. This is called the recycling technique and it was firstly presented in [9] for a current-mirror amplifier to enhance the output impedance and slew rate. In [5], the authors provide a detailed analysis and experimental results of the original

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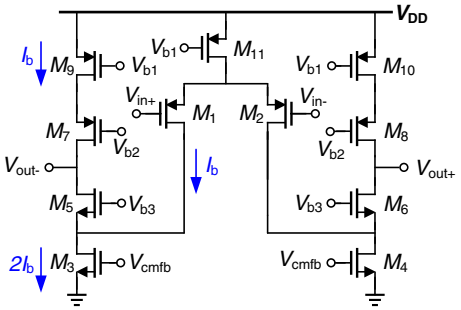

Fig. 1 Conventional folded-cascode operational amplifier

recycling folded-cascode amplifier presented in [4]. It is shown that compared to the conventional FCA, the recycling folded-cascode amplifier achieves almost twice the bandwidth and better than twice the slew rate for the same area and power budgets and capacitive load. Moreover, the DC gain is also improved about 7.6 dB.

In [6], an improved recycling structure is proposed to separate the AC path from the DC one resulting in further enhanced unity-gain bandwidth and DC gain. This is achieved by adding two current sources to the drains of additional input pair steering some of the DC current from the active current mirrors as was already utilized in literature such as [10] and more developed in [11]. In [7], the double recycling technique was utilized to convert the added current source transistors in [6] into the signal path by employing an additional input pair. This results in higher DC gain and unity-gain bandwidth compared to the improved recycling folded-cascode amplifier with the same area and power budgets. In [8], instead of using two current sources in [6], two cross-coupled transistors were connected to the drains of the additional input pair transistors in the recycling folded-cascode amplifier. This provides a positive feedback path resulting in a boosted small-signal transconductance. Compared to the recycling folded-cascode amplifier, this technique improves the DC gain, unity-gain bandwidth, and slew rate without any increasing the power consumption and die area.

However, in all of the above-mentioned techniques, the current of either the pMOS or the nMOS output current source transistors is fixed, and hence, in the fully-differential structure, a small slew rate is achieved. Indeed, most of them are using the single-ended scheme to achieve the symmetric slewing behavior. In [12], a single-stage class AB three-path fully-differential amplifier is presented by using the flipped-voltage follower (FVF) cell [13] to build the class AB operation. In this circuit, both pMOS and nMOS current source transistors in the conventional folded-cascode amplifier are used in the signal path. Although, it results in a significantly enhanced unity-gain bandwidth and DC gain and large slew rate, however, like to all input-stage class AB amplifiers, the common-mode rejection ratio (CMRR) is degraded since the output resistance of the input tail current source is very smaller than that of the conventional class A input-stage amplifiers. This was owing to the use of FVF cell to realize a class AB operation to achieve a large slew rate. In this paper, an alternative technique was utilized to boost the slew rate in fully-differential amplifiers without using a FVF cell. This technique also improves the small-signal performance of the amplifier as well.

The paper is organized as follows. Section 2 describes the structure of the proposed amplifier and provides an extensive analysis. The proposed amplifier is compared with the conventional FCA in Sect. 3. In Sect. 4, two simplified structures of the proposed amplifier are presented and compared. Section 5 provides the circuit level simulation results, and finally, the conclusions are given in Sect. 6.

2 Proposed multi-path operational amplifier

In this Sect., firstly the structure of the proposed amplifier is described, and then, the analysis of slew rate, small-signal transconductance, DC gain, unity-gain bandwidth, and frequency poles and zeros are presented.

2.1 Proposed OTA structure

Figure 2 shows the structure of the proposed operational amplifier. The transistors M_1–M_{11} realize the conventional folded-cascode amplifier. The pMOS input transistors are split as M_1, M_{1a}, M_2, and M_{2a} to provide a path from the input into the nMOS current source transistors, M_3 and M_4 in the conventional FCA similar to [4]. This is intended to bring the nMOS current source transistors into the signal path. Besides, the nMOS current source transistors, M_3 and M_4 are split into M_3, M_{3a}, M_4, and M_{4a} to make a two path amplifier. Transistors M_{3b} and M_{4b} realize a positive feedback network at the gates of M_3 and M_4, respectively.

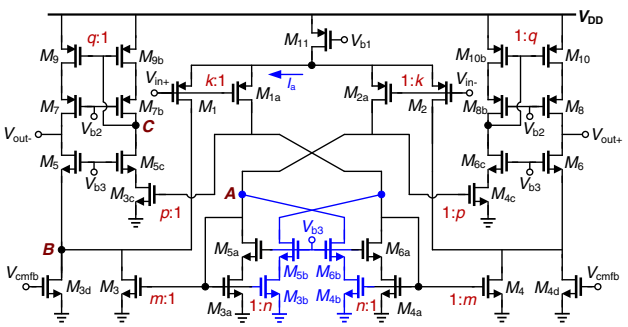

Fig. 2 Proposed single-stage multi-path operational amplifier

The transistors $M_{5a,6a}$, $M_{5b,6b}$, and $M_{5c,6c}$ are used to form the wide-swing cascode current mirrors for improved matching. To change the pMOS current source transistors, M_9 and M_{10}, in the conventional FCA, into driving transistors, another path is employed to drive their gate. This path is realized by wide-swing cascode current mirrors comprising of transistors M_{3c}–M_{6c} and M_{7b}–M_{10b}.

Transistors M_{3d} and M_{4d} are used to control the output common-mode voltage. A simple switched-capacitor common-mode feedback (CMFB) circuit (not shown here for simplicity) is used to control the gate voltage of transistors M_{3d} and M_{4d} in order to define the output common-mode voltage. It is worth mentioning that the output of the CMFB circuit cannot be applied to the gate of M_{11} unlike the conventional folded-cascode amplifier. This is because, in this case, we have different paths from the gate of transistor M_{11} into the output nodes with different signs most probably resulting in a positive feedback loop. To change the feedback loop to the negative one, an inverted gain stage is needed in the common-mode feedback circuit resulting in more power dissipation. So, the output of the CMFB circuit is simply is applied to the gate of M_{3d} and M_{4d} without needing such a power hungry gain stage. Finally, the biasing voltages V_{b1}–V_{b3} are provided by a simple constant current biasing network where the wide-swing cascode current mirrors are also utilized to provide large output signal swing.

As it is clear from Fig. 2, the proposed amplifier is realized by the combination of three different amplifiers: one folded-cascode amplifier and two different current-mirror amplifiers with pMOS input pairs. In the following, an extensive analysis of the proposed amplifier is provided.

2.2 DC analysis and slew rate

The DC current of all transistors excluding M_{3d} and M_{4d} is determined through the different current mirror ratios defined in Fig. 2 as k, m, n, p, and q between the corresponding transistors. By doing a simple DC analysis, the bias current of transistors M_{3d} and M_{4d} is obtained as:

$$I_{D3d,4d} = I_a \frac{k(n+1)+p\,q-m}{(k+1)(n+1)}, \tag{1}$$

where I_a as shown in Fig. 2 is the total DC current of input transistors in each path.

During large-signal operation, one of the input signals is much greater the other. In this case, the total bias current of the tail transistor, M_{11}, goes to the input transistors with the lower applied input signal to their gate. If for instance, V_{in+} to be much greater than V_{in-}, M_1 and M_{1a} enter the cut-off region and the total drain current of M_2 and M_{2a} is equal to that of M_{11}. In this case, the transistors M_4 and M_9 also enter the cut-off region since there is not any current going to the drain of transistor M_{4a-} in order to be mirrored through the corresponding current mirrors. This also cut-offs the transistors M_{3b} and M_{4b}. Therefore, the drain current of transistors M_3 and M_{10} is as follows:

$$I_{D3} = mI_{D2a}, \quad I_{D10} = p\,qI_{D2a} \tag{2}$$

On the other hand, the drain current of transistors M_{3d} and M_{4d} is always constant since their gate is driven by the CMFB circuit and it is assumed that the output of the CMFB circuit is constant during slewing. The DC current of transistors M_{3d} and M_{4d} is usually selected less than twice the DC current of M_1 and M_2. Therefore, during positive slewing, the drain voltage of M_2 is increased making M_6 to turn off. So, the drain current of the input transistor M_2 is constant during positive slewing and it is equal to that of M_{4d}. Hence, the drain current of M_{2a} is given by:

$$\begin{aligned} I_{D2a} &= 2I_a - I_{D4d} = 2I_a - I_a \frac{k(n+1)+p\,q-m}{(k+1)(n+1)} \\ &= I_a \frac{(k+2)(n+1)-p\,q+m}{(k+1)(n+1)} \end{aligned} \tag{3}$$

Therefore, the positive and negative slew rates are obtained as follows:

$$SR^+ = \frac{I_{D10}}{C_L} = \frac{p\,qI_{D2a}}{C_L}, \tag{4}$$

$$SR^- = \frac{I_{D3}+I_{D3d}}{C_L} = \frac{mI_{D2a}+I_{D3d}}{C_L}, \tag{5}$$

where C_L is the load capacitor from each output node to the ground. To achieve a symmetric slewing behavior, the positive and negative slew rates should be the same. So, we have:

$$p\,qI_{D2a} = mI_{D2a} + I_{D3d} \;=>\; I_{D4d} = (p\,q-m)I_{D2a} \tag{6}$$

Now, we have the relations (1) and (6) for the bias current of transistors M_{3d} and M_{4d}. Therefore, the following criterion is needed to be satisfied:

$$\begin{aligned} &I_a \left[\frac{k(n+1)+p\,q-m}{(k+1)(n+1)}\right] \\ &= (pq-m) \times I_a \left[\frac{(k+2)(n+1)-p\,q+m}{(k+1)(n+1)}\right] \end{aligned} \tag{7}$$

Here, we use an optimal value for k to satisfy the above condition, resulting in:

$$k_{opt} = \frac{(pq-m)\,(2n+1-p\,q+m)}{(n+1)(1-pq+m)} \tag{8}$$

Therefore, the differential slew rate is obtained as follows:

$$SR_{diff} = SR^{+} + SR^{-} = \frac{2pqI_a}{C_L} \times \frac{(k+2)(n+1) - (p\,q - m)}{(k+1)(n+1)}, \quad (9)$$

where the optimal value of k given by relation (8) is used in (9).

2.3 Small-signal transconductance and DC gain

The small-signal transconductance of the proposed amplifier defined as the ratio between the differential output short-circuit current and the input signal is readily obtained as follows:

$$\begin{aligned} G_m &= g_{m1} + g_{m1a}\frac{1}{g_{m3a} - g_{m3b}}(g_{m3} + q\,g_{m3c}) \\ &= g_{m1} + \frac{g_{m1}}{k\,g_{m3a}} \times \frac{(g_{m3} + q\,g_{m3c})}{1-n}, = g_{m1} + \frac{g_{m1}}{k} \times \frac{(m+pq)}{1-n} \\ &= g_{m1}\frac{k(1-n) + m + pq}{k(1-n)} \end{aligned} \quad (10)$$

where g_{mi} denotes the small-signal transconductance of the corresponding transistors. Hence, the amplifier's DC gain is given by:

$$\begin{aligned} A_{dc} &= G_m R_{out} \\ &\simeq g_{m1} \times \frac{k(1-n) + m + pq}{k(1-n)} \\ &\quad \times [g_{m7} r_{ds7} r_{ds9} || g_{m5} r_{ds5} (r_{ds1} || r_{ds3} || r_{ds3d})], \end{aligned} \quad (11)$$

where r_{ds} is the drain–source resistance of the transistors. Assuming a dominant pole to achieve a single-pole frequency response, the unity-gain bandwidth of the proposed amplifier is obtained as:

$$\omega_t \simeq \frac{G_m}{C_L} \simeq g_{m1}\frac{k(1-n) + m + pq}{k(1-n)C_L} \quad (12)$$

2.4 Small-signal frequency response

In this sub-section, the small-signal transfer function of the proposed multi-path amplifier is calculated to obtain the frequency poles and zeros. According to Fig. 2, the input signal passes from four nodes named as A, B, C, and output. By associating one pole to each of these nodes and considering different signal paths, the small-signal transfer function is given by:

$$\begin{aligned} A_v(s) &= \frac{A_1}{(1 + s/\omega_{out})(1 + s/\omega_B)} + \frac{A_2}{(1 + s/\omega_{out})(1 + s/\omega_A)} + \frac{A_3}{(1 + s/\omega_{out})(1 + s/\omega_A)(1 + s/\omega_C)} \\ &= \frac{s^2\left[\frac{A_1}{\omega_A\omega_C} + \frac{A_2}{\omega_B\omega_C}\right] + s\left[\frac{A_1}{\omega_A} + \frac{A_1}{\omega_C} + \frac{A_2}{\omega_B} + \frac{A_2}{\omega_C} + \frac{A_3}{\omega_B}\right] + (A_1 + A_2 + A_3)}{(1 + s/\omega_{out})(1 + s/\omega_A)(1 + s/\omega_B)(1 + s/\omega_C)}, \end{aligned} \quad (13)$$

where A_1, A_2, A_3, ω_{out}, ω_A, ω_B and ω_C are as follows:

$$\begin{aligned} A_1 &= g_{m1}R_{out} \\ A_2 &= g_{m1a}\frac{g_{m3}}{g_{m3a} - g_{m3b}}R_{out} = \frac{m}{k(1-n)}g_{m1}R_{out} \\ &= \frac{m}{k(1-n)}A_1 \equiv \alpha A_1 \\ A_3 &= g_{m1a}\frac{q g_{m3c}}{g_{m3a} - g_{m3b}}R_{out} = \frac{pq}{k(1-n)}g_{m1}R_{out} \\ &= \frac{pq}{k(1-n)}A_1 \equiv \beta A_1 \\ \omega_{out} &= \frac{1}{R_{out}C_L}, \quad \omega_A = \frac{g_{m3a} - g_{m3b}}{C_A} = \frac{(1-n)}{m}\frac{g_{m3}}{C_A} \\ \omega_B &= \frac{g_{m5}}{C_B}, \quad \omega_C = \frac{g_{m9b}}{C_C} = \frac{1}{q}\frac{g_{m9}}{C_C} \end{aligned} \quad (14)$$

According to relation (13), there are three non-dominant poles and two zeros. The zeros are due to the using three different signal paths. The frequency zeros are obtained as:

$$\begin{aligned} \omega_{z1,2} &= -\lambda \pm \sqrt{\lambda^2 - \frac{(1 + \alpha + \beta)\omega_A\omega_B\omega_C}{(\omega_B + \alpha\omega_A)}} \\ \lambda &= \frac{(1+\alpha)\omega_A\omega_B + (\alpha + \beta)\omega_A\omega_C + \omega_B\omega_C}{2(\omega_B + \alpha\omega_A)} \end{aligned} \quad (15)$$

The pole associated with node A, ω_A, is usually smaller than the other non-dominant poles. So, to achieve a sufficient phase margin, and hence, a well behavior transient response, the value of n should be selected properly. This is equivalent to an optimal sizing of the cross-coupled transistors, M_{3b}, M_{4b}. By increasing n, both the DC gain and unity-gain bandwidth are enhanced. But, the equivalent second pole, which is mainly determined by ω_A, is decreased. Therefore, there is a trade-off between the enhanced DC gain and unity-gain bandwidth and the amplifier's stability and this can be compromised by carefully choosing the aspect ratio of the cross-coupled transistors (M_{3b}, M_{4b}) respected to the diode-connected transistors (M_{3a}, M_{4a}), i.e. the value of n. In practice, the equivalent second pole should be at least two times larger than the unity-gain bandwidth to achieve a phase margin beyond 60 degree [1].

3 Comparison with conventional folded-cascode amplifier

In this section, the proposed amplifier is compared with the conventional FCA. To provide a fair comparison, firstly, the same total bias current is used in both amplifiers. The total bias current of the proposed amplifier is given by:

$$I_{total} = 2(I_{D1} + I_{D1a} + I_{D9} + I_{D9b}) = 2I_a \times \frac{(k+1)(n+1) + p(1+q)}{(k+1)(n+1)} \quad (16)$$

In the conventional FCA, as mentioned before, to achieve a symmetric slewing behavior, the same bias current is used in the input and cascode transistors [1]. So, in FCA by denoting the bias current of input transistors as I_b, and then equating the total current of the proposed amplifier with that of the FCA, the following relation is achieved:

$$I_a = I_b \times \frac{2(k+1)(n+1)}{(k+1)(n+1) + p(1+q)} \quad (17)$$

Secondly, the same aspect ratio in the input transistors of the proposed amplifier and the conventional FCA is considered to have the equal input parasitic capacitors, and hence, the same feedback factor in the closed-loop configuration. Therefore, with the equal power consumption, their small-signal transconductance is related by:

$$G_m = G_{m,fc} \times \frac{k(1-n) + m + pq}{(1-n)(k+1)} \sqrt{\frac{2(k+1)(n+1)}{(k+1)(n+1) + p(1+q)}}, \quad (18)$$

where $G_{m,fc}$ is the total transconductance in the FCA which is equal to the g_m of input transistors. Hence, the DC gain and unity-gain bandwidth of the proposed amplifier compared to the FCA are increased as:

$$A_{dc} = A_{dc,fc} \times \frac{k(1-n) + m + pq}{(1-n)(k+1)} \sqrt{\frac{2(k+1)(n+1)}{(k+1)(n+1) + p(1+q)}}, \quad (19)$$

$$\omega_t = \omega_{t,fc} \times \frac{k(1-n) + m + pq}{(1-n)(k+1)} \sqrt{\frac{2(k+1)(n+1)}{(k+1)(n+1) + p(1+q)}}, \quad (20)$$

where $A_{dc,fc}$ and $\omega_{t,fc}$ represent the DC gain and unity-gain bandwidth of the FCA, respectively. Nonetheless, the phase margin of the proposed amplifier is degraded compared to the FCA since it has more non-dominant poles due to the active current mirrors. However, this can be alleviated by using small current mirror ratios to move the non-dominants poles to higher frequencies.

To provide a clear view, an example is considered here. By assuming, $m = 2$, $n = 0.5$, $p = 1$, and $q = 2.5$, the optimal value of k is calculated from relation (8) as 1. According to relations (19) and (20), both the DC gain and unity-gain bandwidth of the proposed amplifier are enhanced about 4.8 times compared to the FCA which is a significant improvement without consuming any extra power.

The slew rate of the proposed amplifier is also compared with that of FCA. To do so, the same total bias current is assumed in both amplifiers. For the FCA, the differential slew rate is given by:

$$SR_{diff,fc} = \frac{2I_b}{C_L} \quad (21)$$

So, according to the relations (9), (17), and (21), the slew rate of the proposed amplifier compared to the FCA is enhanced according to the following relation:

$$SR_{diff} = SR_{diff,fc} \times \frac{2pq[(k+2)(n+1) - (p\,q - m)]}{(k+1)(n+1) + p(1+q)} \quad (22)$$

For the above example, the slew rate enhancement is about 3.1 times.

4 Simplified structures of the proposed amplifier

In this section, two simplified structures of the proposed amplifier is examined and compared with the conventional FCA and the proposed OTA. Firstly, the cross-coupled transistors, M_{3b}–M_{6b} are removed from the amplifier circuit in Fig. 2. This is equivalent to the case of $n = 0$ and results in the recycling folded-cascode OTA with three signal paths (the OTA presented in [12] without the FVF cell). Secondly, only one of the input differential pairs (M_{1a} and M_{2a}) is considered and the other one (M_1 and M_2) is removed from the amplifier's circuit. This is achieved by setting k to zero. In this case, a two-path current-mirror amplifier is resulted.

4.1 Proposed amplifier without cross-coupled transistors

When the cross-coupled transistors M_{3b}–M_{6b} are removed from Fig. 2, by doing the same analysis as before, the optimal value of k to achieve a symmetric slewing behavior is given by:

$$k_{opt} = \frac{(pq - m)\,(1 - p\,q + m)}{(1 - pq + m)} \quad (23)$$

So, the differential slew rate is obtained as:

$$SR_{diff} = \frac{2pqI_a}{C_L} \times \frac{(k+2)-(p\,q-m)}{(k+1)} \tag{24}$$

The resulting amplifier is also compared with the conventional FCA with the same total current consumption and aspect ratio in input transistors. Their small-signal parameters are related by:

$$A_{dc} = A_{dc,fc} \times \frac{k+m+pq}{(k+1)} \sqrt{\frac{2(k+1)}{(k+1)+p(1+q)}} \tag{25}$$

$$\omega_t = \omega_{t,fc} \times \frac{k+m+pq}{(k+1)} \sqrt{\frac{2(k+1)}{(k+1)+p(1+q)}} \tag{26}$$

The differential slew rate of this amplifier is related to the FCA as follows when the same power is consumed in both amplifiers:

$$SR_{diff} = SR_{diff,fc} \times \frac{2pq[(k+2)-(p\,q-m)]}{(k+1)+p(1+q)} \tag{27}$$

The above-mentioned example is also considered here. By assuming $m = 2$, $p = 1$, and $q = 2.5$, the optimal value of k is calculated from relation (23) as 0.5. According to the relations (25) and (26), both the DC gain and unity-gain bandwidth of this amplifier is enhanced about 2.6 times compared to the conventional FCA. In this example, the slew rate of this amplifier is almost 2 times larger than that of the FCA with the same power consumption.

As it is clear, a great improvement compared to the FCA is still achieved, but, this is lower than the case when the cross-coupled transistors are utilized. So, the cross-coupled transistors, M_{3b}–M_{6b}, realizing a positive feedback network, improve both the small-signal and large-signal parameters of the proposed amplifier. As it is well-known, the small-signal parameters are enhanced since transistors M_{3b}–M_{6b} realize a negative resistance at drains of M_{3a} and M_{3b} making these nodes relatively high impedance. But, their impact on the slew rate is also considerable and it is more than 50 %.

4.2 Two-path current-mirror amplifier

In this case, one of the input differential pairs comprising of M_1 and M_2 is removed. Hence, the drain DC current of transistors M_{3d} and M_{4d} is given by:

$$I_{D3d,4d} = I_a \frac{p\,q-m}{(n+1)} \tag{28}$$

The positive and negative slew rates can be easily obtained as follows:

$$SR^+ = \frac{I_{D10}-I_{D4d}}{C_L} = \frac{2p\,qI_a - I_{D4d}}{C_L} \tag{29}$$

$$SR^- = \frac{I_{D3}+I_{D3d}}{C_L} = \frac{2mI_a + I_{D3d}}{C_L} \tag{30}$$

According to the relations (28)–(30), the symmetric slewing behavior is achieved when $n = 0$. This means, in this case, the cross-coupled transistors M_{3b}–M_{6b} cannot be used. Therefore, in this case, the cross-coupled transistors M_{3b}–M_{6b} are also removed from Fig. 2, and hence, the differential slew rate is given by:

$$SR_{diff} = \frac{2I_a(p\,q+m)}{C_L} \tag{31}$$

The resulting two-path current-mirror amplifier is also compared with the conventional FCA with the same aspect ratio in input transistors and the same power dissipation. Therefore, we have:

$$A_{dc} = A_{dc,fc} \times (m+pq)\sqrt{\frac{2}{[1+p(1+q)]}} \tag{32}$$

$$\omega_t = \omega_{t,fc} \times (m+pq)\sqrt{\frac{2}{[1+p(1+q)]}} \tag{33}$$

Finally, their slew rate is related through:

$$SR_{diff} = SR_{diff,fc} \times \frac{2(p\,q+m)}{1+p(1+q)} \tag{34}$$

The same example is also considered here. For $m = 2$, $p = 1$, and $q = 2.5$, both the DC gain and unity-gain bandwidth of this amplifier are about 3 times higher than that of the FCA. The slew rate is also improved about two times compared to the FCA with the same power.

From both the simplified structures of the proposed amplifier, it is clear that the cross-coupled transistors improve both the large-signal and small-signal performances of the proposed OTA substantially.

5 Simulation results

To evaluate the usefulness of the proposed amplifier, HSPICE simulation results are provided using a 90 nm BSIM4v4 level 54 mixed-signal CMOS technology with a 1.2 V power supply. The above-mentioned examples for the current mirror ratios were considered in the simulations. The amplifiers were designed for a switched-capacitor integrator with the sampling and integrating capacitors of 5 and 10 pF, respectively. The load capacitor was 5 and 1.7 pF in AC open-loop and transient closed-loop simulations, respectively, which corresponds to an effective load capacitance, C_L, of 5 pF in both simulations. The conventional FCA shown in Fig. 1 was also simulated with the same power consumption and equal overdrive voltage in all signal path transistors except the input transistors (where the same aspect ratios were employed) in order to provide a fair comparison. The channel length of transistors has been

Table 1 Device sizes of the simulated amplifiers

Parameter	Conventional folded-cascode OTA (μm)	Proposed OTA without cross-coupled transistors (μm)	Two-path current-mirror OTA (μm)	Proposed multi-path OTA (μm)
$(W/L)_{1,2}$	8 × 8/0.18	3 × 7/0.18	–	4 × 8/0.18
$(W/L)_{1a,2a}$	–	6 × 7/0.18	8 × 8/0.18	4 × 8/0.18
$(W/L)_{3,4}$	5 × 5/0.18	4 × 2.5/0.18	4 × 2.8/0.18	4 × 2/0.18
$(W/L)_{3a,4a}$	–	2 × 2.5/0.18	2 × 2.8/0.18	2 × 2/0.18
$(W/L)_{3b,4b}$	–	–	–	1 × 2/0.18
$(W/L)_{3c,4c}$	–	2 × 2.5/0.18	2 × 2.8/0.18	2 × 2/0.18
$(W/L)_{3d,4d}$	–	4 × 2.5/0.18	1 × 2.8/0.18	4 × 2/0.18
$(W/L)_{5,6}$	5 × 3/0.18	5 × 2.4/0.18	5 × 3.3/0.18	5 × 2.3/0.18
$(W/L)_{5a,6a}$	–	2 × 2.4/0.18	2 × 3.3/0.18	2 × 2.3/0.18
$(W/L)_{5b,6b}$	–	–	–	1 × 2.3/0.18
$(W/L)_{5c,6c}$	–	2 × 2.4/0.18	2 × 3.3/0.18	2 × 2.3/0.18
$(W/L)_{7,8}$	5 × 6/0.18	5 × 4.8/0.18	5 × 6.7/0.18	5 × 4.4/0.18
$(W/L)_{7b,8b}$	–	2 × 4.8/0.18	2 × 6.7/0.18	2 × 4.4/0.18
$(W/L)_{9,10}$	5 × 6/0.18	5 × 4.9/0.18	5 × 6.8/0.18	5 × 4.5/0.18
$(W/L)_{9b,10b}$	–	2 × 4.9/0.18	2 × 6.8/0.18	2 × 4.5/0.18
$(W/L)_{11}$	10 × 5/0.18	6 × 5/0.18	5 × 4.4/0.18	8 × 5.8/0.18

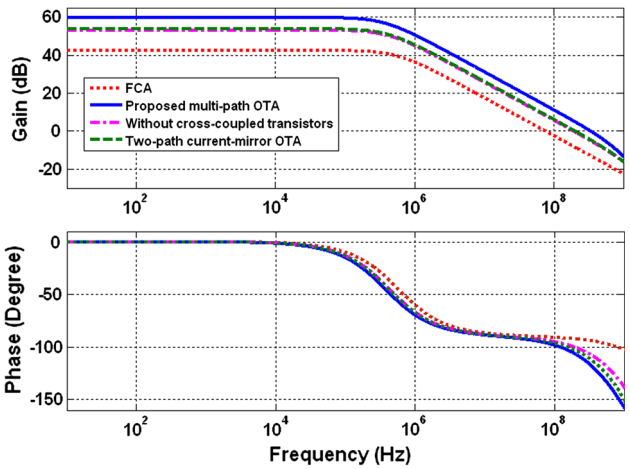

Fig. 3 Open-loop frequency response of the simulated amplifiers

selected twice the technology minimum channel length to achieve a relatively high DC gain. All of the amplifiers use the same bias circuitry with appropriate currents and a simple switched-capacitor CMFB circuit. The input and output common-mode voltages of the amplifiers were 0.4 and 0.6 V, respectively. The simulated device sizes are summarized in Table 1.

The open-loop frequency and closed-loop transient responses of the simulated amplifiers are illustrated in Figs. 3 and 4, respectively. In large-signal transient simulations, an input step of 1 V differential height was employed. Table 2 summarizes the simulation results. To provide a clear view, the improvements resulted from the analytical calculations and the simulations are shown in Table 3. As it is seen, both the small-signal and large-signal performances of the proposed amplifier and its simplified structures are improved almost according to the analytical calculations. The DC gain improvement is more than the theoretically predicted value since the output resistance in the proposed amplifier and its simplified structures is also increased owing to using lower bias current in output transistors.

The phase margin of the proposed multi-path amplifier is degraded compared to the FCA since it has more non-dominant poles due to the active current mirrors. But, the achieved phase margin is still high enough to have a well behavior transient response with a much lower settling time. Indeed, the phase margin of the conventional FCA is very high resulting in a slow step response. The enhanced slew rate and unity-gain bandwidth of the proposed amplifier makes it to settle more rapidly than the conventional FCA in switched-capacitor circuits. As it is seen from Table 2, the proposed OTA outperforms its simplified structures and the conventional FCA in terms of both small-signal and large-signal figure of merits (FoMs).

The input-referred noise voltage of the proposed multi-path amplifier is approximately the same as the conventional FCA. The active area of the proposed amplifier is larger than the conventional FCA. But, this is not a critical issue since the active area in mixed-signal circuits is mostly determined by passive components such as capacitors.

The simulation results of the proposed amplifier in different process corner cases and temperature variations are

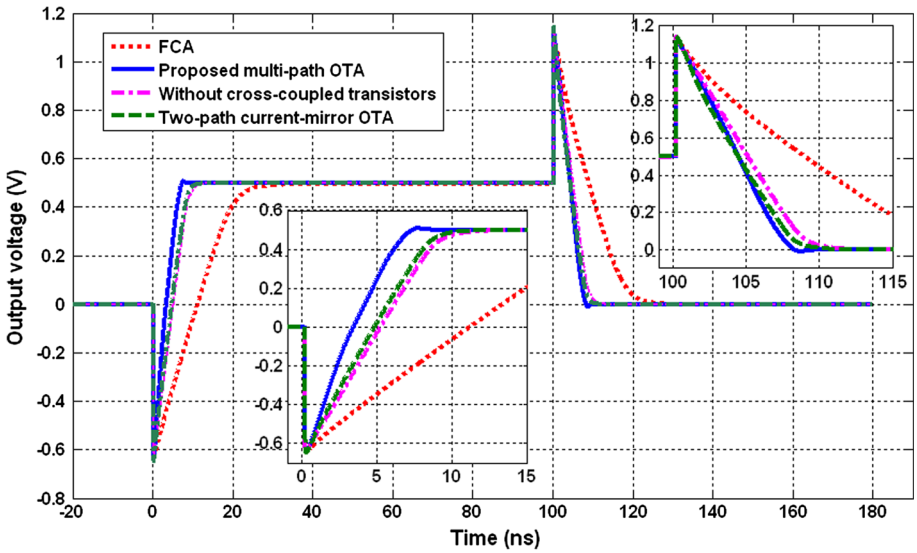

Fig. 4 Large-signal transient response of the simulated amplifiers

Table 2 Simulation results summary

Parameter	Conventional folded-cascode OTA	Proposed OTA without cross-coupled transistors	Two-path current-mirror OTA	Proposed multi-path OTA
DC gain (dB)	42.4	53.1	53.8	59.8
Unity-gain bandwidth (MHz)	78.1	197.8	208.2	348.1
Phase margin (°)	89.5	80.1	76.7	62.2
Average slew rate (V/μs)	54.1	127.5	135	173
0.01 % settling times (t_{s+}/t_{s-}) (ns)	42.9/53.3	17/24.7	15.6/21.9	9.5/10.7
Input-referred noise density @ 100 kHz	40.6 nV/$\sqrt{\text{Hz}}$	42.5 nV/$\sqrt{\text{Hz}}$	38.9 nV/$\sqrt{\text{Hz}}$	34.9 nV/$\sqrt{\text{Hz}}$
	−147.8 $\text{dBV}_{\text{rms}}/\sqrt{\text{Hz}}$	−147.4 $\text{dBV}_{\text{rms}}/\sqrt{\text{Hz}}$	−148.2 $\text{dBV}_{\text{rms}}/\sqrt{\text{Hz}}$	−149.1 $\text{dBV}_{\text{rms}}/\sqrt{\text{Hz}}$
Static power dissipation (including bias circuitry) (μW)	856	853.8	852.5	851.9
FoM_1 (MHz × pF/mA)	547.4	1,390.0	1465.3	2457.3
FoM_2 ((V/μs) × pF/mA)	379.2	896.0	950.1	1218.5
Capacitive load (C_L)	5 pF			
Power supply voltage	1.2 V			
Technology	90 nm 1P9M CMOS			

FoM_1 = (unity-gain bandwith × load capacitance)/total current

FoM_2 = (average slew rate × load capacitance)/total current

Table 3 Calculated and simulated amplifiers prameters respected to the FCA

Parameter	Proposed multi-path OTA		Proposed OTA without cross-coupled transistors		Two-path current-mirror OTA	
	Calculation	Simulation	Calculation	Simulation	Calculation	Simulation
I_a	0.92 × I_b	0.98 × I_b	0.6 × I_b	0.65 × I_b	0.44 × I_b	0.47 × I_b
A_{dc}	4.8 × $A_{dc,fc}$	7.4 × $A_{dc,fc}$	2.6 × $A_{dc,fc}$	3.4 × $A_{dc,fc}$	3 × $A_{dc,fc}$	3.7 × $A_{dc,fc}$
ω_t	4.8 × $\omega_{t,fc}$	4.5 × $\omega_{t,fc}$	2.6 × $\omega_{t,fc}$	2.53 × $\omega_{t,fc}$	3 × $\omega_{t,fc}$	2.67 × $\omega_{t,fc}$
SR_{diff}	3.1 × $SR_{diff,fc}$	3.2 × $SR_{diff,fc}$	2 × $SR_{diff,fc}$	2.36 × $SR_{diff,fc}$	2 × $SR_{diff,fc}$	2.5 × $SR_{diff,fc}$

Table 4 Simulation results of the proposed multi-path amplifier in different process corner cases and temperature variations

Parameter	TT@ 27 °C	FF@ −40 °C	SS@ 85 °C
DC gain (dB)	59.8	59.7	59.3
Unity-gain bandwidth (MHz)	348.1	412.1	305.5
Phase margin (°)	62.2	63.2	61.7
Average slew rate (V/μs)	173	183	143.5
0.01 % settling times (t_{s+}/t_{s-}) (ns)	9.5/10.7	8.4/9.9	10.5/11.6
Input-referred noise density @ 100 kHz	34.9 nV/$\sqrt{\text{Hz}}$	35.2 nV/$\sqrt{\text{Hz}}$	35.1 nV/$\sqrt{\text{Hz}}$
	−149.14 $\text{dBV}_{\text{rms}}/\sqrt{\text{Hz}}$	−149.07 $\text{dBV}_{\text{rms}}/\sqrt{\text{Hz}}$	−149.09 $\text{dBV}_{\text{rms}}/\sqrt{\text{Hz}}$
Static power dissipation (including bias circuitry)	851.9 μW	897.3 μW	832.1 μW
FoM_1 (MHz × pF/mA)	2457.3	2755.6	2202.9
FoM_2 [(V/μs) × pF/mA]	1218.5	1223.7	1034.7

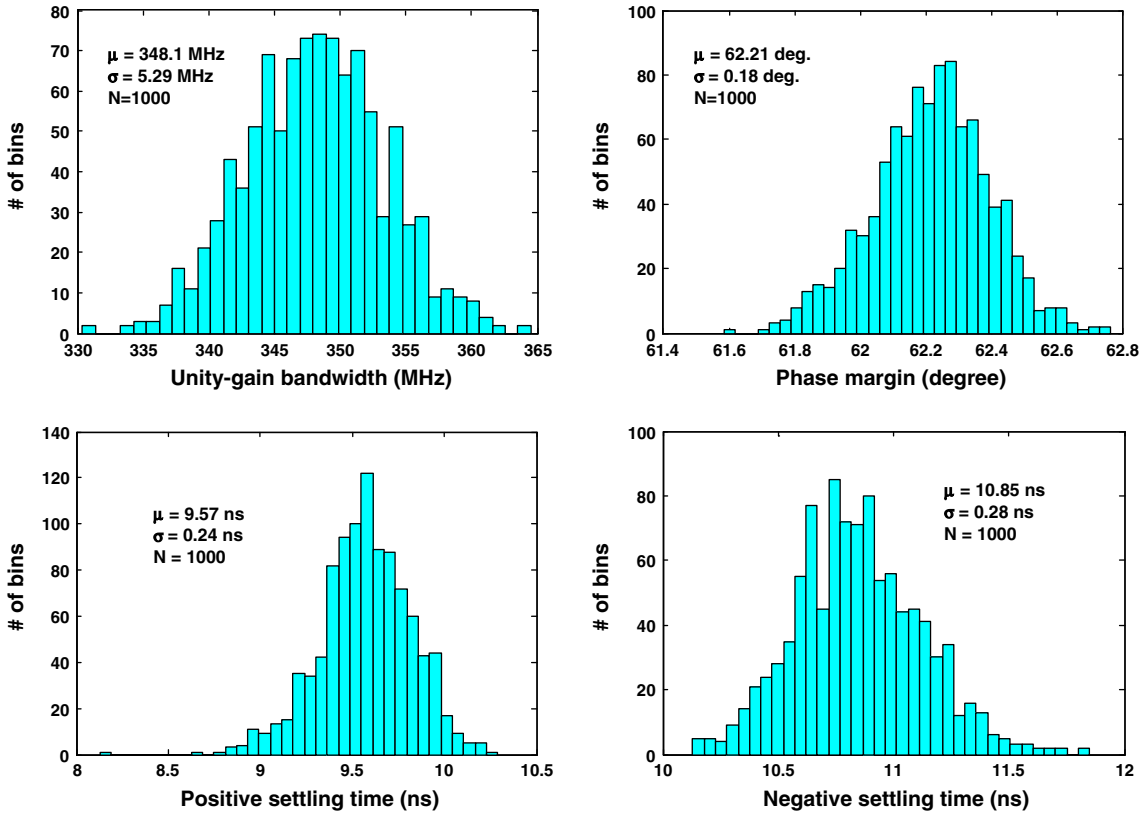

Fig. 5 Monte Carlo simulation results of the proposed multi-path amplifier

summarized in Table 4. The robustness of the proposed amplifier against process and mismatch variations were evaluated through extensive circuit level Monte Carlo simulations. The results are shown in Fig. 5 where the unity-gain bandwidth, phase margin, and both positive and negative settling times are illustrated for 1,000 iterations in which both process and local variations of device parameters were taken into account. As it is seen, the proposed amplifier is more tolerant to the process variations and shows negligible performance degradation.

6 Conclusions

A single-stage multi-path operational amplifier for high-resolution fast-settling switched-capacitor circuits was proposed. It uses all idle devices in the conventional FCA in the signal path and the positive feedback network to improve both the amplifier's large-signal and small-signal parameters significantly. The proposed amplifier achieves enhanced DC gain, unity-gain bandwidth, and slew rate making it to settle more rapidly than the conventional FCA

in SC circuits with the same power consumption. It can be used in high-resolution and high-speed A/D converters.

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