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A 55–64-GHz Low-Power Small-Area LNA in 65-nm CMOS With 3.8-dB Average NF and ∼12.8-dB Power Gain

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***Abstract*—This letter presents a low-power small-footprint low-noise amplifier (LNA) that operates over the frequency band of 55–64 GHz. Using a resistor between bulk and substrate (ground) nodes, these two nodes are isolated. This bulk isolation technique is introduced to achieve the maximum gain of the transistor at the desired frequency band. Also, a methodology is proposed to determine the optimal size of transistors to achieve the maximum possible gain. As a proof of concept, the proposed LNA is fabricated in a 65-nm bulk CMOS process, and the design features 12.8 ± 0.5 dB power gain and an average noise figure of 3.8 dB. The output 1-dB compression point of the LNA is −6 dBm. The LNA consumes 8.8 mW from a 1-V supply and excluding the pads occupies a silicon area of 0.23 mm^2.**

***Index Terms*—Beamforming, CMOS, low-noise amplifier (LNA), low power, millimeter wave (mm wave), phased-array receivers.**

I. Introduction

THE interest for high-speed data rate in wireless communication is continuously growing. Beamforming or phased-array method, which is considered in IEEE 802.11ad and IEEE 802.15.3c standards, improves the power efficiency and signal-to-noise ratio in such transceivers. Two main drawbacks of the phased-array technique are relatively high power consumption and large chip area due to the large number of transceivers in the array. Therefore, low-power building blocks with a compact size are required for the operation of these transceivers at millimeter-wave (mm-wave) frequencies.

Low-noise amplifiers (LNAs) are one of the critical building blocks of the receiver. They provide a relatively high gain with a low noise figure (NF) to reduce the noise contribution of the subsequent blocks. Typically, LNAs cannot be shared in phased-array receivers, and each signal path incorporates its own LNA. Therefore, the number of LNAs is proportional to the number of elements used in the array, and thus, the LNAs should be power efficient and compact. Generally, mm-wave LNAs employ common source (CS), cascode, or current reuse topologies at mm-wave frequencies [1]–[9]. CS topology benefits from the lowest NF amongst that of other structures, while it suffers from a relatively low gain and poor isolation [1]. Two- and three-stage LNAs have been reported in [2]–[5] where a CS topology has been employed in the first stage. Also, the transformer feedbacked neutralizer technique has been introduced to boost the LNA gain in [2] and [3]. However, this technique results in a relatively narrow bandwidth LNA. The cascode topology offers higher isolation and gain at the cost of a higher NF [6]–[9]. In [1], dc current reuse has been employed to save power in a three-stage LNA. This topology is the same as its CS counterpart, while it introduces more complexity, especially at mm-wave frequencies.

The number of stages used in an LNA directly affects the power consumption and the occupied area directly. Therefore, an LNA with the minimum number of stages is attractive to mitigate the large area and power consumption, especially in phased-array systems.

In this letter, we propose a technique based on bulk isolation for designing low-power small-footprint LNAs. The rest of this paper is organized as follows. Section II describes the proposed LNA implementation. Simulation and measurement results are presented in Section III and concluding remarks are provided in Section IV.

II. Proposed LNA

Fig. 1 (excluding $R_{\rm Bulk}$) shows the typical layout and the small-signal model of RF nMOS transistors in the CMOS design kit with separate bulk and substrate nodes. To increase the gain of transistor at high frequencies, the impact of $C_{\rm sb}$ and $C_{\rm db}$ (source-bulk and drain-bulk capacitors) should be neutralized. This can be achieved by adding a large resistor [$R_{\rm Bulk}$ in Fig. 1(b)] between the bulk and ground nodes to isolate the bulk node. To achieve such isolation, $R_{\rm Bulk}||Z_T$ should have a relatively large magnitude over the bandwidth of interest so it can be approximated as an open circuit. Here [as shown in Fig. 1(b)], Z_T is the total impedance between bulk and ground. $R_{\rm n-well}$ and $R_{\rm sub}$ are the equivalent resistance of n-well and substrate, respectively, and $C_{\rm n-well}$ and $C_{\rm sub}$ are the equivalent capacitance of n-well and substrate diodes, respectively. It is worth mentioning that in [10], a 1-kΩ resistor has been added between n-well and supply nodes to mitigate the effect of $C_{\rm sub}$ and $C_{\rm n-well}$. Also, in [11], a large resistor is inserted in series with the gate of the transistor and a large resistor is placed between bulk and ground nodes to increase the isolation of transistor when it is used as a passive switch.

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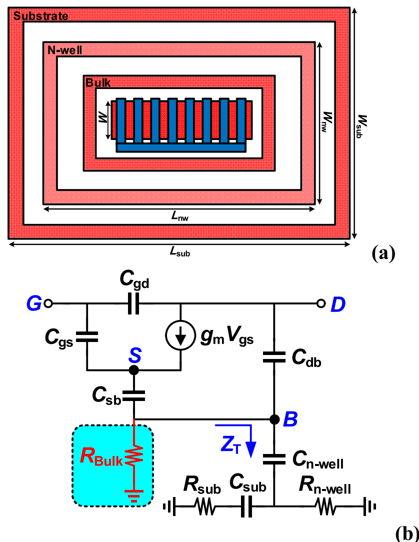

Fig. 1. nMOS RF transistor. (a) Layout view. (b) Small-signal model.

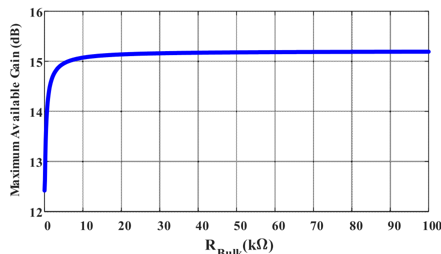

Fig. 2. Maximum available gain of a cascode structure at 60 GHz versus R_{Bulk}. ($W = 2\ \mu$m, $L = 60$ nm, $N = 8$, and $m = 2$).

Since the cascode topology offers a higher gain and a better input–output isolation compared to a single-transistor amplifier, for the proposed design, we use cascode topology.

To show the effect of R_{Bulk} in increasing the gain, one can derive the following equation for the relative maximum available gain (A_{VR}) of the cascode amplifier with and without R_{Bulk} added to both transistors:

$$\lim_{\substack{R_B\to\infty \\ s\to\infty}} A_{VR} = \frac{A_V|_{R_{\text{Bulk}}\neq 0}}{A_V|_{R_{\text{Bulk}}=0}} \approx \frac{C_{xo}}{C_{xo} - 1.5C_{\text{db}}} \times \frac{g_o + G_{\text{out}}}{g_o + g_{m2}}. \tag{1}$$

Here, G_{out}, g_{m2}, and g_o are the real part of the output admittance, transconductance of the cascode transistor, and drain–source transconductance of both transistors, respectively. Also, $C_{xo} = C_{\text{gs}} + 2C_{\text{gd}} + C_{\text{db}} + C_{\text{sb}}$. In deriving (1), some simplifying assumptions including $|Z_T|$ being relatively large, conjugate matching at the output, identical transistors for cascade amplifier, and using Miller equivalent of gate–drain capacitor of the input transistor are made. It can be shown that the value of A_{VR} is larger than one which means that large R_{Bulk} increases the gain at high frequencies. Using the circuit parameters of Fig. 2, A_{VR} is 1.875 (2.73 dB) at high frequencies.

Fig. 2 shows the simulated maximum available gain of a cascode structure with two identical nMOS transistors at 60 GHz as a function of R_{Bulk}. In Fig. 2, simulations are performed using the Keysight Advanced Design System (ADS). According to Fig. 2, a 2.7-dB improvement in the maximum available gain can be achieved when $R_{\text{Bulk}} \geq 10$ kΩ which is in a good agreement with (1). Beyond 10 kΩ, the increase in the gain is minimal and tends to saturate. Thus, we use $R_{\text{Bulk}} = 10$ kΩ.

At low frequencies, the intrinsic gain of a multifinger MOS transistor increases when the width of the unit transistor and the number of fingers become larger. However, an arbitrary increase in the size and number of fingers is not a feasible approach at mm-wave frequencies due to the increased loss when the signal travels through the gate as well as an increase in the device capacitances. Therefore, at mm-wave frequencies, for a given gate bias, there is an optimum width per finger while the total width of the multifinger transistor is kept constant. For this, the contours of the maximum available gain versus the gate bias and transistor size should be extracted from the simulation results using the process design kit.

In this letter, a two-stage LNA is designed using the transistors with bulk isolation, and the corresponding schematic is shown in Fig. 3. In this proof-of-concept design, we use a single-ended topology as opposed to a differential version. The single-ended design also requires a lower power consumption. Considering the loss of matching networks, at least, two stages are needed to achieve a reasonable power gain. Based on contours of the maximum available gain, for each transistor in the cascode structure, two parallel multifinger transistors with the unit transistor size of $W = 2\ \mu$m, $L = 60$ nm, and number of fingers $(N) = 8$ are used.

The input matching network is optimized to transform the 50-Ω impedance at the input ground-signal-ground (GSG) pads to the optimum noise source impedance at the first gain stage. Due to the loss of passive devices, the minimum number of passive components has been utilized in the input matching network to reduce the adverse effects on the NF. The interstage matching network transforms the input impedance of the second gain stage to the optimum load impedance of the first stage. Similarly, the output matching network transforms the 50-Ω impedance at the output of GSG pads to the optimum load impedance of the second stage. The matching networks are designed using high-order filters (i.e., fourth order and fifth order) with a low quality factor which help to achieve a nearly flat gain within the bandwidth of interest. Furthermore, L_2 and L_6 are used to gain peaking at high frequencies by neutralizing the effect of C_{gs} and C_{gd} of the cascode transistors. Also, C_2 and C_5 capacitors are employed for dc blocking. All the matching networks are implemented using the top (thickest) metal layer to mitigate the loss. Moreover, the coplanar structure has been used for transmission lines with a ∼5-μm spacing to the ground plane. The required capacitors are realized as interdigitated metal–oxide–metal capacitors using sixth to eighth metal layers. Due to the single-ended implementation, the circuit is highly sensitive to the ground node. Therefore, special attention should be paid to carefully model the ground. The ground pad of GSG pad is considered as the only ground node on the chip, and it is considered as a reference in all electromagnetic (EM) simulations.

III. Simulation and Measurement Results

Fig. 4(a) shows the micrograph of the proposed LNA that is fabricated in a 65-nm CMOS process. The chip area excluding the pads is 0.23 mm^2. DC pads are wire bonded on a CFP24 package, and RF signals are probed. The S-parameters and NF are measured up to 67 GHz by Keysight PNA N5247A. The measurement and ADS Momentum EM simulation results are shown in Fig. 4(b) and (c). Power gain is around 12.8 dB (with ±0.5 dB variations across the frequency range of

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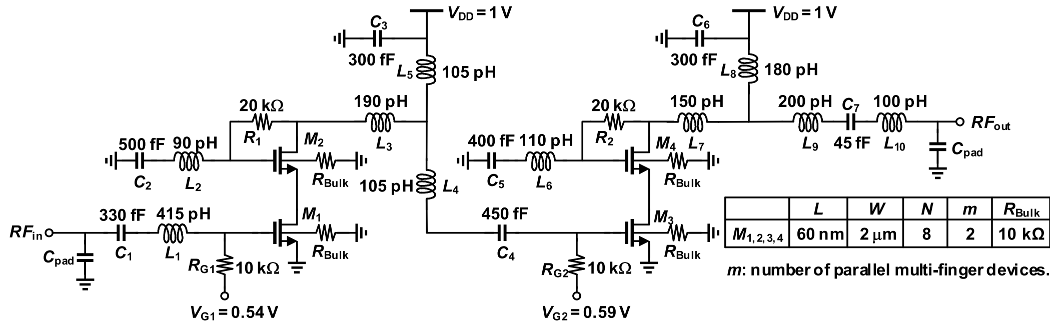

Fig. 3. Schematic of LNA.

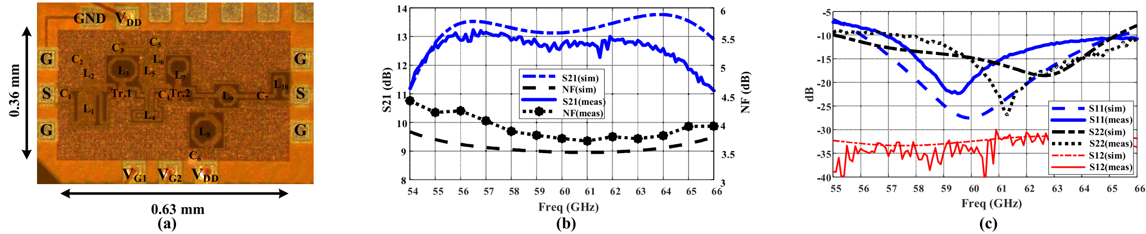

Fig. 4. (a) Die micrograph (the five pads on the top right of the design which are not labeled belong to the adjacent design), and measurement and simulation results of LNA: (b) power gain and NF and (c) input and output reflection coefficients and isolation.

TABLE I

PERFORMANCE SUMMARY AND COMPARISON WITH PREVIOUSLY PUBLISHED SINGLE-ENDED WORKS

Reference	**This Work**	ELL'17 [1]	ELL'15 [2]	ELL'13 [4]	EuMW'13 [6]	MTT'15 [7]
Topology	**2 Cas**	3 Cas	3 CS	CS+Cas+CS	2 Cas+CS	2 Cas
BW [GHz]	**55-64**	48-65	57-66	51-63	57-60	58-72
P. Gain[dB]	**12.8±0.5**	13.4±1.5	25±5	9.9±1.5	21±1	13±0.8
NF_{min} [dB]	**3.6@ 61GHz**	5.7@ 62GHz	4.6@ 62GHz	3.9@ 55GHz	3.7@ 61GHz	4@ 60GHz
OP_{1dB}[dBm]	**–6**	-8	N/A	N/A	-2	1
P_{DC} [mW]	**8.8**	9.6	8.9	14.1	13.5	24
Supply [V]	**1**	1	1	1.2	1.5	2
Area*[mm^2]	**0.33**	0.58	0.49	0.44	0.59	0.38
FoM	**201**	103	-	-	104	485
Tech. (nm)	**65**	65	65	90	90	28

CS = Common Source, Cas = Cascode, *including pads

interest), and average NF across the bandwidth is ∼3.8 dB. The fabricated LNA is unconditionally stable and no signs of instability were observed on the output spectrum. The measured power consumption and output $P_{-1\mathrm{dB}}$ at 60 GHz are 8.8 mW and –6 dBm, respectively. Table I summarizes the performance of the proposed LNA and compares it with that of the state-of-the-art designs. For the purpose of comparison, the following figure of merit (FoM) is used [7]:

$$\mathrm{FoM} = \frac{G \times IP_{-1\mathrm{dB}}/(\mathrm{mW}) \times \mathrm{BW}/(\mathrm{MHz})}{(F-1) \times P_{\mathrm{dc}}/(\mathrm{mW})} \tag{2}$$

where G, $IP_{-1\mathrm{dB}}$, BW, and F are the power gain, input 1-dB compression point, bandwidth, and noise factor, respectively.

IV. CONCLUSION

A two-stage low-power compact LNA operating from 55 to 64 GHz is implemented in a 65-nm CMOS process. Using the bulk isolation technique, the power gain is improved by increasing the intrinsic gain of the transistors. In another perspective, the proposed technique allows for reducing the required number of gain stages for a given gain thereby, reducing the power consumption. The implemented 0.23-mm^{2}LNA achieves a power gain of 12.8 ± 0.5 dB and an average NF of 3.8 dB over 55–64 GHz. The LNA consumes 8.8 mW and the measured output $P_{-1\mathrm{dB}}$ is -6 dBm. The proposed LNA compares favorably with the state-of-the-art designs, in particular, in terms of silicon area and NF.

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