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High-performance time-based continuous-time sigma-delta modulators using single-opamp resonator and noise-shaped quantizer

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ABSTRACT

In this paper, a new methodology to improve the performance of continuous-time sigma-delta modulators is presented. The proposed structure notated as the time-based continuous-time sigma-delta modulator (TCSDM) utilizes the time encoding approach. Time-based encoding is known as a promising alternative to overcome the resolution problems of analog-to-digital converters (ADCs) in low-voltage circuits. The proposed TCSDM incorporates a novel time-based noise-shaped quantizer (NSQ) to significantly enhance its performance at a very low cost. Using the proposed NSQ, the modulator's noise-shaping order is improved by two without increasing the loop filter order. Furthermore, the implementation of the proposed TCSDM is alleviated using a new single-opamp resonator (SOR) to realize the loop filter. This significantly reduces the power consumption and saves more area. The concept is elaborated for a second-order TCSDM. The analytical calculations and the system-level simulation results are presented to verify the performance. To further confirm the effectiveness of the presented structure, the circuit-level implementation of the modulator is provided in TSMC 90 nm CMOS technology. The results show that the proposed modulator achieves a dynamic range of 82 dB over a 30 MHz bandwidth while consuming less than 18.2 mW power from a single 1 V power supply. With the proposed NSQ and SOR, both the order and bandwidth requirements of the loop filter are relaxed, and as a result, the analog complexity of the modulator is significantly reduced.

1. Introduction

The advances in the CMOS technology scaling has been resulted in restricting the voltage headroom of the circuits. As a consequence, the performance of the voltage-based mixed-mode circuits scales poorly with the technology improvement. Nevertheless, the scaling has led to the significant improvement in the time accuracy of digital circuits. It offers an attractive and technology friendly alternative for conventional amplitude-mode signal processing so-called as the time-based approach [1]. In the time-mode approach, the analog variables are represented by the time information rather than the nodal voltages or branch currents.

Time-mode circuits possess a number of intrinsic characteristics that are scaled well with CMOS technology. This feature makes them a promising and viable option to implement some of the key building blocks of mixed analog-digital systems such as analog-to-digital converters (ADCs) [1–3]. To realize wideband digital communication systems, low cost and low power ADCs are needed. Sigma-delta modulators (SDMs) have attracted a lot of attention as a high-resolution digital friendly structure for ADCs. They can be benefited from the superiority of the time-mode approach since the substantial part of the signal processing is performed in digital domain [4]. Recently, continuous-time sigma-delta modulators are widely used to digitize moderate to large bandwidth signals due to their efficient power consumption and silicon area [5]. The increased switching speed and the lower power consumption of transistors in modern CMOS technologies has emerged the time-based quantizers as a promising quantization architecture for CT sigma-delta modulators [6].

In [7], an open-loop time-mode ADC with low power consumption is introduced. Its performance, however, is severely affected by the nonlinearity of the voltage-to-time converter (VTC) and the resolution of the time-to-digital converter (TDC). As another example of the time-based modulators, in [8], a closed-loop CT sigma-delta modulator employing a synchronous ramp-based pulse-width modulator (PWM) as the VTC and a multi-bit flash TDC as the sampler is introduced. Noise floor increasing due to the aliasing effects of the synchronous sampler is the main shortcoming of this work. The time-encoded structures in [9,10] can also be categorized into the wideband high performance time-based CT sigma-delta modulators. However, their sampling rates

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are in the order of multi-GHz resulting in significant power consumption in the quantizer.

It is well-known that increasing the loop filter order and the sampling frequency theoretically improves the performance of a sigma-delta modulator. However, this achievement comes at the expense of higher power consumption and even the poor stability. On the other hand, enhancing the performance by using a multi-bit quantizer may require a multi-bit digital-to-analog converter (DAC) at the feedback path. This also increases the power consumption and degrades the linearity of the modulator. The noise transfer function (NTF) enhancement through the noise-coupling is found to be an efficient method to increase the noise-shaping order in SDMs. The concept has been well established for discrete-time (DT) SDMs in [11]. However, it is not straightforward to apply this technique in conventional continuous-time SDMs especially if a higher order enhancement is desired [12].

In this paper, a new method is developed to explore a linear model for the proposed time-based continuous-time sigma-delta modulator (TCSDM). Using this model, a concept similar to the noise-coupling technique is deployed to realize a noise-shaped quantizer (NSQ) for the TCSDM. The NSQ significantly enhances the noise-shaping order of the proposed TCSDM. The fully passive continuous-time implementation of the proposed NSQ is based on the Tustin's functions. Its core block is an asynchronous oscillatory pulse width modulator (PWM) followed by a fully digital polyphase sampler. The NSQ is designed to provide both the first- and second-order noise-shaping enhancement. Using the proposed NSQ in an Lth-order TCSDM gives the superiority of having an $L+1$ or $L+2$ order of noise-shaping. As will be discussed, this worthy achievement is obtained with a very low cost.

Furthermore, a novel single-opamp resonator (SOR) is introduced to be utilized in the proposed modulator. The proposed SOR emulates a second-order loop filter while utilizing a mere amplifier. This makes it possible to save more power consumption and die area. It also improves the stability of the proposed TCSDM by reducing the total amount of the loop delay and feedback branches.

The rest of the paper is organized as follows. The proposed NSQ along with the explored linearized model is introduced in Section 2. The system-level analysis and the simulation results of the proposed TCSDM are presented in Section 3. Section 4 is devoted to the proposed single-opamp resonator. In Section 5, the circuit-level implementation of the proposed TCSDM followed by the extensive simulation results are provided. Finally, Section 6 concludes the paper.

2. Noise-shaped quantizer

2.1. The non-linearity problem of the comparator

In Fig. 1, the conceptual block diagram of the proposed TCSDM is illustrated. It is comprised of an Lth-order loop filter, $H(s)$, and the NSQ with the noise-shaping order of L_{NS}. The NSQ itself can be conceived as an individual time-based sub-ADC. It is inherently a nonlinear block due to the existence of a comparator in its

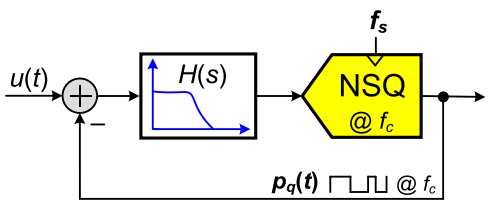

Fig. 1. The conceptual block diagram of the proposed modulator.

structure. In order to approximate the signal and noise transfer functions of the proposed TCSDM, a linearized model is required for the analysis. Some generalized approaches in the context of automated control systems, such as describing function (DF) have been already developed to introduce a semi-linear model for the comparator-based systems [13–16]. The usual assumption for applicability of the DF method is that the linear part of the system satisfies the filtering hypothesis [13]. Although, the DF theory can be regarded as an efficient method to calculate the NTF responses in CTSDMs, however, its dependency to the input signal amplitude makes some challenges.

If a comparator is located inside an oscillatory closed-loop system, its associated gain and phase can be calculated through the Barkhausen's criteria. For this case, the SDM is said to be working at the limit-cycle mode. This way, a linearized model may be attributed to the SDM for the sake of a simple mathematical analysis. However, voltage-mode continuous-time SDMs may not be benefited from this approach as they are not usually designed to work at the limit-cycle mode. In contrast, if the quantization is performed in time-domain, the associated time-based SDM can operate at both the clock [17] and the limit-cycle modes [18,19]. For a time-based SDM working at the limit-cycle mode, the oscillation frequency, f_c, can be regarded as a counterpart of the clock frequency, f_s, (i.e., $f_c < f_s$). This way, the nonlinearity problem of the comparator is analytically resolved making it possible to mathematically evaluate the modulator. For taking advantages of the time-based quantization approach, an interfacing block called as VTC is required to convert the signal from the voltage to the time-domain. The VTC can be realized using VCOs [20], PWMs [21] or voltage controlled delay units (VCDUs) [22,23]. In the proposed NSQ, an oscillatory VTC is utilized as is described in the following section.

2.2. The oscillatory voltage-to-time converter (VTC)

The core of the proposed NSQ is an oscillatory voltage-to-time converter (VTC). The oscillatory VTC is a closed-loop structure comprised of an integrator and a nonlinear element. Two types of comparator-based oscillatory VTCs are illustrated in Fig. 2. Based on the sampler position, they are classified into synchronous and asynchronous architectures. In the synchronous VTC, the oscillation frequency is an integer fraction of the sampling clock rate [19]. Thus, it cannot oscillate at any desired frequency. In contrast, the oscillation frequency of the asynchronous VTC depends only on the loop parameters and not on the sampling clock rate. This offers a degree of freedom in designing the various types of time-based quantizers. However, the oscillation controlling in asynchronous topologies is the main concern in some applications.

As shown in Fig. 2, the oscillatory VTC is comprised of a linear filtering block denoted by $A(s)$, the nonlinear element and the delay unit pointed as T_d. Denoting the zero-input oscillation frequency as f_c, the sampling frequency f_Q, is much higher than f_c for a proper functionality of the VTC (i.e., $f_Q \gg f_c$) [3]. The nonlinear element of the VTC can be a simple binary comparator. Since the asynchronous oscillatory VTC is the core of the proposed NSQ, its analysis is given in the following section.

2.3. Analysis of the asynchronous oscillatory VTC

The nonlinearity of the comparator makes it difficult to explore a linearized model for the proposed VTC-based NSQ. As previously mentioned, applying DFs is a frequently used method to model the binary comparator. However, the DF representation depends on the comparator input primary component [13]. However, if the comparator is located inside an oscillatory asynchronous VTC loop, its gain can be approximated by using the Barkhausen criteria.

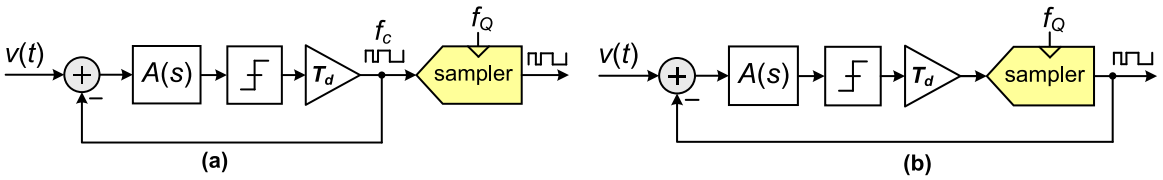

Fig. 2. The block diagram of the oscillatory VTC, (a) asynchronous, and (b) synchronous.

Notating the comparator approximated gain as k_{app}, the asynchronous VTC oscillates at the frequency of ω_c if:

$$A(j\omega)E(j\omega) = -1/k_{app.} \quad @\ \omega = \omega_c \tag{1}$$

where $A(j\omega)$ is the VTC filtering block defined as $\omega_a/(s+\omega_a)$ and $E(j\omega)=e^{-j\omega Td}$ represents the delay element of T_d. The phase relation of (1) can be stated as:

$$-\tan^{-1}(\omega_c/\omega_a) - \omega_c T_d - \pi = -2\pi \tag{2}$$

By solving the Eq. (2), the oscillation frequency, ω_c, can be estimated as:

$$\omega_c = \frac{\pi - \tan^{-1}(\omega_c/\omega_a)}{T_d} \approx \frac{\pi}{2T_d} \quad @\ \omega_c >> \omega_a \tag{3}$$

In order to extend the mathematical analysis of the VTC, a proper representation for the delay unit is also required to determine the k_{app}. There are some approximations that have rational polynomial forms for the delay element such as: Forward Euler (FE), Backward Euler (BE) and Tustin's approximations as are stated in Table 1, where $E(s)$ represents the delay element transfer function. To study their usefulness in the proposed linear model, the oscillatory VTC is simulated in MATLAB for different values of T_d. Then, the oscillation frequencies obtained from the simulation results are compared with the approximated one given in (3). The comparison verifies that the simulation results may have a negligible difference from (3) if the Tustin's approximation is applied for the delay unit. As a consequence, Tustin's functions will be applied to extend the mathematical analysis of the proposed modulator.

2.4. Approximation of the comparator gain

As discussed before, although determination of the comparator gain in the conventional voltage-mode quantizers is not a straightforward task, fortunately in the proposed NSQ, it can be linearly estimated since it is located inside an oscillatory loop. According to the oscillation conditions and by applying Tustin's representation for the delay element, the gain criteria of the oscillator can be calculated as:

$$\frac{\omega_a}{\sqrt{\omega^2+\omega_a^2}} \times \left|\frac{2-j\omega T_d}{2+j\omega T_d}\right| \times k_{app.} = 1 \quad @\ \omega = \omega_c \tag{4}$$

From (4), the approximated comparator gain $k_{app.}$ is calculated as:

$$k_{app.} = \sqrt{1+\left(\frac{\omega_c}{\omega_a}\right)^2} \tag{5}$$

where $k_{app.}$ is a constant value that depends only on ω_a and ω_c, and thus, it can be applied for the model extraction. It should be noted that, as is indicated in (3), this approximation remains valid if $\omega_c \gg \omega_a$. The minimum value of ω_a is determined by the RC-product of the filter $A(s)$. As a result, for some feasible values of ω_a, the approximated gain $k_{app.}$ can be applied for linear analysis of the VTC.

Table 1
Three different approximations of the delay element.

	Forward Euler approx. (F.E. approx.)	Backward Euler approx. (B.E. approx.)	Tustin's approx.
$E(s)$	$1 - sT_d$	$\frac{1}{1+sT_d}$	$\frac{2-sT_d}{2+sT_d}$

2.5. Noise-shaping concept in the oscillatory VTC

Based on the introduced oscillatory VTC, the proposed NSQ can now be presented. Its conceptual block diagram is shown in Fig. 3 (a). Also its modified version is illustrated in Fig. 3(b). In the NSQ block diagram, $G(s)$ is a continuous-time transfer function that is calculated according to the NTF of the NSQ. Realization of the proposed NSQ is feasible if a proper transfer function is selected for $G(s)$. For this target, the transfer function of the sampler is required. The time-based sampler performs a sample and hold operation with the sampling frequency of f_Q. The associated frequency response of this operation can be given as $sinc(f/f_Q)$. For $f \gg f_Q$, which is usually the case in SDMs, the magnitude of $sinc(f/f_Q)$ is assumed as 1. As a consequence, the linearized signal flow graph (SFG) of the NSQ can be explored. The SFG of the proposed NSQ is shown in Fig. 3(c) where E_Q denotes the quantization error.

According to the introduced SFG, the NTF of the proposed NSQ can be calculated as:

$$NTF(s) = \frac{1}{1+\left(\frac{A(s)E(s)k_{app.}G(s)}{1+A(s)E(s)k_{app.}(1-G(s))}\right)} \tag{6}$$

For a noise-shaped quantizer, the frequency response of NTF should be as a high-pass profile. For this to be achieved, the enclosed term in the denominator of (6) should have a low-pass response assumed as $L_{LPF}(s)$. This way, $G(s)$ can be calculated as:

$$G(s) = \left(\frac{1+A(s)E(s)k_{app.}}{A(s)E(s)k_{app.}}\right) \times \frac{L_{LPF}(s)}{1+L_{LPF}(s)} \tag{7}$$

For sufficiently large values of $k_{app.}$, the first term of (7) can be simplified as ≈ 1. As a result, the approximated representation of $G(s)$ can be stated as:

$$G(s) \approx \frac{L_{LPF}(s)}{1+L_{LPF}(s)} \tag{8}$$

Recalling the well-known approach in designing the discrete-time (DT) SDMs, z-domain analysis may be an efficient method to estimate $L_{LPF}(s)$. Let us represent $L_{LPF}(s)$ as $L_{LPF}(z)$ in DT domain. Among several techniques to perform the conversion from CT to the DT domain, Tustin's method is applied for this target. Noting that $L_{LPF}(z)$ is a DT low-pass filter, we can use the Tustin's mode of the "*d2c*" command in MATLAB to calculate $L_{LPF}(s)$. The normalized results are summarized in Table 2 where $F(s)=1-G(s)$.

Simulation results of the NSQ for different orders of the noise-

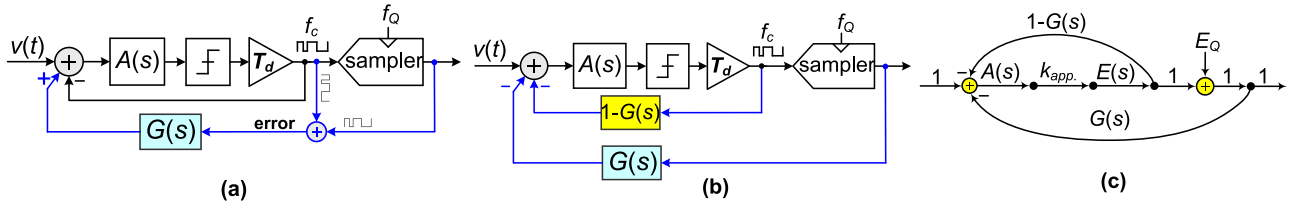

Fig. 3. The proposed NSQ (a) its primary scheme based on the noise-coupling concept, (b) the modified version of Fig. 3(a) and (c) the NSQ linearized signal-flow graph (SFG).

Table 2
Calculation of the Tustin's functions for the proposed NSQ.

Noise-shaping order (L_{NS})	$T_{LPF}(z)$	$G(s)$	$F(s)$
$L_{NS}=1$	$\frac{1}{1-z^{-1}}$	$\frac{0.34s+0.67}{s+0.67}$	$\frac{0.67s}{s+0.67}$
$L_{NS}=2$	$\frac{1}{\left(1-z^{-1}\right)^2}$	$\frac{0.2s^2+0.8s+0.8}{s^2+0.8s+0.8}$	$\frac{0.8s^2}{s^2+0.8s+0.8}$

shaping (L_{NS}) are illustrated in Fig. 4. For this simulation, the oscillation frequency, f_c, is 550 MHz and ω_c/ω_a is 200. As is clear, the proposed NSQ is capable in achieving first- and second-order noise-shaping provided that a proper transfer function is determined for $G(s)$.

2.6. Implementation of the Tustin's functions

Although the proposed NSQ shows its superiority in enhancing the shaping order of the quantization noise, however, its implementation may be a challenging task. Here, a novel realization of the proposed NSQ according to the calculated Tustin's functions is introduced. Regarding to the presence of an amplifier in the VTC front-end, the 1st and 2nd order Tustin's functions can be implemented using only passive elements. In both structures shown in Fig. 5, the transfer function V_m/V_a refers to the $F(s)$ while Vn/Vb realizes the $G(s)$. In the case of $L_{NS}=2$, the damping factor of $G(s)$ is slightly deviated from the one denoted in Table 2. By choosing the damping factor close to 1 (i.e., $\xi \approx 1$), $G(s)$ can be realized using cascaded RC-ladders. The synthesized transfer functions of the NSQ are given in Table 3. The other superiority is that the inherent excess loop delay (ELD) of the proposed quantizer is simply compensated by trimming the gain scaling factor realized by R_{ELD}.

2.7. Implementation of the poly-phase sampler

For an oscillatory VTC, the minimum required sampling frequency, f_Q, for the proper detection of the pulse edges is $f_Q > 4 \times f_c$ [3]. However, utilizing the double-sampled D-flip flops reduces the clock rate as $f_s=f_Q/2N$, where N is the number of the TDC stages [3]. The poly-phase sampler, shown in Fig. 6, is composed of an N-stage time-to-digital converter (TDC) followed by a digital-to-time converter (DTC). The resolution of the TDC is T_Q (i.e., $T_Q=1/f_Q$). The TDC is clocked at the rate of f_s where $f_s=f_Q/2N$. The combination of TDC/DTC works as the combination of an ADC/DAC, thus resolving the need of a multi-bit DAC at the feedback path. Compared to the 50-stage TDC utilized in [8], the proposed TCSDM requires much less TDC quantization levels making it more beneficial from the points of power consumption and design complexity. More details about the proposed poly-phase sampler are presented in [3].

3. System-level simulation of the proposed TCSDM

3.1. The block diagram of the proposed TCSDM

The block diagram of the proposed TCSDM based on the NSQ is shown in Fig. 7. The order of the modulator's loop filter is $L=2$. The filter $H(s)$ has a cascaded integrator feed-forward (CIFF) resonator topology. The passive LPF represented as $L_f(s)=\omega_f/(s+\omega_f)$ is employed in the feedback path to suppress the high frequency tones of $p_q(t)$ before being injected into the feedforward path. This is required since the high frequency tones may destabilize the oscillatory VTC. Furthermore, $L_f(s)$ decreases the modulator's sensitivity to the clock jitter and also alleviates the swing and slew rate requirements of the amplifiers. The filter $L_f(s)$ can also represent the impulse response of the DAC while deriving the linear model of the TCSDM. The gain block denoted as k_{ELD} is used to compensate the excess loop delay (ELD) of the modulator.

3.2. System-level simulation results of the proposed TCSDM

The performance of the proposed TCSDM can be evaluated if the power spectral density (PSD) of the quantization error is

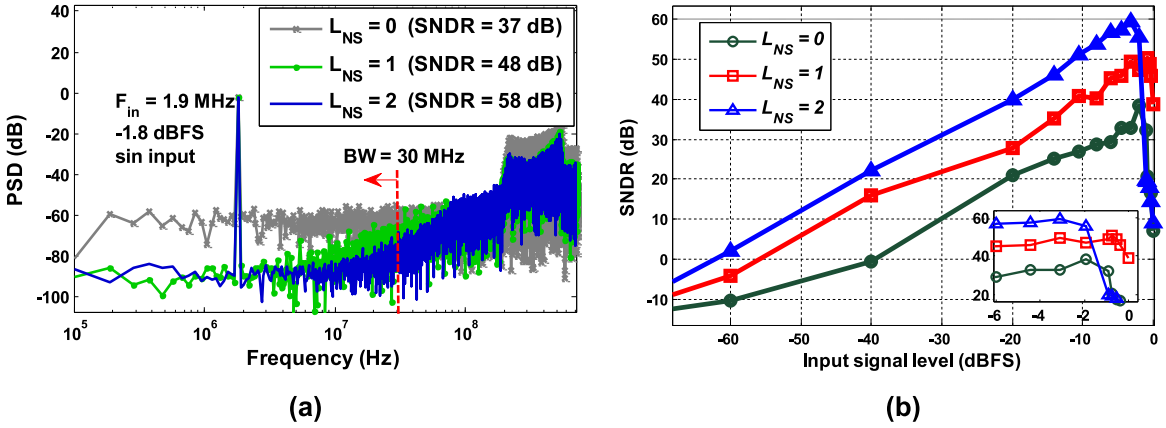

Fig. 4. Proposed NSQ performance, (a) the PSDs for different orders of L_{NS}, and (b) the SNDR versus the input signal amplitude.

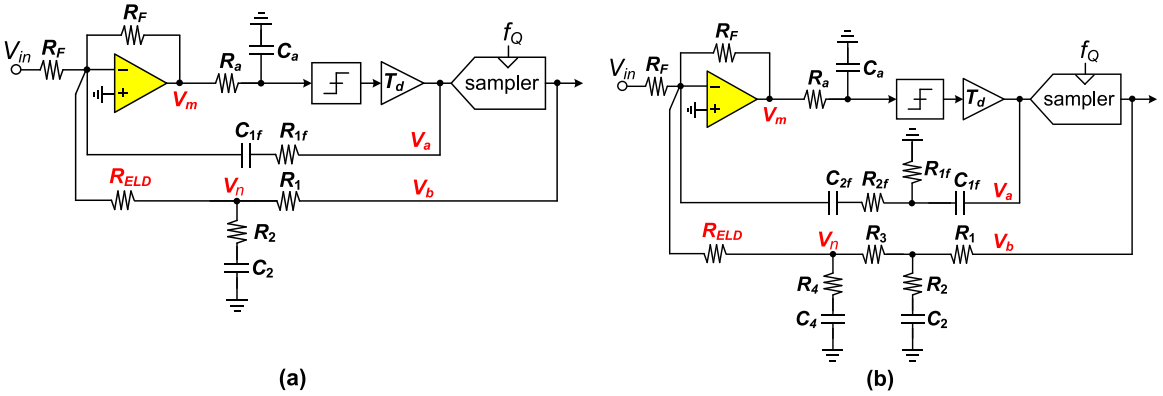

Fig. 5. Implementation of the proposed NSQ Tustin's functions, (a) $L_{NS}=1$, and (b) $L_{NS}=2$.

available. According to the approach introduced in [3], the SNR within the bandwidth of f_{BW} is calculated as:

$$SNR \simeq \frac{3}{8}U_p^2\left(L_{eff}-0.5\right)^2\frac{2L_{eff}+1}{\pi^{2L_{eff}}}\left(\frac{f_Q}{f_c}\right)^2 OCR^{2L_{eff}+1} \tag{9}$$

where U_p is the input signal amplitude, $L_{eff}=L+L_{NS}$ and OCR is the over-cycling ratio stated as $f_c/2f_{BW}$. According to (9), for a TCSDM with $L=2$ and $OCR=8$, the SNR improvement is about 36 dB just by applying a 2nd-order NSQ. For system-level simulation of the proposed TCSDM, the parameters listed in Table 4 are used. According to the linearized model developed in the previous section, the signal and noise transfer functions can be calculated as they are presented in Table 5. These transfer functions are useful in evaluating the efficiency of the NSQ on the proposed TCSDM performance. Thus, the estimated NTF responses of the TCSDM according to the introduced linear model are shown in Fig. 8(a). As shown, the shaping order of the NTFs for different cases verifies the introduced model. The simulated PSD of the proposed TCSDM for a −2 dBFS sinusoidal input signal is also illustrated in Fig. 8(b).

3.3. Clock jitter performance of the proposed TCSDM

The clock jitter error can degrade the performance of continuous-time SDMs. The analysis of the conventional voltage-based continuous-time SDMs is elaborated in [24,25]. However, in the proposed architecture, where the time-based approach is applied for the quantization, the result may be different to some extent. Although, the effect of random pulse position modulation on a time-quantized signal is a demanding task to analyze with equations, the necessary insight can be achieved through simulations [8]. In the proposed quantizer, since the TDC outputs are merged by a DTC, some jitter rejection may be expected. Both the rising and falling edges of the feedback pulse denoted as $p_q(t)$ carry approximately the same time shift in the presence of the clock jitter. Thus, the clock jitter affects only the position of the feedback pulse and the pulse width remains approximately unchanged. Furthermore, the probable errors in the clock signal can be shaped since the TDC is located inside the modulator's loop. However, the variations of the $p_q(t)$ pulse can be seen as a clock jitter. The performance of the proposed TCSDM with the parameters of Table 4, using the jitter model introduced in [26] is plotted in Fig. 9. As is see, an acceptable robustness of the SNDR variation across the jitter noise in the proposed TCSDM compared to the conventional CT sigma-delta modulators such as [24] is achieved. This is owing to the pulse width invariance in the presence of clock jitter and also due to the utilization of $L_f(s)$ in the outer feedback path of the modulator.

4. Single-opamp resonator (SOR)

4.1. The loop filter topologies and their constraints

As is clear, the loop filter in a SDM dissipates a significant amount of the power and occupies a major portion of the die area. They are usually realized using a chain of integrators with either feedback or feedforward paths. In feedforward structures, the signal component at the output of the loop filter integrators is reduced and the modulator sensitivity to the integrator nonlinearities is decreased. Moreover, feedforward filters are the best solution when implementing low-power modulators, since only one feedback path is provided, and hence, only one DAC is theoretically required [27]. For a given signal bandwidth, increasing the loop filter order is recognized as one of the most effective ways to improve the modulator SNR. However, this approach needs more integrators resulting in more power dissipation and also larger silicon die area.

4.2. Realization of the second-order loop filter

As illustrated in Fig. 7, the loop filter of the proposed TCSDM is a second-order feed-forward resonator. The local feedback path including the gain block of g realizes a resonance frequency close to the bandwidth of the SDM. This topology can realize a zero-optimized NTF for the SDM. It can be shown that if the resonance frequency is optimally placed in the desired bandwidth, the SNR is multiplied by $(L-0.5)^2$ [27]. The attributed transfer function of this

Table 3
Circuit-level realization of the Tustin's functions in the NSQ.

Tustin functions	$L_{NS}=1$	$L_{NS}=2$
$G(s)$	$\frac{sR_2C_2+1}{sC_2(R_1+R_2)+1}$	$\frac{s^2(R_2R_4C_2C_4)+s(R_2C_2+R_4C_4)+1}{s^2C_2C_4(R_1R_3+R_2R_3+R_1R_2+R_2R_4+R_1R_4)+s(R_3C_4+R_1C_4+R_4C_4+R_2C_2+R_1C_2)+1}$
$F(s)$	$-\frac{sR_FC_1}{sR_1C_1+1}$	$-\frac{s^2\left(R_FR_{1f}C_{1f}C_{2f}\right)}{s^2\left(R_{1f}R_{2f}C_{1f}C_{2f}\right)+s\left(R_{1f}C_{1f}+R_{2f}C_{2f}+R_{1f}C_{2f}\right)+1}$

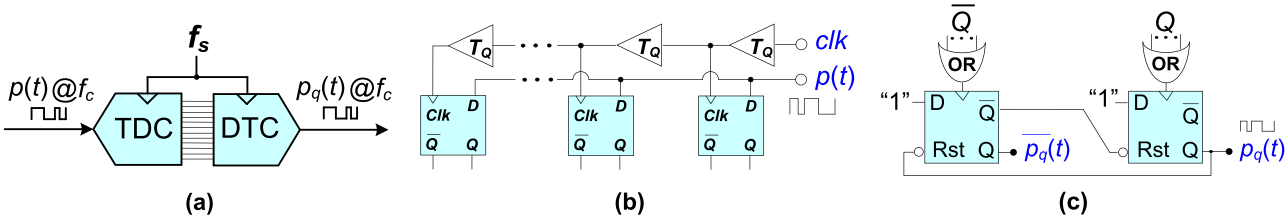

Fig. 6. (a) The proposed poly-phase sampler, (b) *N*-stage TDC, and (c) asynchronous DTC.

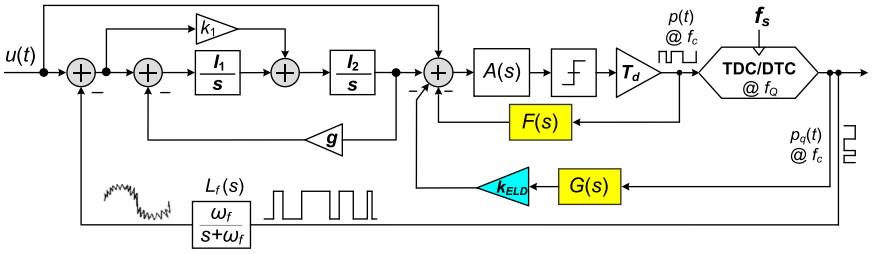

Fig. 7. The block diagram of the proposed TCSDM for $L=2$, $L_{NS}=2$ and $L_{eff}=4$.

Table 4
TCSDM system level parameters used in the simulations of Figs. 8 and 9.

2nd-order TCSDM with $L_{NC}=2$ (system level)					
N	6	k	1	T_Q (psec)	80
g	0.09	k_g	1.8	T (nsec)	1.5
I_1	3.8×10^8	f_c (MHz)	550	ω_a/ω_c	0.005
I_2	8.37×10^8	f_s (GHz)	1.04	ω_f (Mrad/sec)	$2\pi\times80$

Table 5
Estimated STF and NTF of the TCSDM using the proposed linearized model.

Noise-shaping order (L_{NS})	**STF (s)**	**NTF (s)**
$L_{NS}=0$	$\frac{k_{app}A(s)E(s)(1+H_0(s))}{1+k_{app}A(s)E(s)(1+H_0(s)L_f(s))}$	$\frac{1+k_{app}A(s)E(s)}{1+k_{app}A(s)E(s)(1+H_0(s)L_f(s))}$
$L_{NS}=1$	$\frac{k_{app}A(s)E(s)(1+H_1(s))}{1+k_{app}A(s)E(s)(1+H_1(s)L_f(s))}$	$\frac{1+k_{app}A(s)E(s)F_1(s)}{1+k_{app}A(s)E(s)(1+H_1(s)L_f(s))}$
$L_{NS}=2$	$\frac{k_{app}A(s)E(s)(1+H_2(s))}{1+k_{app}A(s)E(s)(1+H_2(s)L_f(s))}$	$\frac{1+k_{app}A(s)E(s)F_2(s)}{1+k_{app}A(s)E(s)(1+H_2(s)L_f(s))}$

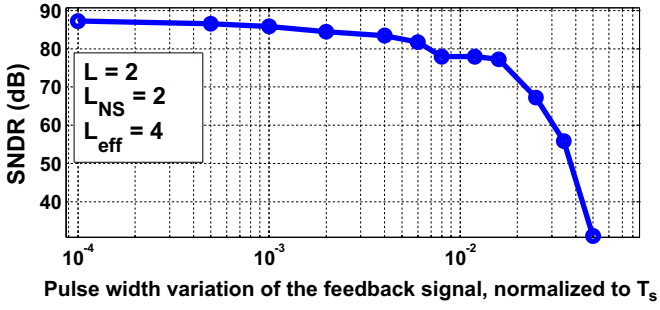

Fig. 9. SNDR versus the feedback pulse width variations.

resonator can be stated as:

$$H(s)=\frac{kI_1s+I_1I_2}{s^2+gI_1I_2} \tag{10}$$

where I_1, I_2 and k are the resonator gains and feedforward coefficient, respectively.

The finite gain bandwidth (GBW) of the amplifier in the integral path of the modulator causes a large phase delay. This can destabilize the modulator. More power consumption is required to

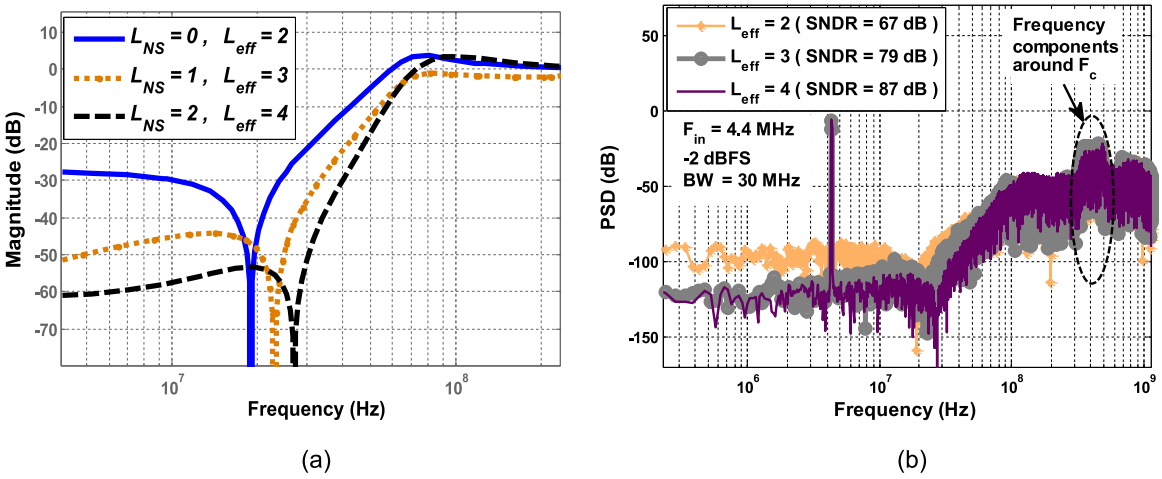

Fig. 8. (a) Estimation of the proposed TCSDM NTF responses according to the explored linearized model, and (b) system-level simulation results of the proposed TCSDM.

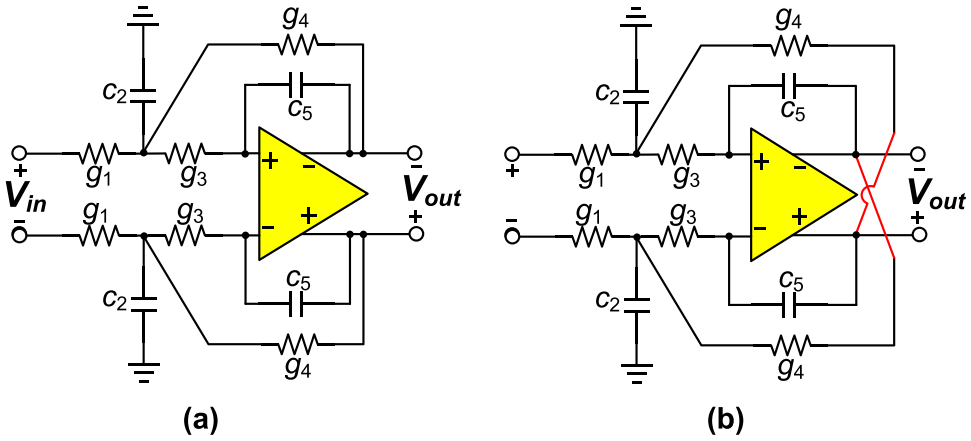

Fig. 10. Conventional realization of the second-order biquadratic transfer function using single-amplifier network, (a) stable but with a non-zero damping factor, and (b) zero-damped unstable network.

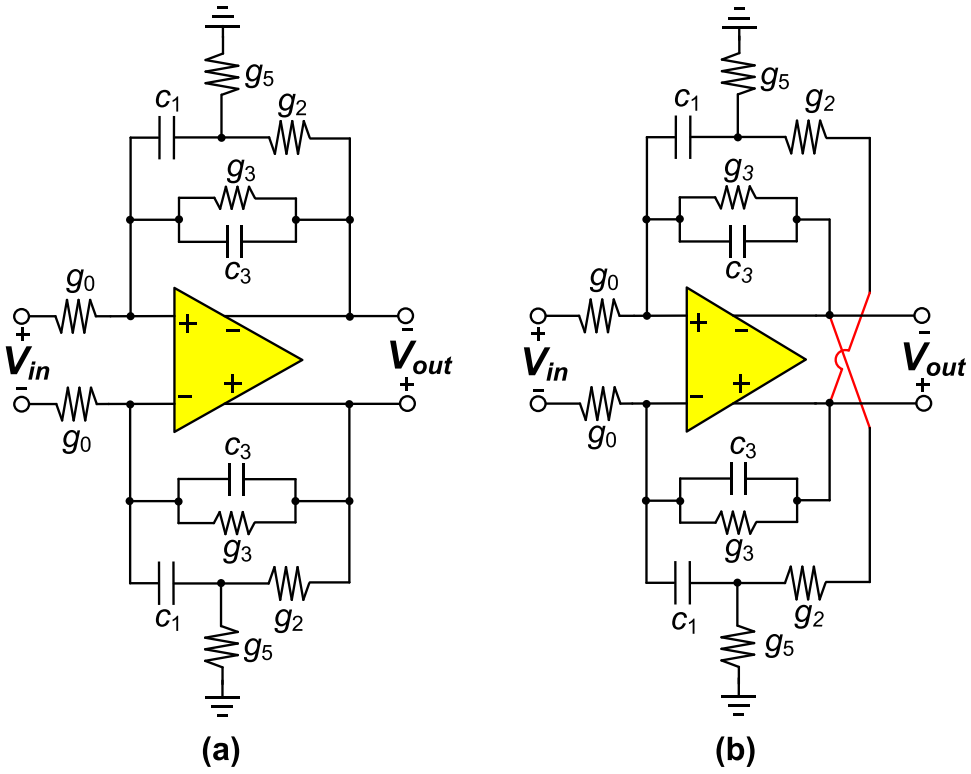

Fig. 11. (a) The proposed second-order biquadratic transfer function with a non-zero damping factor, and (b) proposed stable zero-damped single-opamp resonator (SOR).

enhance the opamp GBW and improve the loop phase delay effect. Reducing the number of filter amplifiers will enhance the achievable figure of merit (FoM) since it decreases the power consumption, loop phase delay, and the modulator total die area. Single amplifier biquads (SABs) can be utilized to realize a second-order loop filter with only one amplifier. The following section is devoted to study the feasibility of using a SAB for the proposed TCSDM.

4.3. Single amplifier biquads

It is possible to implement the loop filter in a way that combines both advantages of active and passive networks. This has been presented in [28] and it consists of a passive network and a single amplifier. The network is called a single amplifier biquad (SAB). The transfer function of a general biquadratic low-pass filter is as:

$$H(s) = \frac{a_2 s^2 + a_1 s + a_0}{s^2 + 2\xi\omega_n + \omega_n^2} \tag{11}$$

where ω_n is the undamped natural frequency and ξ is the damping factor of the filter. The coefficient a_2 can also be considered as zero for low-pass filters. A conventional implementation of a typical low-pass SAB is shown in Fig. 10(a). This network can't be applied in the modulator front-end, since its input signal is not connected to the virtual ground. Furthermore, this network has a non-zero damping factor. This makes it impossible to realize an ideal second-order resonator unless it is somehow modified. Realizing a negative resistance by making a positive feedback may be the primary alternative to remove the damping factor. This is accomplished via reversing the connections of g_4 to the output. The modified network is shown in Fig. 10(b). Its transfer function can

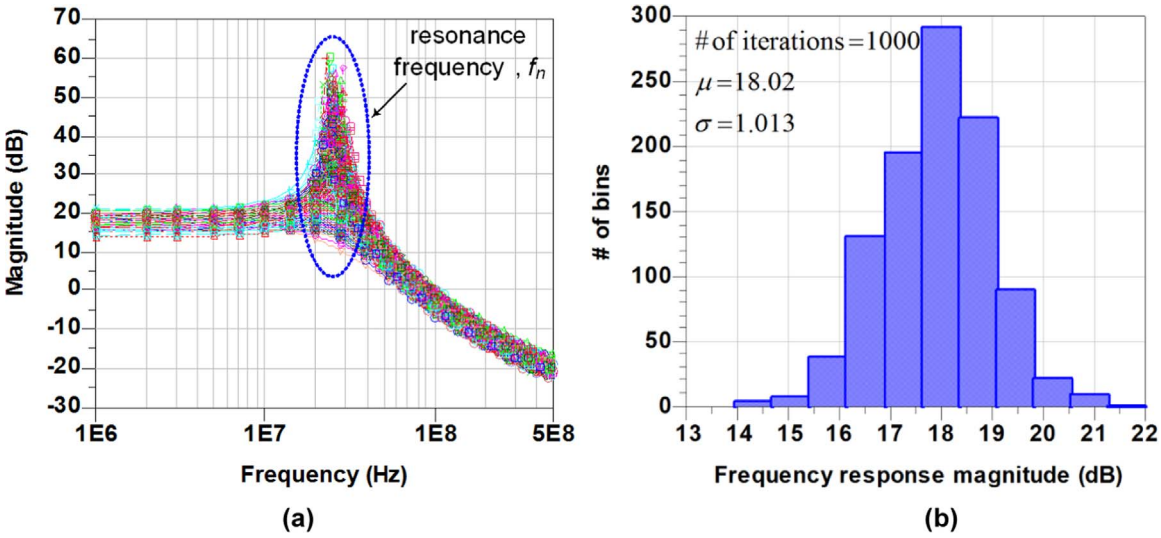

Fig. 12. (a) Monte Carlo simulation result of the proposed SOR, and (b) histogram of the SOR gain variations.

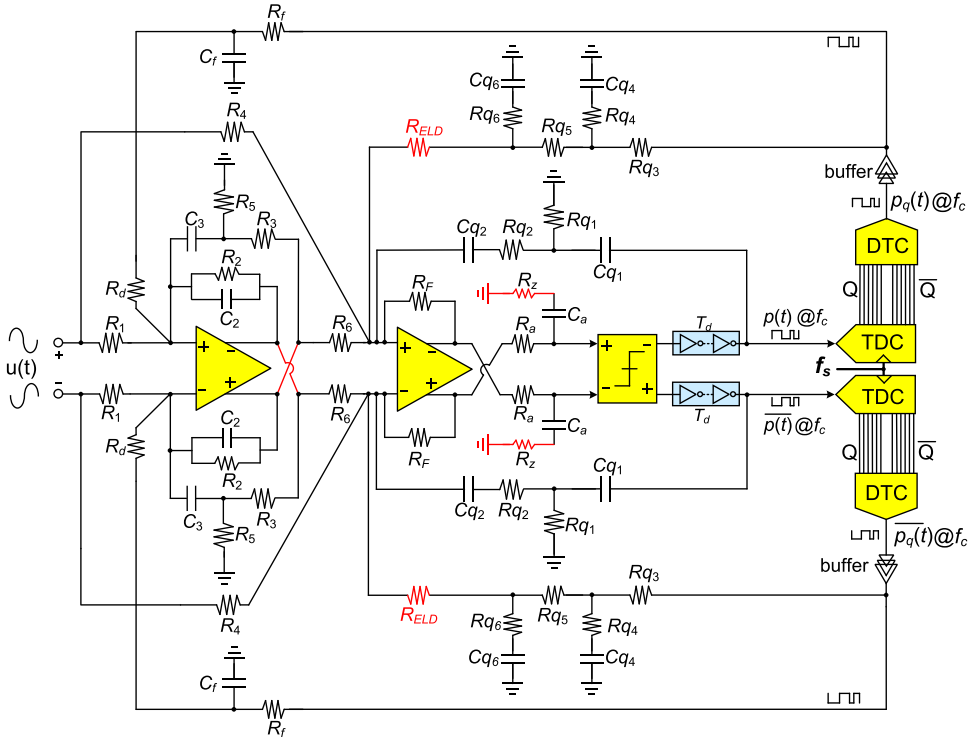

Fig. 13. Fully-differential implementation of the proposed TCSDM with L=2, L_{NS}=2 and L_{eff}=4.

also be calculated as:

$$H_a(s) = \frac{s\left(\frac{g_1 g_3}{c_2 g_4}\right) + \left(\frac{g_1 g_3}{c_1 c_2}\right)}{s^2 - \left(\frac{g_2 g_3}{c_1 c_2}\right)} \quad ; \text{unstable}$$

$$!\text{when} \quad g_2 = g_4\left(\frac{g_1 + g_3}{g_3 + g_4}\right) \tag{12}$$

As (12) indicates, the modified network is an unstable one since the poles are located at the right half plane (RHP).

4.4. Proposed single-opamp resonator (SOR)

In order to utilize the biquadratic network in the modulator front-end, its input signal should be connected to the virtual ground. The primary schematic of the proposed single-opamp network for the modulator loop filter is shown in Fig. 11(a). As it is clear, the input signal is applied to the virtual ground. The transfer function of this network is calculated as:

$$H_{b1}(s) = g_0 \times \frac{s\left(\frac{1}{c_3}\right) + \left(\frac{g_2 + g_5}{c_1 c_3}\right)}{s^2 + s\left(\frac{g_3 c_1 + g_5 c_3 + g_2(c_1 + c_3)}{c_1 c_3}\right) + g_3\left(\frac{g_2 + g_5}{c_1 c_3}\right)} \tag{13}$$

As it is obvious, the non-zero damping factor is still remained in this network. This makes it an unsuitable alternative for the second-order resonator.

As mentioned before, a positive feedback path is required to remove the damping factor in the second-order biquadratic

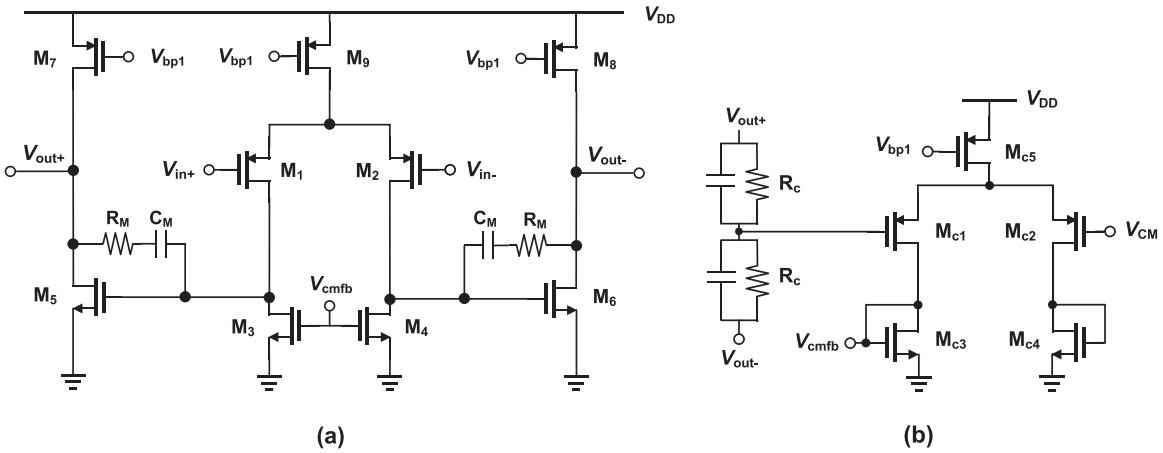

Fig. 14. (a) Two-stage OTA, and (b) the schematic of the common-mode feedback (CMFB) circuit.

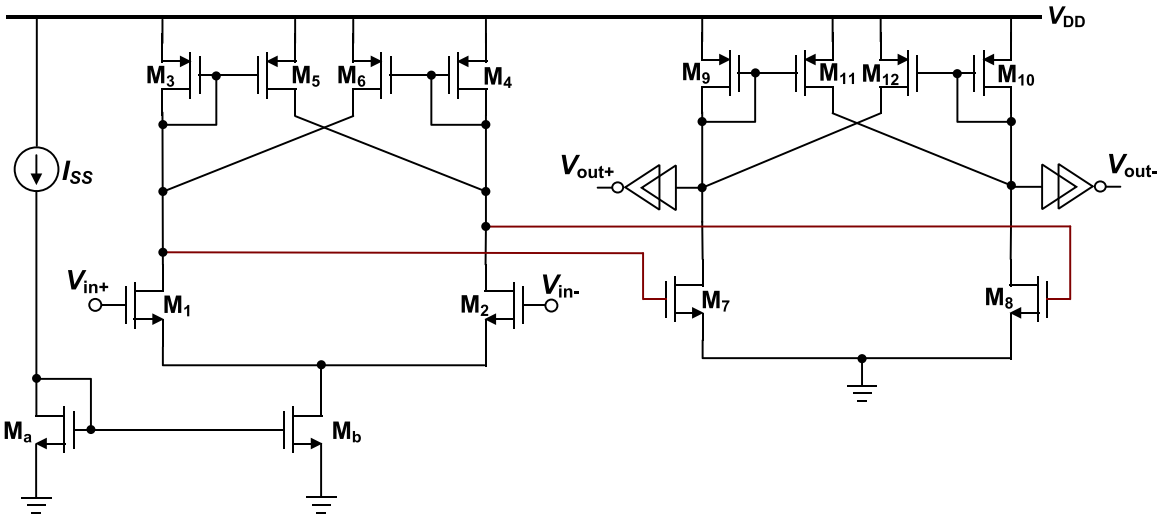

Fig. 15. Continuous-time binary comparator.

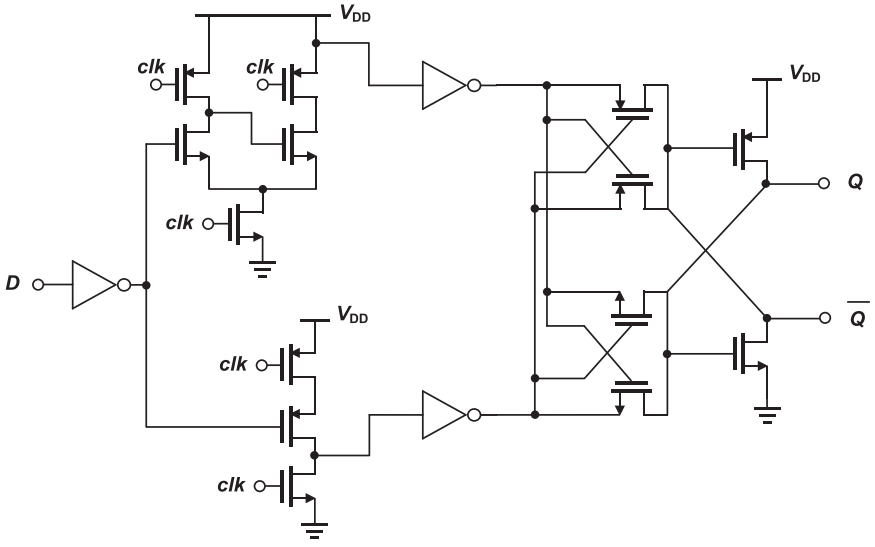

Fig. 16. Implementation of the proposed double-sampled D-flip flop used in the TDC.

network. However, this should not destabilize the network. By applying the positive feedback in the proposed biquadratic network, the modified version of the network is realized as shown in Fig. 11(b). This network can be regarded as a suitable alternative for the ideal resonator if the damping factor is removed and also the network remains stable with the applied positive feedback.

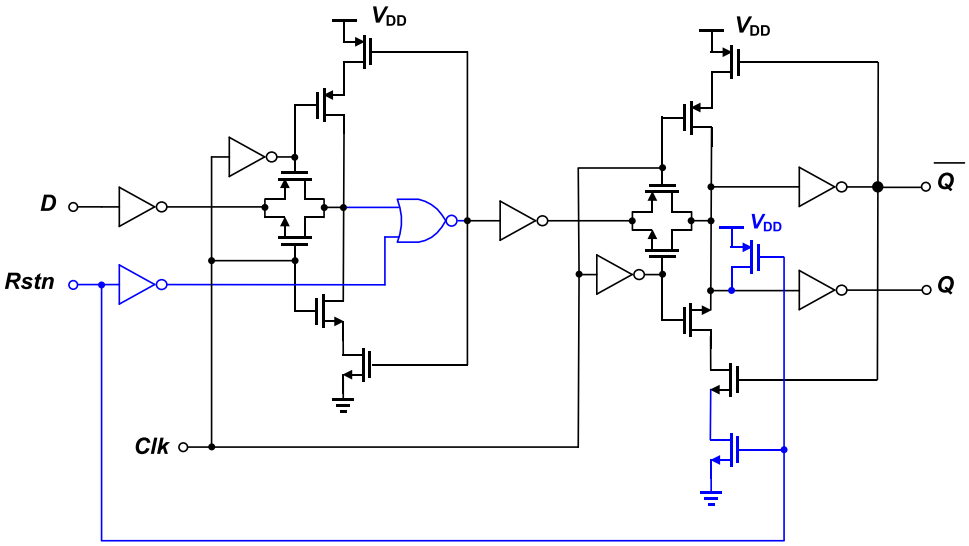

Fig. 17. Implementation of the resetable D-flip flop used in the DTC logic.

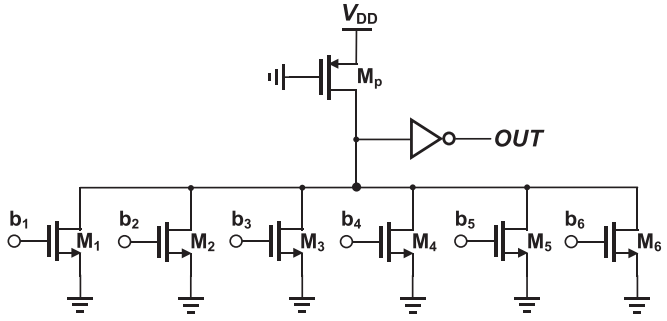

Fig. 18. Implementation of the 6-input wired OR gate.

The transfer function of the proposed single-opamp resonator (SOR) is calculated as:

$$H_{b2}(s) = g_0 \times \frac{s\left(\frac{1}{c_3}\right) + \left(\frac{g_2+g_5}{c_1c_3}\right)}{s^2 + g_3\left(\frac{g_5-g_2}{c_1c_3}\right)} \quad ; \text{when} \quad g_2 = \left(\frac{g_3c_1 + g_5c_3}{c_1 + c_3}\right) \tag{14}$$

As it is clear, the zero-damped $H_b(s)$ with the mentioned condition is a stable network since the poles are not located at the RHP. The main features of the proposed SOR are: 1) it successfully realizes the resonator transfer function in (10), 2) unlike the filter in Fig. 10(a), the input signal is applied to the virtual ground making it possible to be utilized in the modulator front-end to subtract the feedback signal directly from the input and 3) compared with [29], the proposed SOR has smaller number of the elements (since the number of the capacitances is equal to the resonator order), leading to an area reduction.

The robustness of the proposed SOR is also examined using the Monte Carlo simulations. In this simulation, ±%15 standard deviation (*stdev*) in the values of the filter element is assumed. The magnitude and also the histogram of the network response variation for 1000 iterations are depicted in Fig. 12. As is obtained from Fig. 12(a), the resonance frequency, f_n, (the main feature of the SOR) have a good degree of the robustness against the variation of the filter elements. It should be noted that using the NSQ to enhance the modulator performance alleviates the gain constraint of the resonator. This makes it possible to save more power by using a resonator with a moderate gain.

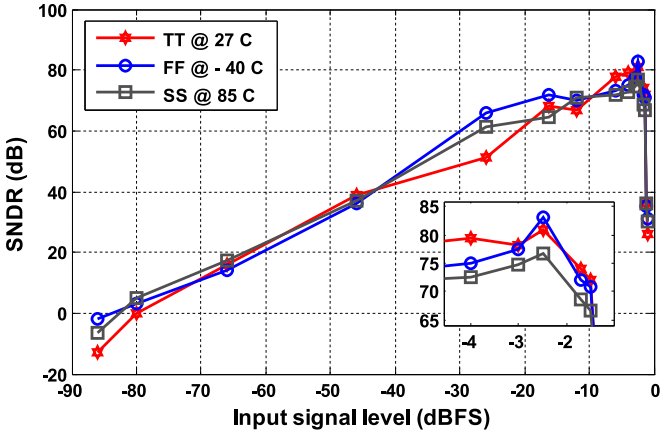

Fig. 19. Circuit-level simulation results of the SNDR versus the input signal amplitude in different process corner cases.

5. Implementation of the proposed TCSDM

5.1. Circuit-level implementation

The differential circuit level implementation of the proposed

Table 6
Design parameters of the circuit-level implementation.

TCSDM with L_{NS}=2 and L_{eff} =4 (circuit-level)											
R_1	2 kΩ	R_6	5 kΩ	R_z	400 Ω	R_{q4}	1 kΩ	C_2	1.3 pF	C_{q4}	316 fF
R_2	19 kΩ	R_d	625 Ω	R_a	5 kΩ	R_{q5}	500 Ω	C_3	4.9 pF	C_{q6}	950 fF
R_3	850 Ω	R_F	5 kΩ	R_f	500 Ω	R_{q6}	1 kΩ	C_a	1.6 pF	C_f	5.78 pF
R_4	5 kΩ	R_{q1}	60 Ω	R_{ELD}	1.16 kΩ	N	6	C_{q1}	30 pF		
R_5	450 Ω	R_{q2}	5.5 kΩ	R_{q3}	1 kΩ	f_s	1 GHz	C_{q2}	500 fF		

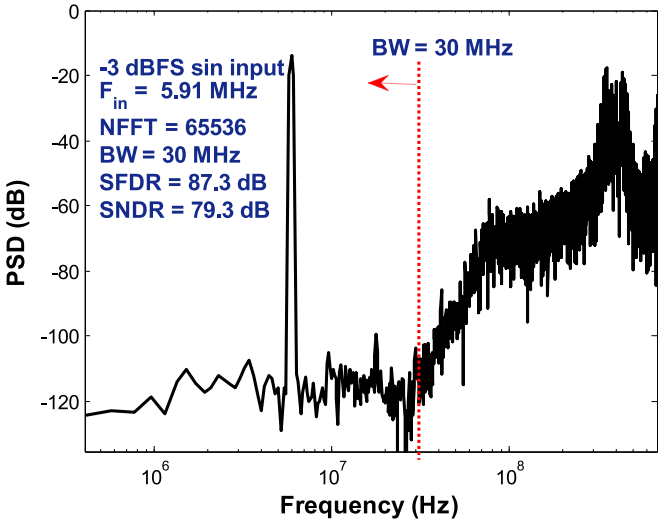

Fig. 20. Circuit-level PSD simulation of the proposed TCSDM (TT@27 °C).

Table 7
Summary of the circuit-level simulated performance.

Type	Time-quantized $CT-\Sigma\Delta M$	
Loop filter order (L)	2	
NSQ order (L_{NS})	2	
Noise-shaping order (L_{eff})	4	
f_c	500 MHz	
f_s	1.04 GHz	
***N*-TDC**	6	
BW	30 MHz	
OCR (f_c/2*BW)	8.3	
Peak SNDR	Excluding circuit noise	79.4 dB
	Including circuit noise	77.6 dB
DR	82 dB (TT@27 °C)	
Technology	TSMC 90 nm CMOS	
Supply voltage	1 V	
Power	18.2 mW	
FoM (P/(2*BW*2^{ENOB}))	38 fJ/conv-step	

TCSDM based on the NSQ and second-order SOR is shown in Fig. 13. In the proposed modulator, the ELD compensation is done through the trimming of both R_{ELD} and R_z. The additional resistance denoted by R_z reduces the delay of $A(s)$, thus improving the phase margin of the NSQ loop. This way, the ELD of the modulator is partially compensated. Furthermore, trimming the scaling factor realized by R_{ELD} can fulfill the compensation procedure for the proposed TCSDM. The values of these compensation elements are accurately obtained through extensive trial and error simulations.

The topology of the OTAs used in both the SOR and the summing amplifier are identical for the sake of implementation simplicity. The amplifier required for the summing node needs to be a high speed one since it is located inside the ELD compensation loop. Hence, its UGBW is designed to be at least five times the NSQ oscillation frequency. However, it does not need a high dc gain. In order to better satisfy the swing constraints of the SOR and the summing amplifier, Miller-compensated two-stage OTAs are selected for both of them. The schematics of the amplifiers and also their associated common-mode feedback (CMFB) circuit are shown in Fig. 14.

The schematic of the nonlinear block located within the NSQ is illustrated in Fig. 15. It is comprised of a fully continuous-time cross-coupled preamplifier followed by a simple comparator.

The proposed 6-stage TDC which is previously shown in Fig. 6 utilizes a novel implementation of the double-sampled DFF. Its clock phases are generated using cascaded CMOS inverters. The circuit level implementation of the proposed double-sampled DFF is shown in Fig. 16. It is based on true single-phase-clocked (TSPC) logic for its high speed and low power performance. This DFF is comprised of two positive and negative latches which their outputs are merged by a pass transistor logic (PTL) XOR gate to be able to detect both the rising and falling edges of $p(t)$. As previously mentioned, the DTC logic is composed of the two multi-input OR gate forwarded by DFFs with an asynchronous reset. The DFF included in the DTC logic is shown in Fig. 17. A simple wired OR gate, similar to the one introduced in [30], is applied for the proposed DTC. Its schematic is shown in Fig. 18.

The circuit-level design parameters of the proposed TCSDM are given in Table 6. The proposed TCSDM is designed and simulated in TSMC 90 nm CMOS technology with 1 V power supply.

5.2. Circuit-level simulation results

Transistor level simulations in different process corner cases and temperature variations are performed to further verify the effectiveness of the proposed modulator. The simulation result in Fig. 19 shows an acceptable degree of the modulator robustness in different conditions. As is shown, a dynamic range greater than 82 dB in a 30-MHz bandwidth can be achieved in the typical-typical (TT @ 27 °C) process corner case. The simulated PSD of the modulator with a 5.9 MHz, −3 dBFS sin input signal is shown in Fig. 20. Taking into account the circuit noise of the modulator with calculating its power within the desired bandwidth, a loss of approximately 3 dB is incorporated in the previously defined SNDR values.

Table 7 summarizes the simulated performance of the proposed TCSDM. In Table 8, the simulated performance of the

Table 8
Performance comparison of the proposed SDM with several alternatives.

References	SNDR (dB)	BW (MHz)	Power (mW)	Output rate (MHz)	Technology (nm)	Supply voltage (V)	FoM (fJ/conv.step)
[4][a] **JSSC'08**	55	20	38	950	130	1.5	2058
[8][a] **JSSC'11**	60	20	10.5	250	65	1	319
[10][a] **JSSC'11**	61	20	7	2560	65	1	170
[18][a] **JSSC'11**	56.1	5	6	850	180	1.8	1090
[31][b] **TCAS-I'07**	66	10	7.5	640	180	1.8	110
[32][b] **AICSP'08**	70	25	16.4	800	90	1	69
[33][b] **MWSCAS'10**	82	10	36.1	320	180	1.8	177
[34][b] **EDSSC'14**	83	2	10	128	180	1.8	216
[35][b] **MWSCAS'14**	43	10	17.3	1000	350	3.3	546
[36][b] **CTA'15**	80	30	26	450	90	1	72
[37][a] **MEJO'13**	82.7	0.02	0.264	2.56	180	0.8	360
This work[b]	79.4	30	18.2	500	90	1	38

[a] Measurement results.
[b] Simulation results.

proposed modulator is compared with some other works. Although, the performance of the proposed modulator is verified through the extensive circuit-level simulations rather than the measurement results, the reasonable achieved FoM under the various corner cases and temperature variations confirms its performance as a good candidate for broadband and low-voltage applications.

6. Conclusions

In this paper, a novel time-based continuous-time sigma-delta modulator notated as TCSDM is proposed. It leverages the new NTF enhancement technique to realize a noise-shaped quantizer (NSQ) to improve its performance. Thanks to the time-based approach applied for the quantization, exploiting a linearized model for the proposed modulator is evaluated. The proposed TCSDM benefits from a fully digital TDC followed by a DTC as the polyphase sampler. This makes it possible to avoid using the nonlinear multi-bit DAC at the modulator feedback path. On the other hand, by combining the TDC and DTC, the robustness of the proposed modulator against the clock jitter is improved due to the invariance of the feedback pulse width. Furthermore, a novel single-opamp resonator (SOR) is also presented to realize the second-order loop filter. Simulation results performed in both system and circuit levels confirm the effectiveness of the proposed NTF-enhanced TCSDM. Furthermore, by applying the proposed NSQ and SOR in the TCSDM, the modulator design complexity becomes more relaxed. The simulation results are also illustrated and compared with the analytical derivations to confirm the usefulness of the proposed modulator.

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