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A wideband time-based continuous-time sigma-delta modulator with 2nd order noise-coupling based on passive elements

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SUMMARY

Embedding the time encoding approach inside the loop of the sigma-delta modulators has been shown as a promising alternative to overcome the resolution problems of analog-to-digital converters in low-voltage complementary metal-oxide semiconductor (CMOS) circuits. In this paper, a wideband noise-transfer-function (NTF)-enhanced time-based continuous-time sigma-delta modulator (TCSDM) with a second-order noise-coupling is presented. The proposed structure benefits from the combination of an asynchronous pulse width modulator as the voltage-to-time converter and a time-to-digital converter as the sampler to realize the time quantization. By using a novel implementation of the analog-based noise-coupling technique, the modulator's noise-shaping order is improved by two. The concept is elaborated for an NTF-enhanced second-order TCSDM, and the comparative analytical calculations and behavioral simulation results are presented to verify the performance of the proposed structure. To further confirm the effectiveness of the presented structure, the circuit-level implementation of the modulator is provided in Taiwan Semiconductor Manufacturing Company (TSMC) 90 nm CMOS technology. The simulation results show that the proposed modulator achieves a dynamic range of 84 dB over 30 MHz bandwidth while consuming less than 25 mW power from a single 1 V power supply. With the proposed time-based noise-coupling structure, both the order and bandwidth requirements of the loop filter are relaxed, and as a result, the analog complexity of the modulator is significantly reduced.

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KEY WORDS: asynchronous pulse width modulator; continuous-time sigma-delta modulators; noise-coupling; time-to-digital converter

1. INTRODUCTION

To realize wideband digital communication systems, low cost and low power analog-to-digital converters (ADCs) are needed. Sigma-delta modulators have attracted a lot of attention as a digital-friendly structure for ADCs because the substantial part of the signal processing is performed in digital domain. Continuous-time (CT) sigma-delta modulators are widely used to digitize the moderate to large bandwidth signals because of their efficient power consumption and silicon area [1]. However, the voltage headroom reduction in current CMOS technologies not only reduces the signal-to-noise ratio (SNR) but also deteriorates the effect of the nonlinear behavior of transistors, and thus, it reduces the dynamic range (DR) of voltage mode circuits [2].

Because of the finer time resolution of the advanced CMOS technology, the signal processing in time domain becomes increasingly beneficial [3, 4]. The increased switching speed of Metal-Oxide Semiconductor (MOS) transistors in modern technologies offers an excellent accuracy such that the time

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resolution of digital circuits has well overcome the problems of the voltage resolution in analog circuits. As a result, the time-based quantizers have emerged as a promising quantization architecture for CT sigma-delta modulators [5]. A major advantage of the signal processing in time domain (i.e., time-mode ADCs) is the digital-friendly nature of the system, which scales down with the technology.

Although open-loop time-mode ADCs can have short conversion time and lower power consumption, their performance is severely affected by the nonlinearity of the voltage-to-time converter (VTC), and as a result, the linearization techniques are essentially needed [6].

In contrast, the closed-loop structures employ the negative feedback to improve the performance. In [7], a closed-loop time-based sigma-delta modulator with a voltage-controlled oscillator (VCO) quantizer is designed for wideband applications in which the effect of the VCO nonlinearity and the harmonic tones are suppressed by the loop filter. Although the noise-shaping order is increased by one because of the VCO, the loop filter must provide most of the loop gain, which is needed to suppress the quantization noise, because the VCO gain is not sufficient.

As another example, in [8], a closed-loop CT sigma-delta modulator employing a synchronous ramp-based pulse-width modulator (PWM) as the VTC and a multi-bit time-to-digital converter (TDC) as the sampler is introduced. Although this structure provides some significant achievements, it suffers from several problems mainly arising from the combination of the synchronous PWM and the TDC. This combination causes the high frequency tones to fold back into the PWM spectrum. This way, the noise floor is significantly increased resulting in the modulator's signal-to-noise and distortion ratio (SNDR) degradation. The time-encoded structures in [9, 10] can also be categorized into wideband high performance PWM-based CT sigma-delta modulators. However, their sampling rates are in the order of multi-GHz resulting in significant power consumption in the quantizer.

In this paper, a CT sigma-delta modulator based on an asynchronous PWM (APWM) is proposed. The second-order noise-coupling is utilized to enhance the modulator's noise-shaping ability without affecting its signal transfer function (STF) and adding any integrator in the loop filter [11, 12]. An efficient realization of the noise-coupling technique in CT sigma-delta modulators is presented. A multi-bit double-sampled TDC, based on dual-edge triggered D-flip flops (DEDFF), is utilized to digitize the output signal of the APWM. The TDC is followed by a digital block named as digital-to-time converter (DTC). The combination of TDC and DTC can emulate the multi-bit digital-to-analog converter (DAC) operation by providing the time quantized feedback pulse without needing any multi-bit DAC. This brings a significant improvement in both area and power of a practical circuit.

The rest of the paper is organized as follows. An exchange of the conventional noise-coupled CT sigma-delta modulator to the proposed time-based noise-coupling structure with concentrating on the APWM as a VTC is explained in Section 2. The concept of the noise-coupling technique is elaborated in Section 3. The proposed time-based continuous-time sigma-delta modulator (TCSDM) with a second-order noise-transfer-function (NTF) enhancement is introduced in Section 4. Section 5 is devoted to the time-quantization and error approximation. System level simulation results of the proposed TCSDM are presented in Section 6. In Section 7, the circuit-level implementation of the proposed structure followed by the simulation results are provided. Finally, Section 8 concludes the paper.

2. PULSE-WIDTH MODULATION AS A VOLTAGE-TO-TIME CONVERSION

The principle core of the time-based sigma-delta modulators is the VTC. The VTC can be realized using VCOs [7], PWMs [13], or voltage controlled delay units (VCDUs) [14]. In the proposed structure, an APWM is utilized, which is described in more details in the following section.

Based on this VTC, the simplified block diagram showing the exchange of a conventional voltage-mode CT sigma-delta modulator to a time-based one is illustrated in Figure 1. Avoiding the use of multi-bit DACs in the feedback branch is one of the main targets of the time-encoding quantizers. To have a better understanding for this feature of time-encoded quantizers, we assume that the APWM has a carrier frequency of f_c and the sampling frequency is f_Q. It can be shown that the combination of an n-bit conventional quantizer with an n-bit DAC, which is sampled at the rate of f_c, can be replaced by an APWM whose output is oversampled by f_Q where $f_Q >> f_c$ [13]. As a

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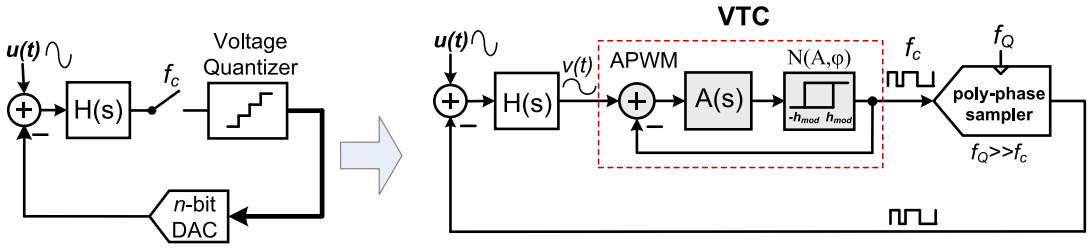

Figure 1. An exchange of the voltage-mode continuous-time sigma-delta modulator to the asynchronous pulse-width modulator (APWM)-based time-mode structure. VTC, voltage-to-time converter; DAC, digital-to-analog converter.

result of this concept, by choosing $f_Q = 2^n \times f_c$, the modulator equipped with a time-based quantizer can resolve the need of an n-bit DAC.

Another superiority of the time-based sigma-delta modulators is that the loop filter has to process the signals with the rate of f_c rather than f_Q where $f_c << f_Q$. This way, the speed requirements of the amplifiers used in the loop filter are relaxed, and thus, a significant reduction of the total power is obtained.

Although providing such a high sampling frequency as f_Q is a major challenge, this can be realized using an N-stage poly-phase sampling scheme [15]. This way, the rate of the sampling clock is reduced and it becomes f_Q/N. In this paper, an N-stage TDC is utilized to realize the poly-phase sampling block in order to reduce the clock frequency.

2.1. *Asynchronous pulse width modulator*

An APWM operates without a reference clock to avoid the quantization noise aliasing [16]. The self-oscillating behavior of the APWM resolves the need of an additional circuitry to create an external carrier, resulting in a compact circuit [17]. An APWM is consists of an integrator, a hysteretic comparator, and a negative feedback loop path. The output of the APWM is a continuous-time, discrete-amplitude signal without the quantization noise because the time is not quantized or sampled [15]. The oscillation frequency or the limit cycle denoted by f_c is the main design parameter to determine the spectral properties of the APWMs and the quality of the amplitude-to-time transformation [18].

Because the APWM is a nonlinear element due to the presence of a hysteresis, the self-oscillation conditions may be satisfied for a zero input. For a hysteresis comparator, the approximated transfer function using the describing function can be modeled as follows [19]:

$$N(A,\phi) = \frac{4D}{\pi A} e^{-j\sin^{-1}(h_1/A)} = \frac{4D}{\pi A}\sqrt{1-(h_1/A)^2} - j\frac{4Dh_1}{\pi A^2} \quad ; (A \geq h_1) \tag{1}$$

where h_1 is the hysteresis factor of the comparator, D is the level of the hysteresis window, and A is the amplitude of its input signal. Regarding an APWM loop as the feedback structure, the existence of a limit cycle oscillation is determined according to the gain-phase relation famed as Barkhausen's criteria. Assuming a first order $A(s)$ as $\omega_a/(s+\omega_a)$, the self-oscillation frequency is obtained as follows:

$$\omega_c = \frac{\omega_a\left(2+\sqrt{4-\pi^2 h_1^2}\right)}{\pi h_1} \approx \frac{4\omega_a}{\pi h_1} \tag{2}$$

For a sinusoidal input signal of $v(t) = A\sin(\omega t)$, the average instantaneous frequency denoted by f_0 can be stated as follows [16]:

$$f_0 = f_c\left(1-0.5A^2\right) \tag{3}$$

As it is clear, the value of f_0 varies as the amplitude of the APWM input. It can be easily shown that modifying the hysteresis factor as (4) can significantly reduce the carrier frequency fluctuation for large values of A:

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$$h_{\mathrm{mod}} = \left(1 - 0.5A_{\mathrm{max}}^2\right) h_1 \tag{4}$$

where h_{mod} is the modified hysteresis factor. By using h_{mod} as a hysteresis factor of the comparator, the value of f_0 becomes approximately equal to the free running frequency, f_c, namely $f_0 \approx f_c$. On the other hand, it is worth mentioning that by inserting the APWM inside the loop of the sigma-delta modulator (as it is the case in the proposed structure), the swing of the APWM input signal becomes small. In this condition, the approximation of $f_0 \approx f_c$ remains valid in the analysis.

3. NOISE-TRANSFER-FUNCTION ENHANCEMENT BY NOISE-COUPLING

The SNR of a sigma-delta modulator is improved if the order of the loop filter, $H(s)$, is increased. But this improvement is achieved at the expense of a lower stability. An NTF enhancement through the noise-coupling (NC) is another technique to increase the noise-shaping performance of a sigma-delta modulator. In this technique, the STF does not change, and the order of the loop filter remains the same. This enhancement is achieved by extracting the quantization error and then coupling its filtered version into the forward path of the modulator. The NTF of a noise-coupled sigma-delta modulator denoted as $\mathrm{NTF_{NC}}$, can be stated as follows [11]:

$$NTF_{\mathrm{NC}} = (1 - G(z))\, NTF \tag{5}$$

where $G(z)$ is the transfer function of a finite-impulse response (FIR) filter. The block diagram of the noise-coupling concept in conventional sigma-delta modulators is shown in Figure 2(a). Considering a simple delay block such as z^{-1} for $G(z)$, the NTF order is improved by one according to (5).

Unlike the realization of the noise-coupling technique in discrete-time (DT) sigma-delta modulators, it is not so straight forward to take the advantage of this idea in CT sigma-delta modulators owing to the difficulty in the analog subtractor implementation.

In [12], a discrete-time noise-coupling branch using a switched-capacitor circuit and a clocking scheme is utilized to realize the noise-coupling in the CT sigma-delta modulator. Although it is shown that the noise-coupling technique is properly realized, the introduced modulator is not a fully continuous-time because the noise-coupling branch utilizes a discrete-time active subtractor, which makes it an unsuitable choice for wideband and low power applications.

By applying the DT-to-CT conversion accompanied with some modifications on the structure in Figure 2(a), one can implement the first-order enhancement by using only passive filters [20]. Although a higher-order enhancement is also feasible, it requires positioning multiple zeros at DC to form the high-pass profile for the NTF. So, it cannot be implemented using only passive filters, and additional active filters are needed resulting in more power dissipation. It will be shown that by using an APWM as the VTC, not only the first-order NTF enhancement is feasible, the second-order noise-coupling is also realizable without needing any additional active filter. In the next section, this superiority of the proposed TCSDM is presented.

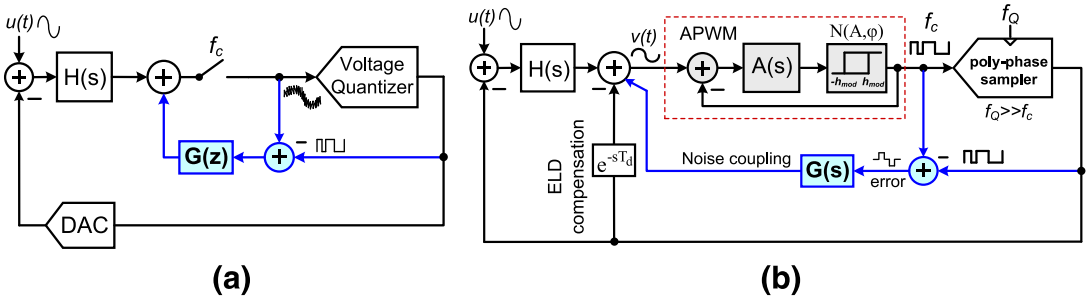

Figure 2. (a) Noise-coupling in conventional continuous-time sigma-delta modulator and (b) the conceptual illustration of the proposed noise-transfer-function-enhanced structure. APWM, asynchronous pulse-width modulator; DAC, digital-to-analog converter; ELD, excess loop delay.

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3.1. *Proposed noise-transfer-function-enhanced time-based continuous-time sigma-delta modulator*

The conceptual block diagram of the proposed TCSDM with the excess loop delay (ELD) compensation and noise-coupling branches is shown in Figure 2(b) where $G(s)$ is the CT equivalent of $G(z)$. The ELD increases the delay of the feedback path, and hence, it can degrade the modulator stability. This can be compensated by using a fast feedback path composed of a delay and gain block around the quantizer [21]. In Figure 2(b), the branch with a delay of e^{-sT_d} is applied for ELD compensation, where T_d mainly accounts for the total delay of the APWM and the sampler. Although the ELD in CT sigma-delta modulators has a negative effect on the stability and performance of the modulator, its compensation path can be used to simplify the modulator architecture and reduce the number of the feedback branches.

By using the APWM inherent summing node, the feedforward and internal feedback branches can be integrated at the input point of the APWM. This modification resolves the need of an extra subtractor or a summing amplifier. This way, the extended version of the proposed modulator is illustrated in Figure 3(a). By merging the blocks highlighted with dashed lines, the structure of the proposed modulator is simplified as shown in Figure 3(b). Although the appearance of the APWM is changed in this way, the oscillation condition of the APWM is still valid because the whole structure forces the loop to oscillate properly while applying the noise-coupling technique. Here, $G(s)$ will be approximated according to the transfer function of the FIR filter, $G(z)$. The approximated $G(s)$ can be implemented using only passive elements.

3.2. *First-order NTF enhancement*

According to (5), by assuming $G(z)=z^{-1}$, the order of the NTF is enhanced by one. As mentioned earlier, in the proposed TCSDM, the output of the loop filter is sampled by the rate, which is approximately equal to the oscillation frequency of the APWM, f_0 (i.e., $f_0 \approx f_c$). Hence, the CT counterpart of $G(z)=z^{-1}$ can be given as e^{-sT_0} where $T_0=1/f_0$ is the time delay equivalent associated with z^{-1}. According to the Taylor's series approximation of e^{-sT_0}, it can be shown that:

$$e^{-sT_0} = 1 - sT_0 + \frac{s^2T_0^2}{2} - \frac{s^3T_0^3}{6} + \ldots \quad ; \; s = j\omega \tag{6}$$

When $f << 1/T_0$, the relation (6) is simplified as follows:

$$e^{-sT_0} \approx \frac{1}{1+sT_0} \tag{7}$$

which indicates that $G(z)$ can be realized by a passive low-pass filter (LPF) in a CT counterpart. This approach is applicable if the time constant of the LPF has a negligible variation as the frequency of its input signal is changed. Otherwise, it is not an effective alternative to the FIR $G(z)$. Fortunately, owing to the oversampling phenomenon in sigma-delta modulators, the approximation of $f << 1/T_0$ is usually valid. By using this approximation, the feedback branch of the APWM, 1-$G(s)$, performs as a high-pass filter (HPF) with the following transfer function:

$$1 - G(s)_{NC1} = 1 - \frac{1}{1+sT_0} = \frac{s}{s+\omega_{p1}} \quad ; \; \omega_{p1} = 1/T_0 \tag{8}$$

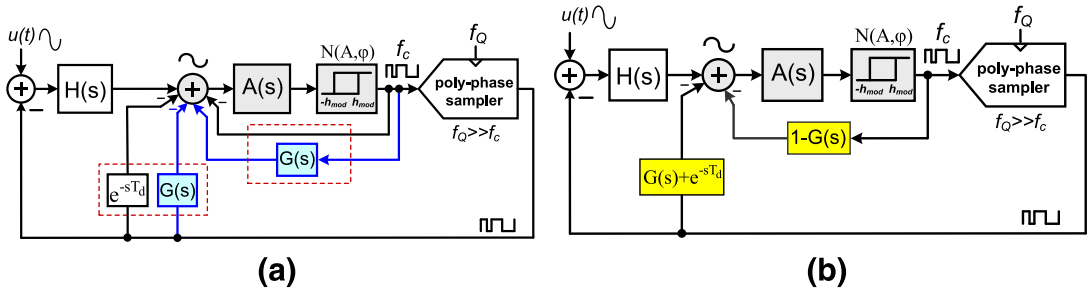

Figure 3. (a) Extended version of the noise-coupling time-based continous-time sigma-delta modulator (TCSDM) and (b) finalized block diagram of the noise-coupling concept in the proposed TCSDM.

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where NC_1 refers to the first-order noise-coupling. As mentioned previously, the delay of the ELD compensation path in Figure 3(b) is considered as T_0 (i.e., $T_0 \approx T_d$). Hence, the transfer function of the new ELD compensation path for the first-order noise-coupling can be calculated as follows:

$$e^{-sT_d} + G(s)_{NC1} = 2 \times \frac{\omega_{p1}}{s + \omega_{p1}} \quad ; \; T_d \approx T_0 \tag{9}$$

This indicates that the ELD compensation path is comprised of an LPF and a gain block. As the main target of this paper is the feasibility evaluation of the second-order NTF enhancement, the rest of the paper is devoted to the realization of this feature.

4. SECOND-ORDER NOISE-TRANSFER-FUNCTION ENHANCEMENT

In this section, the generalization of the previously mentioned NTF enhancement technique to the higher orders is studied. To do this, we will elaborate on the possibility of the second-order noise-coupling realization. As indicated before, the order of the NTF enhancement may not be so attractive in conventional noise-coupling structures because of the need of additional amplifiers. But we will show the effectiveness of this idea in the proposed modulator.

Considering Equation (5), to achieve the second-order NTF enhancement, we need to realize a second-order FIR, $G(z)$ as follows:

$$G(z)_{NC2} = 2z^{-1} - z^{-2} \tag{10}$$

According to the result of the previous section, we conclude that a first-order FIR, $G(z)$, can be approximated by an LPF in the CT counterpart. This way the CT equivalence of (10) can be given as follows:

$$G(s)_{NC2} = \frac{2}{1 + sT_0} - \left(\frac{1}{1 + sT_0}\right)^2 = \frac{1 + 2sT_0}{(1 + sT_0)^2} \tag{11}$$

Assuming $T_d \approx T_0$ for the ELD compensation path in Figure 3(b), the transfer function of this branch is calculated as follows:

$$e^{-sT_d} + G(s)_{NC2} = \frac{2 + 3sT_0}{(1 + sT_0)^2} \quad ; \; T_d \approx T_0 \tag{12}$$

The equation in (12) can be simplified without any significant loss of equivalency in phase and magnitude of the transfer function within the bandwidth of the modulator. This simplification may be written as follows:

$$\frac{2 + 3s/\omega_{p2}}{\left(1 + s/\omega_{p2}\right)^2} \approx \frac{3 - \alpha}{1 + s/\omega_{p2}} \quad ; \; \omega_{p2} = 1/T_0 \tag{13}$$

where α is a constant that is applied to further equalize the two functions within the desired bandwidth. This constant has a small value (i.e., $\alpha < 1$) and it can be determined through the simulations. This simplification is worth from the implementation point of view because the realization of the approximated transfer function is easy compared with the one in (12).

The feedback branch of the APWM in Figure 3(b) can also be obtained as follows:

$$1 - G(s)_{NC2} = \frac{s^2}{(s + 1/T_0)^2} = \frac{s^2}{\left(s + \omega_{p2}\right)^2} \tag{14}$$

This indicates that the feedback path of the APWM is a second-order HPF with two zeros at the origin and two real and identical poles at the left side of the $j\omega$-axis. The realization of this second-order HPF may be a major challenge. However, an effective method is introduced to implement it without using any additional hardware.

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4.1. *Realization of the second-order high-pass filter*

A simple way to implement a second-order HPF is to cascade two passive HPFs as $s/(s+\omega_{p2})$. However, the loading effect of these two stages makes the poles to significantly split from each other. So, such implementation for the HPF in (14) is not more feasible. On the other hand, cascading two first-order HPFs in the feedback branch of the APWM can significantly load the quantizer's output, and hence, disturb the oscillation condition of the APWM. Alternatively, an active second-order HPF can be used to realize the equation in (14).

The schematic of the active second-order HPF is shown in Figure 4(a). The transfer function of this filter is as follows:

$$\frac{V_{o1}(s)}{V_{i1}(s)} = -\frac{s^2}{(s+1/RC)^2} \tag{15}$$

As it is clear, the transfer function in (15) can successfully be a representative for the one in (14) if we assume $\omega_{p2}=1/RC$. But this realization needs two amplifiers resulting in more power consumption and design complexity. In order to avoid these two amplifiers, we must modify the transfer function of (14), because it is impossible to realize it without using the amplifiers. For this, we can slightly split the poles of the second-order HPF. In other words, if we replace the poles in $\omega_{p2}\pm\varepsilon$ ($\varepsilon<<\omega_{p2}$) rather than arranging both of them in ω_{p2}, we can obtain a degree of freedom to implement an alleviated second-order HPF. An implementation of the second-order HPF with new position of the poles is shown in Figure 4(b). The transfer function associated with this circuit is calculated as follows:

$$\frac{V_{o2}(s)}{V_{i2}(s)} = -\frac{s^2}{s^2\left(\frac{R_2}{R_2}\right)+s\left(\frac{1}{R_3C_2}+\frac{1}{R_3C_1}+\frac{R_2}{R_1R_3C_1}\right)+\frac{1}{R_1R_3C_1C_2}} \tag{16}$$

As it is clear, the transfer function has two zeros at the origin and two different poles, which can be matched with $\omega_{p2}+\varepsilon$ and ω_{p2}-ε with the proper selection of the elements value. Assuming $R_2=R_3$, we can write:

$$\begin{aligned}\frac{1}{R_1C_1}+\frac{1}{R_2C_1}+\frac{1}{R_2C_2} &= 2\omega_{p2}\\ \frac{1}{\sqrt{R_1R_2C_1C_2}} &= \sqrt{\omega_{p2}^2-\varepsilon^2}\end{aligned} \tag{17}$$

Now the target is to find the condition between the elements of the new HPF for which the equation (17) is valid. For this, we assume $R_1=\beta R_2$ and $C_1=\gamma C_2$ and rewrite (17) as:

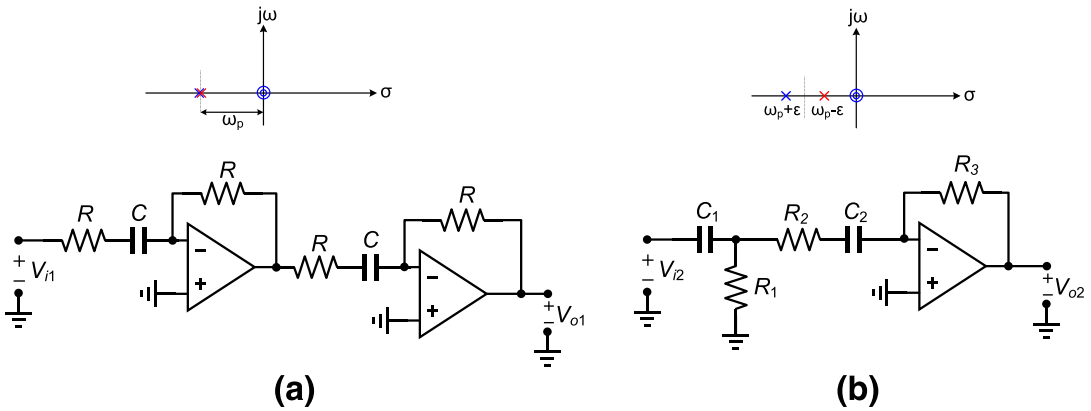

Figure 4. (a) Second-order active high-pass filter (HPF) and (b) the proposed second-order HPF.

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$$\frac{1+\beta+\beta\gamma}{\sqrt{\beta\gamma}} = K \tag{18}$$

where K is defined as

$$K = \frac{2\omega_{p2}}{\sqrt{\omega_{p2}^2 - \varepsilon^2}} \tag{19}$$

Regarding to the relations denoted in (17), we can write:

$$\beta^2\left(\gamma^2 + 2\gamma + 1\right) + \beta\left(2 + \left(1 - K^2\right)\gamma\right) + 1 = 0 \tag{20}$$

To solve (18), we should consider that β and γ are two positive constants. On the other hand, the equation in (20) should have two positive roots. Hence, the conditions for the validity of (17) are obtained as follows:

$$\begin{aligned} &\beta,\ \ \gamma > 0 \Rightarrow\ K > \sqrt{\frac{2+2\gamma}{\gamma}} \\ &\Delta \geq 0\ \ \Rightarrow\ \ \gamma > \frac{4}{K^2-4}\ \text{ and }\ K > 2 \end{aligned} \tag{21}$$

Although the new second-order HPF still needs an amplifier, it should be noted that this amplifier can be removed because the inherent summing node of the APWM can serve as an amplifier for this filter. In other words, the superiority of the proposed second-order noise-coupling based on an APWM is that the inherent amplifier of the APWM not only serves as the summing node to the ELD compensation and feedforward branches but also it can play the role of an amplifier to realize the second-order HPF. This way the second-order NTF enhancement concept is realized without needing any additional hardware.

4.2. Loop filter topology selection

The CT loop-filter, $H(s)$, which determines the order of the modulator, can be implemented using a chain of integrators with either feedback or feedforward compensation paths [22]. The feedforward architecture has the disadvantage that its closed-loop frequency response has a peaking at high frequencies because of the zeros in the signal path. In the feedback structure, which has L feedback paths, the frequency response is monotonic without any frequency peaking. Moreover, feedforward filters are the best solution when implementing low power modulators, because only one feedback path is needed, and hence, only one DAC is theoretically required. Therefore, the feedforward structure is selected in our proposed design. The transfer function of a feedforward structure is as follows:

$$H_{FF}(s) = \frac{I_1 k_1 s^{L-1} + I_1 I_2 k_2 s^{L-2} + \ldots + I_1 I_2 \ldots I_L k_L}{s^L} \tag{22}$$

where L is the filter order and I_i and k_i are the integrator gains and feedforward coefficients, respectively. The loop filter design is commonly performed in discrete-time domain by realizing the desired $H(z)$ as $NTF(z) = 1/(1+H(z))$ via the Delta-Sigma Toolbox provided by Schreier [23]. To achieve more noise-shaping, some of the NTF zeros are placed at the inband frequencies. The resulting resonator can be realized with two different topologies shown in Figure 5. The zero of both these resonators is the same but with different positions for the poles. The topology in Figure 5(a) represents a lossless resonator because its poles are spread exactly on the $j\omega$-axis. But the one in Figure 5(b) is not a good choice for an ideal resonator because it has a damping factor that moves the poles to the left side of the $j\omega$-axis, and thus, decreases the performance of the resonator. On the other hand, the local feedback of the damping resonator in Figure 5(b) is typically realized with a large resistor, which can directly affect the input-referred thermal noise. Hence, we discard the damping resonator and utilize the resonator in Figure 5(a) in our design.

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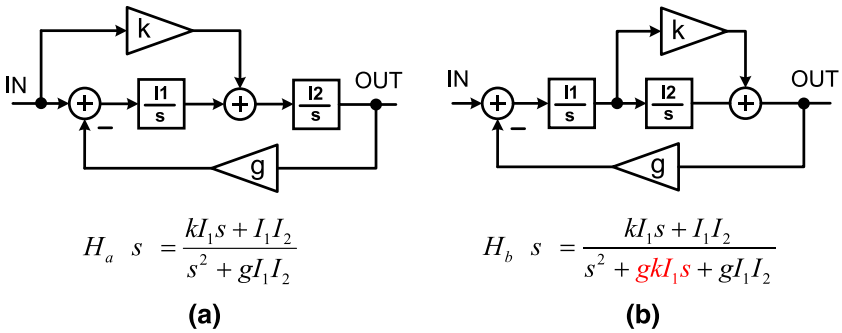

Figure 5. Two possible implementation of the second-order feedforward loop filter (a) without a damping factor and (b) with a damping factor.

4.3. Block diagram of the proposed time-based continuous-time sigma-delta modulator with second-order noise-coupling

To have a detailed view from the complete structure of the proposed TCSDM, a second-order modulator employing the second-order noise-coupling technique is illustrated in Figure 6. Although the order of the loop filter is two, the overall noise-shaping order is four because of the second-order noise-coupling.

The loop of the APWM oscillates properly if the Barkhausen's criteria is satisfied and also if the input signal is slower enough compared with its output signal, $p(t)$ [22]. It means that high frequency components in the two-level stream of the feedback signal should be attenuated before the summing node at the input of the APWM, otherwise the modulator becomes unstable. For this to be satisfied, a first-order passive LPF such as $k_f\omega_f/(s+\omega_f)$ is utilized in the main feedback path to filter out the high frequency components around the limit cycle frequency of $p_q(t)$. This filter can also improve the clock jitter immunity of the modulator [22]. The LPF in the feedback branch also converts the feedback signal waveform from a single-bit stream to a multi level one. This way, not only the instability problem is resolved but also the swing and slew rate requirements of the amplifiers are relaxed.

To realize the poly phase sampler, a combination of the TDC and DTC is utilized. The combination of TDC/DTC works as a combination of an ADC/DAC, thus resolving the need of a multi-bit DAC. This issue is more explained in the following section.

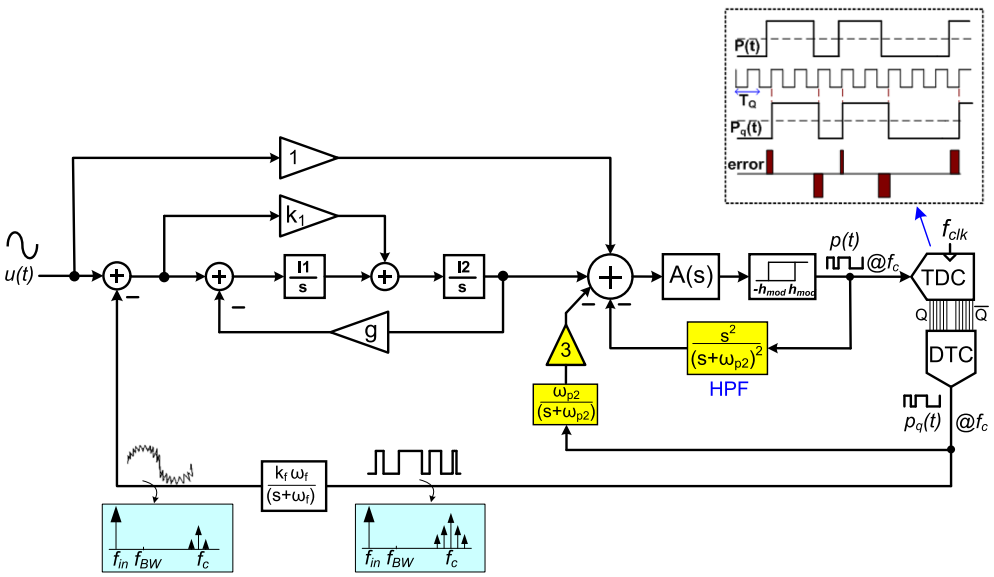

Figure 6. A block diagram of the proposed second-order time-based continuous-time sigma-delta modulator with the second-order noise-transfer-function enhancement. TDC, time-to-digital converter; HPF, high-pass filter; DTC, digital-to-time converter.

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5. TIME QUANTIZATION AND ERROR APPROXIMATION

5.1. Time quantization

Although the amplitude-to-time mapping of an APWM can be very accurate, the output may not be applicable for digital processing without the pulse quantization. In this paper, a multi-stage delay-line-based TDC is proposed to replace the poly phase sampler. The TDC quantizes the edges of the PWM signal and provides a 'time-quantized' feedback pulse. The quantization of the pulse width is required to ensure that the feedback signal corresponds to the quantized output code of the TDC, otherwise the noise-shaping concept may not be satisfied.

5.2. Time-to-digital converter/digital-to-time converter structure

A TDC is mostly composed of digital components such as inverters and latches, and hence, it can be benefited from the high speed and low power consumption of digital circuits [24]. In an N-level TDC, the combination of a delay line and N latches divide the phase of the input clock into N-1 similar parts and outputs a quantized version of the input pulse width [25]. The minimum value of the ratio of f_{clk}/f_c is critical both for the stability of the TCSDM and for the proper performance of the time quantization. To find this limit, we should find the smallest width associated with the APWM output pulse. It can be shown that the width of the APWM pulses can be calculated as follows:

$$W(t) = \frac{T_c}{2}\left(\frac{1}{1-\mathrm{v}(t)}\right) \tag{23}$$

where $W(t)$ is the width of the pulses. Regarding (23), the widths are changed within $T_c/4 < W < \infty$. As a result, the TDC sampling frequency should be $f_{clk} \geq 4f_c$, so that all PWM signal edges are properly detected. Thus, the sampling rate of the TDC may be undesirably high for high limit cycle frequencies according to $f_{clk} \geq 4f_c$. So, it is preferred to change the TDC structure in a way that the needed sampling clock is reduced. In the proposed TDC, all of the latches are based on DEDFFs. This way, a double-sampled TDC is realized and the minimum required sampling frequency is halved as $f_{clk} \geq 2f_c$. This results in alleviating the design constraints and also leads to the reduction of the power consumption.

As shown in Figure 7, the TDC outputs are recombined together to provide the single bit quantized feedback pulse using a DTC. The DTC is composed of two N-input OR gates and two resettable DFFs, which are asynchronously clocked by the output of two OR gates. Combining the TDC with a DTC can resolve the need of a multi-bit DAC. It should also be noted that an N-stage double-sampled TDC/DTC clocked at f_{clk} can be conceived as a mere DFF with a virtual sampling frequency of $f_Q = 2N \times f_{clk}$.

5.3. Time quantization error approximation

The APWM output signal is a lossless representation of its input, because the information is stored in the pulse width. However, the sampling in TDC will introduce an error even if the sampling frequency is higher than the Nyquist rate. The difference between the signals $p(t)$ and $p_q(t)$ is considered as the time quantization error. The average occurrence rate of this error is f_0 for a non-zero sinusoidal input signal. It is difficult to make an exact analysis of this error because of the redundancy of the pulse. But fortunately, this is not really necessary to find an exact mathematical formula for this purpose [15]. Assuming the error signal, $e(t)$, with an average rate of f_0, we can give a rough approximation of the double-sided power spectral density (PSD) of this error signal denoted by $S_e(f)$ as follows [15]:

$$S_e(f) \approx \frac{4}{3f_0}\left(\frac{f_0}{f_Q}\right)^2 \tag{24}$$

5.4. Signal-to-noise ratio calculation of the proposed time-based continous-time sigma-delta modulator

It is usual to approximate the SNR of CT sigma-delta modulators according to discrete-time counterparts using the impulse invariance transformation (IIT) [21]. The NTF of the discrete-time equivalent of an L^{th}-order sigma-delta modulator is $(1\text{-}z^{-1})^L$. As mentioned previously, the output

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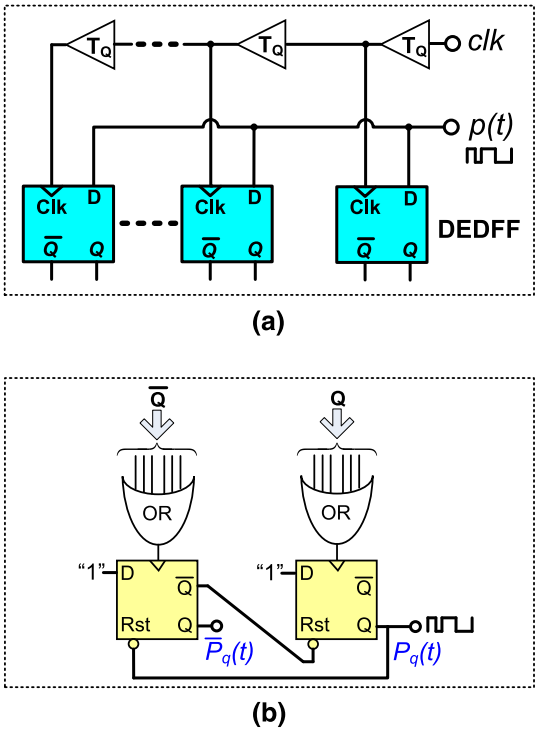

Figure 7. (a) The block diagram of the proposed dual-edge triggered D-flip flops (DEDFF)-based multi-stage time-to-digital coverter and (b) the proposed asynchronous digital-to-time converter.

signal of the loop filter is sampled at the rate of the APWM switching frequency rather than the clock frequency of the TDC. Hence, the power of the time quantization error of an L^{th}-order TCSDM within the bandwidth of f_B can be obtained as follows:

$$P_e = \int_{-f_B}^{f_B} S_e(f)|NTF(f)|^2\,df = \frac{8}{3}\times\frac{(2\pi)^{2L}}{2L+1}\times T_Q^2\times f_0^2\times\left(\frac{f_B}{f_0}\right)^{2L+1};\ |NTF(f)| = (2\pi f/f_0)^L \quad (25)$$

It is preferable to rewrite the equation (25) regarding the limit cycle frequency (f_c) rather than f_0. Assuming $f_0 \approx f_c$, which is valid for our design, the revised formula for SNR is achieved as follows:

$$SNR = \frac{3}{8}U_p^2\times\frac{2L+1}{\pi^{2L}}\times\left(\frac{f_Q}{f_c}\right)^2\times OCR^{2L+1},\quad OCR = f_c/2f_B \quad (26)$$

where U_p is the amplitude of the input signal and OCR is the over-cycling ratio.

On the other hand, the SNR of the proposed L^{th}-order TCSDM with the noise-coupling order of L_{NC} in which the resonator-based loop filter is utilized can be approximated as follows:

$$SNR_{NC} = \frac{3}{8}U_p^2\times\frac{2L_{eq}+1}{\pi^{2L_{eq}}}\times\left(L_{eq}-0.5\right)^2\times\left(\frac{f_Q}{f_c}\right)^2\times OCR^{2L_{eq}+1} \quad (27)$$

where $L_{eq} = L + L_{NC}$.

6. SYSTEM-LEVEL SIMULATION RESULTS OF THE PROPOSED TIME-BASED CONTINUOUS-TIME SIGMA-DELTA MODULATOR

6.1. Simulation assumptions of the proposed time-based continuous-time sigma-delta modulator

Behavioral simulations have been performed in MATLAB/SIMULINK to verify the performance of the proposed TCSDM in more details. In all of the simulation steps, the TDC is an N-stage

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delay-based structure with typical resolution of 80 psec for T_Q, which is defined based on the characteristic of a 90 nm CMOS technology [8]. The signal bandwidth of the modulator is chosen as 30 MHz, and also the loop filter structure is a feedforward topology. The validity of the noise-coupling technique is also elaborated via comparing the dynamic range of the NTF-enhanced TCSDMs with the non-enhanced second-order one. The results are depicted in Figure 8. The output spectrum for an input signal of −1.4 dBFS using the system level parameters summarized in Table I is illustrated in Figure 9. As expected, the spectrum and the dynamic range of the NTF-enhanced second-order TCSDM is improved. Furthermore, the expected slope of 80 dB/dec in the spectrum verifies the effective fourth-order noise-shaping.

To improve the dynamic range, one can reduce the TDC's resolution time. However, because of the technology limitations, it is not possible to decrease T_Q as much as desired. On the other hand, increasing the TDC number of stages can also be an improvement factor. However, the dynamic range enhancement with increasing the number of the TDC stages comes at the expense of the higher power consumption and larger silicon area.

Although increasing the value of f_c may improve the dynamic range, as mentioned previously, for the proposed TDC, the ratio of f_{clk}/f_c should be at least higher than two for the stability concern. This implies an upper limit to the switching frequency of the APWM. In a brief, the simulation results show that one can achieve the desired dynamic range by making a good compromise between the mentioned design parameters.

As a comparison of the proposed TCSDM with conventional voltage-based modulators, assuming the same clock as we used, the conventional modulator needs a loop filter of order $L=2$ with a 6.5-bit quantizer to achieve the DR of our proposed TCSDM. Quantifying the equivalent quantizer number of bits (n_{eq}) in the proposed modulator with using the feedback LPF for $L_{NC}=4$ is also possible. Assuming a conventional sigma-delta modulator with $L=4$, and OSR = 8 (the same as the OCR in the proposed TCSDM), the number of bits for the quantizer is equal to $n_{eq}=5.86$ bits for the achieved dynamic range. It should be noted that removing the feedback LPF in the proposed TCSDM makes the feedback signal to be a two-level stream rather than a multi-level one. This is the case in which the quantizer behaves as a single-bit quantizer. As mentioned earlier, this may

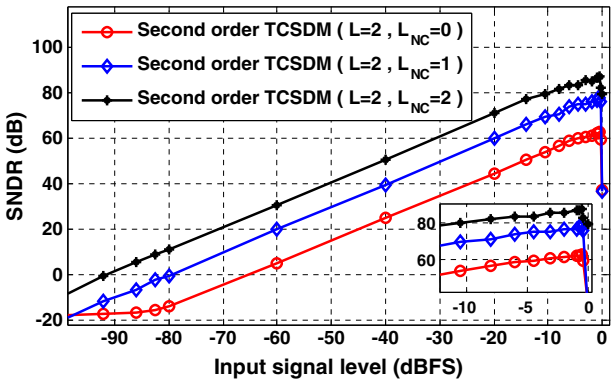

Figure 8. System-level simulation of the signal-to-noise and distortion ratio (SNDR) versus the input signal amplitude. TCSDM, time-based contiuous-time sigma-delta modulator.

Table I. TCSDM system level parameters for the simulation result in Figure 9.

Second-order TCSDM with $L_{NC}=2$ (system level)					
N	6	I_1	0.83 f_c	f_c (MHz)	450
g	0.1	I_2	1.71 f_c	f_{clk} (GHz)	1
α	0.12	k	1	ω_f (Mrad/s)	$2\pi\times50$
h	0.08	k_g	1.8	ω_a(Mrad/s)	$2\pi\times31$

TCSDM, time-based continuous-time sigma-delta modulator.

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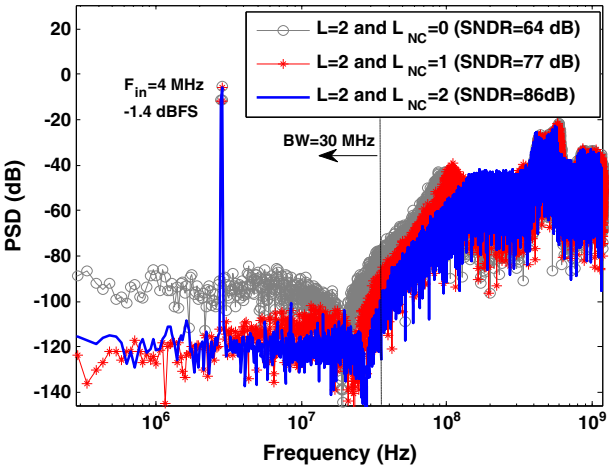

Figure 9. System-level simulation of different kinds of time-based continuous-time sigma-delta modulators. SNDR, signal-to-noise-and-distortion ratio; PSD, power spectral density; BW, bandwidth.

cause the modulator to be unstable. This brief comparison can clearly shows the superiority of the proposed TCSDM from the point of performance and hardware views.

As stated in (26) and (27), the modulator performance is enhanced when the limit cycle frequency, f_c, is increased. In this case, the clock frequency denoted as $f_{clk}=f_Q/N$ should also be increased to satisfy the Nyquist theorem. Unlike the voltage-based modulators where the clocks are applied to the high power dynamic comparators, in the proposed modulator, the clock signal is only injected to the fully digital DFFs. Digital DFFs are more power efficient than the dynamic comparators at higher speeds, namely, in the multi-GHz applications. Hence, a high speed clock signal can be utilized here with less concern in comparison with the conventional modulators.

On the other hand, unlike the voltage-based quantizers, the elements of the time-based quantizers can be implemented using digital circuits, offering a significant superiority from the point of speed, power dissipation, and programmability. Furthermore, thanks to the combination of the TDC and DTC, the feedback signal is a two-level single-bit stream while the output of the TDC is still multi-bit. Hence, any other technique such as the dynamic element matching (DEM) [26] is not needed for the DAC linearization unlike the conventional multi-bit sigma-delta modulators.

6.2. *Delay variation of noise-coupling and excess loop delay compensation paths*

As discussed earlier, one of the most important parameters that can degrade the modulator performance is the ELD. The main contribution of the ELD comes from the propagation delay in the TDC digital logic, the excess phase of the loop filter, and mainly from the APWM, which is the most dominant one.

Considering the ELD, the loop filter should be redesigned to achieve a stable modulator. This requires an additional feedback path around the quantizer to ensure the controllability of the structure [21]. As previously described, the delay blocks in the ELD and noise-coupling branches are implemented using passive elements, which their time constants are defined with *RC*-product. The value of these *RC*-products may be altered due to the various reasons (e.g. the process, temperature, and power supply variations). The effect of this delay variation (normalized to T_0) on the proposed modulator performance is shown in Figure 10. As it is clear, the degradation of the SNDR is negligible for an acceptable period of the delay variation confirming the robustness of the proposed structure.

6.3. *Clock jitter*

The clock jitter error can degrade the performance of the CT sigma-delta modulators. This error can be modeled as a random Gaussian noise with a variance of $\sigma^2_{\Delta t}$ [21]. For a non-return-to-zero (NRZ) DAC, if the SNR is completely limited by the white jitter noise rather than the shaped quantization noise, the signal-to-jitter noise ratio (SNR_j) can be obtained as follows:

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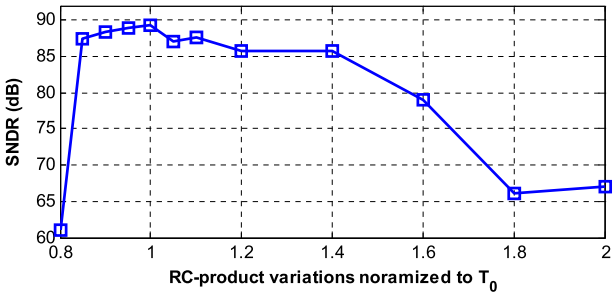

Figure 10. Signal-to-noise and distortion ratio (SNDR) versus the *RC*-product variations of the excess loop delay and noise-coupling paths.

$$SNR_j = 10\log\frac{OSR\times U_p^2/2}{\sigma^2_{\Delta t_N}\times\sigma^2_{\Delta y}} \tag{28}$$

where $\sigma^2_{\Delta y}$ represents the variation of the DAC output at every clock cycle. However, this relation is calculated for conventional voltage-based quantizers.

But, in the proposed architecture, where the TDC-based quantizer is utilized, the result may be different. Because the TDC outputs are merged by a DTC, some jitter rejection may be expected. In other words, because both the rising and falling edges of the feedback pulse denoted as $p_q(t)$ carry approximately the same time shift because of the clock jitter within a clock period, the clock jitter affects only the position of the feedback pulse and the pulse width remains approximately unchanged. On the other hand, because the pulse width in the proposed structure is generated asynchronously, the variation of the clock signal due to the jitter noise does not have a significant effect on the performance. Furthermore, the probable errors in the clock signal can be shaped since the TDC is located inside the modulator's loop.

However, the variations of the pulse width in the feedback signal ($p_q(t)$) can be seen as a clock jitter on the feedback DAC. Although the effect of random pulse position modulation of a PWM waveform is cumbersome to analyze with equations, the necessary insight can be achieved through simulations [8]. The SNDR limitation due to the jitter noise in the feedback pulse, using the model introduced in [27], is plotted in Figure 11. Here, the jitter noise on $p_q(t)$ is modeled as an additive Gaussian white noise.

An acceptable robustness of the SNDR variation across the jitter noise in the proposed TCSDM compared with the conventional CT sigma-delta modulators such as [21] is achieved thanks to the invariance of the pulse width in the presence of clock jitter and also because of the utilization of an LPF in the universal feedback path of the modulator.

6.4. Anti-aliasing behavior

In CT sigma-delta modulators, the continuous-time loop filter acts as an anti-aliasing filter [22]. According to the Nyquist theorem, the spectrum content of the loop filter output, around multiples

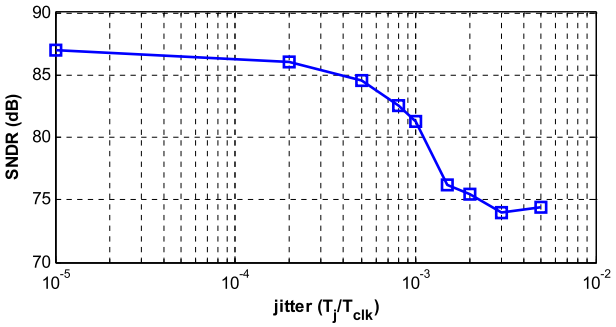

Figure 11. Signal-to-noise-and-distortion ratio (SNDR) versus the jitter noise in the feedback pulse.

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of f_{clk} and within the band of $[f_{clk}-f_B, f_{clk}+f_B]$, folds back to the low frequencies, and hence, increases the inband quantization noise.

The inherent anti-aliasing characteristic of the CT sigma-delta modulato, suppresses these folded components. As shown in Figure 6, the structure utilizes an overall feedforward path in order to relax the requirements on the loop filter and also to reduce the peaking in the signal transfer function. Although it may seem that this feedforward branch can degrade the anti-aliasing feature of the modulator, the anti-aliasing behavior is still acceptable as well. This is mainly, because of the existence of an LPF inside the APWM and in the universal feedback branch, and also because of the asynchronous nature of the pulse generation. The simulation result shown in Figure 12, with an anti-aliasing rejection (AAR) of 92 dB, confirms the sufficient rejection ratio of the aliased frequencies.

7. CIRCUIT-LEVEL IMPLEMENTATION OF THE PROPOSED TIME-BASED CONTINUOUS-TIME SIGMA-DELTA MODULATOR

The circuit level implementation of the proposed TCSDM is shown in Figure 13. The simulated design parameters are given in Table II. The utilized technology is TSMC 90 nm CMOS with 1 V power supply. It incorporates a second-order feedforward loop filter implemented using active-RC integrators with the topology shown in Figure 5.

The Operational Transconductance Amplifier (OTAs) used in the first and second integrators are designed to achieve a DC gain and unity-gain bandwidth (UGBW) about 40 dB and 1 GHz, respectively. However, the amplifier required for the summing node doesn't need a high gain, but its UGBW should be at least five times the limit cycle frequency because it is located inside the ELD compensation loop. Besides, a high swing amplifier is needed for the summing node. Hence, a Miller-compensated two-stage OTA is applied for the summing node. Although single-stage amplifiers such as the folded-cascode can be utilized for the loop filter integrators, two-stage OTAs are proffered in order to reduce the design complexity. On the other hand, because the feedback branches are passed through the low-pass filters, thus, the feedback signals are to some extent multi-level waves. This way, the slew rate of the OTAs is not a critical problem. The schematics of the amplifiers and also the common-mode feedback (CMFB) circuit are shown in Figure 14.

The hysteretic quantizer, used for providing the sufficient delay for the oscillation of the APWM, is shown in Figure 15. It is a cross-coupled quantizer with a positive feedback and the internal hysteresis is tuned by the proper sizing of the transistors' channel widths.

The proposed 6-stage TDC, which utilizes a novel implementation of the DEDFF, is depicted in Figure 16(a). The clock phases of the DEDFFs are generated using cascaded CMOS inverters. The

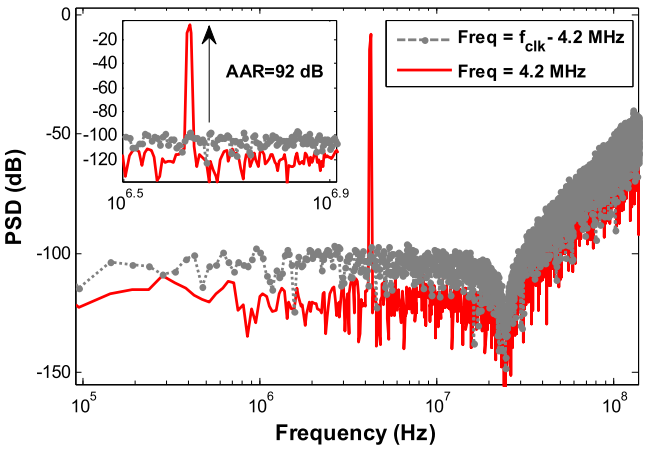

Figure 12. Output spectrum of the proposed time-based continuous-time sigma-delta modulator with −1.4 dB input at 4.2 MHz and at (f_{clk}-4.2 MHz). (All of the amplifiers are considered as non-ideal). PSD, power spectral density; AAR, anti-aliasing rejection.

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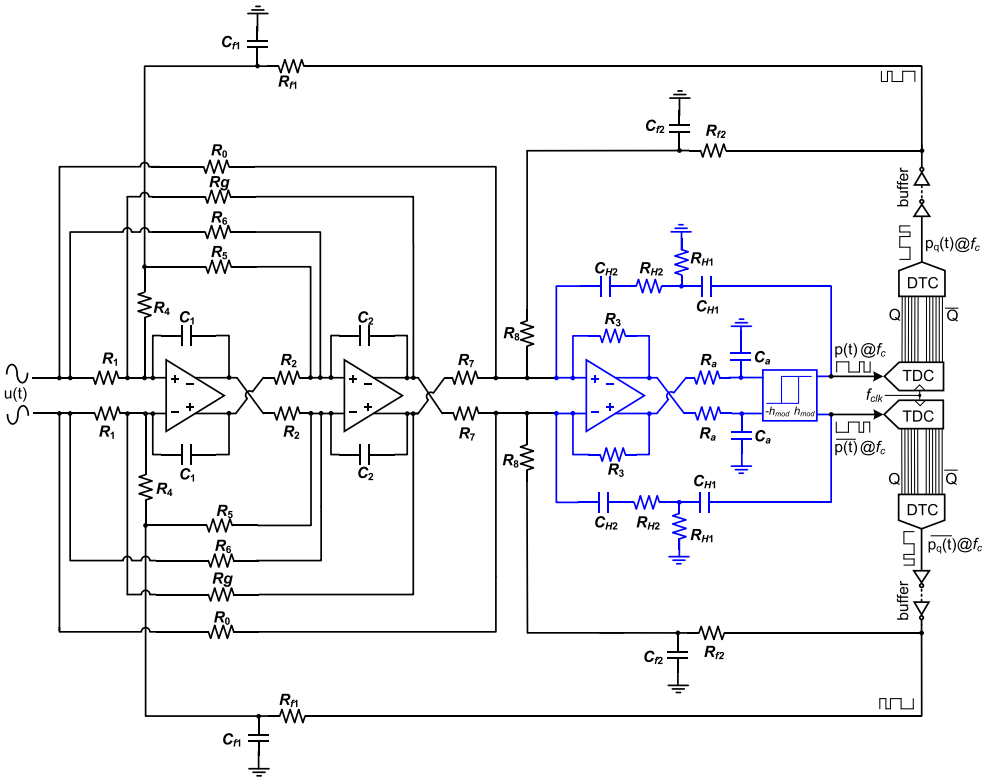

Figure 13. Fully-differential implementation of the proposed time-based continuous-time sigma-delta modulator with $L_{NC} = 2$. DTC, digital-to-time converter; TDC, time-to-digital converter.

Table II. Design parameters of the circuit-level implementation.

Second-order TCSDM with $L_{NC} = 2$ (circuit-level)							
$R_{1,2,6}$	1.5 kΩ	R_{f1}	250 Ω	C_1	1.4 pF	C_{H2}	200 fF
$R_{0,7,3}$	15 kΩ	R_{f2}	1.1 kΩ	C_2	1 pF	C_a	275 fF
$R_{4,5}$	0.9 kΩ	R_{H1}	600 Ω	C_{f1}	14 pF	k_g	2.4
R_8	5 kΩ	R_{H2}	15 kΩ	C_{f2}	2.54 pF	g	0.1
R_g	40 kΩ	R_a	5 kΩ	C_{H1}	4 pF	h	0.07

TCSDM, time-based continuous-time sigma-delta modulator.

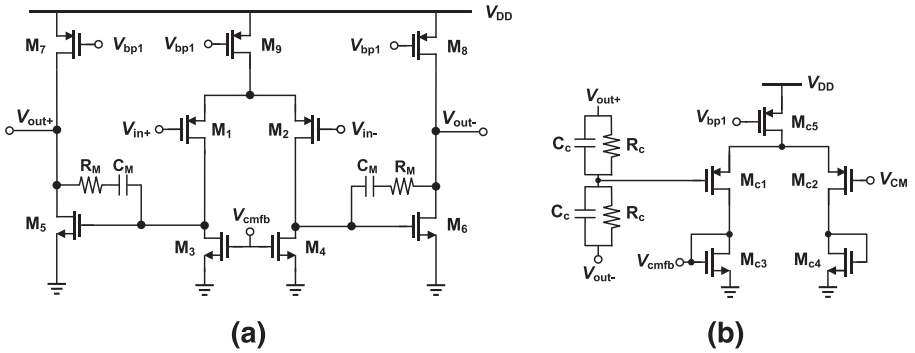

Figure 14. (a) Simulated two-stage OTA and (b) the schematic of the common-mode feedback (CMFB) circuit.

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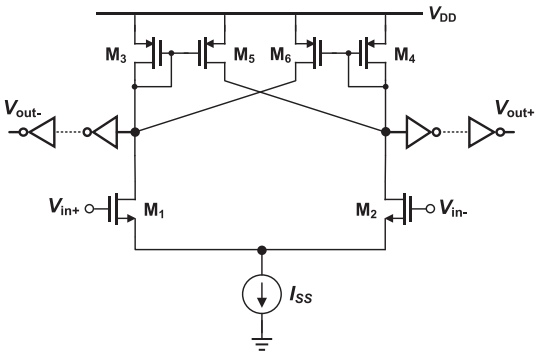

Figure 15. Hysteretic quantizer.

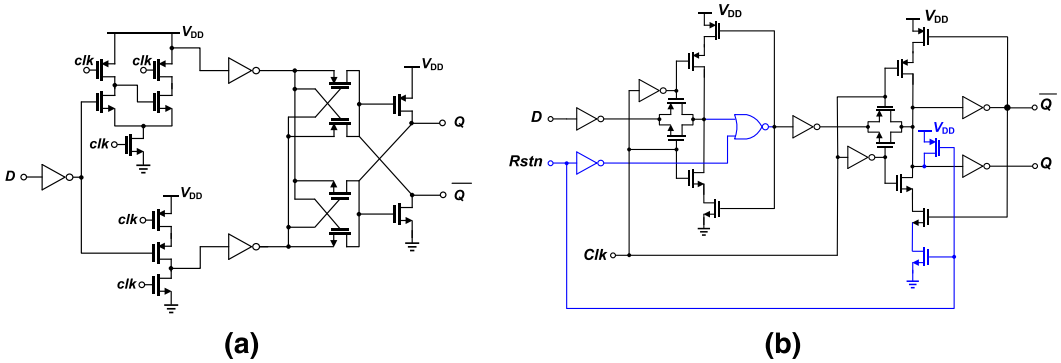

Figure 16. (a) Proposed dual-edge triggered D-flip flops and (b) the DFF of the digital-to-time converter with an asynchronous reset input.

proposed DEDFF is based on true-single-phase-clocked logic. It is composed of two latches, which their outputs are merged by a pass transistor logic XOR gate to be able to detect both the rising and falling edges of the APWM output pulse, $p(t)$. Compared with the 50-stage TDC utilized in [8], the proposed TCSDM requires much less TDC quantization levels making it more beneficial from the points of power consumption and design complexity.

The DFFs included in the DTC logic with an asynchronous reset input is also shown in Figure 16(b). The six-input OR gates in the DTC block are implemented using two-level *NOR-NAND* structure to achieve a small delay [28].

7.1. Circuit-level simulation results

Transistor level simulations in different process corner cases and temperature variations are performed to further verify the effectiveness of the proposed structure. The simulation result in Figure 17 shows an acceptable degree of the modulator robustness in different conditions. As is shown, a dynamic range greater than 84 dB in a 30-MHz bandwidth can be achieved in the typical-typical (TT) process corner case. The spectrum of the modulator with a 4.35 MHz, −2.6 dBFS input signal is shown in Figure 18. Taking into account the circuit noise of the modulator with integrating its power within the desired bandwidth, a loss of approximately 3 ~ 4 dB is incorporated in the previously defined SNDR values.

The robustness of the quantizer hysteresis factor against the process and mismatch variations is evaluated through extensive circuit level Monte Carlo simulations. The result is shown in Figure 19 where the histogram of the hysteresis factor is illustrated in Figure 19(a) for 1000 iterations in which both process and local variations of the device parameters were taken into account. The modulator SNDR across the variation of the comparator hysteresis factor for a −4 dBFS input signal is also

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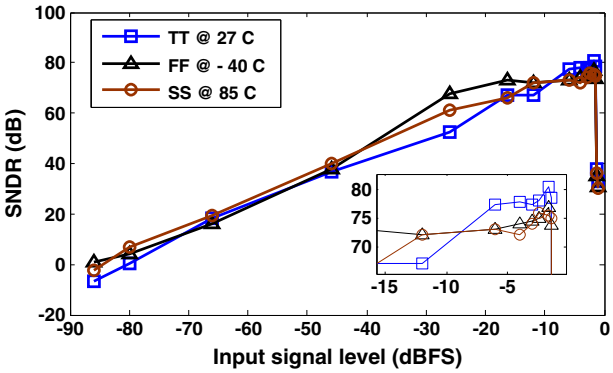

Figure 17. Circuit-level simulated signal-to-noise and distortion ratio (SNDR) versus the input signal amplitude in different process corner cases.

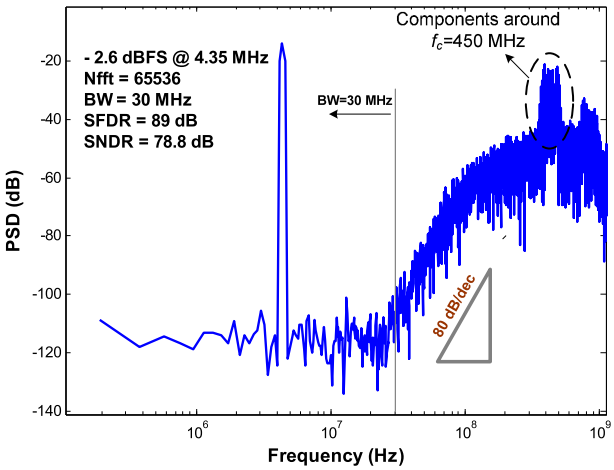

Figure 18. Circuit-level power spectral density (PSD) simulation of the proposed time-based continuous-time sigma-delta modulator (TT @ 27 °C). BW, bandwidth; SFDR, spurious-free dynamic range; SNDR, signal-to-noise and distortion ratio.

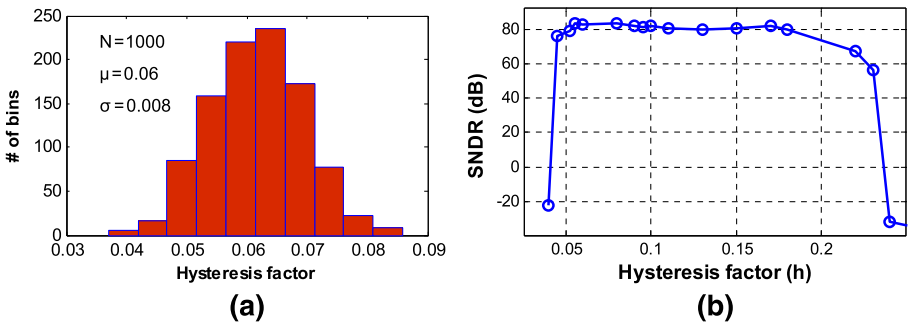

Figure 19. (a) Monte Carlo simulation results of the hysteretic quantizer and (b) signal-to-noise and distortion modulator (SNDR) versus the variation of the comparator hysteresis factor (@ −4 dBFS input signal).

illustrated in Figure 19(b). As it is seen, the proposed structure is more tolerant to the process variations of quantizer delay, and the performance degradation is negligible.

Table III summarizes the simulated performance of the proposed TCSDM. The estimation of the TDC/DTC power consumption is given as the digital power of the modulator for comparison

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Table III. Summary of the circuit-level simulated performance.

Type	Time-quantized CT-ΣΔM	
Loop filter order	2	
Noise-shaping order	4	
f_c	450 MHz	
f_{clk}	1 GHz	
N-TDC	6	
BW	30 MHz	
OCR (f_c/2*BW)	8	
Peak SNDR	Excluding circuit noise	80 dB
	Including circuit noise	77.2 dB
DR	84 dB (TT @ 27 °C)	
Technology	TSMC 90 nm CMOS	
Supply voltage	1 V	
Analog power	23 mW	
Digital power	3 mW	
FoM (P/(2*BW*2^{ENOB}))	72 fJ/conv-step	

CT, contiuous time; TDC, time-to-digital converter; BW, bandwith; OCR, over-cycling ratio; SNDR, signal-to-noise and distortion ratio; DR, dynamic range; CMOS, complementary metal-oxide semiconductor; TSMC, Taiwan Semiconductor Manufacturing Company; TT, typical-typical; FoM, figure-of-merit.

Table IV. Performance comparison of the proposed ΣΔM with several recently reported alternatives.

Parameter	[30] TCAS-I'07	[31] AICSP'08	[32] MWSCAS'10	[33] EDSSC'14	[34] FTFC'14	[35] MWSCAS'14	This work
SNDR (dB)	66	70	82	83	50	43	80
BW (MHz)	10	25	10	2	2	10	30
Power (mW)	7.5	16.4	36.1	10	0.75	17.3	26
Output rate (MHz)	640	800	320	128	100	1000	450
Technology (nm)	180	90	180	180	65	350	90
Supply voltage (V)	1.8	1	1.8	1.8	0.75	3.3	1
FoM (fJ/conv.step)	110	69	177	216	581	546	72

SNDR, signal-to-noise and distortion ratio; BW, bandwidth; FoM, figure-of-merit.

purposes. The modulator reported in [8] consumes almost 11 mW for a clock rate as small as 250 MHz. If the clock rate in [8] would be a higher one (such as 1 GHz in [29]), the total power consumption becomes significantly large. This is mainly because of the higher number of the TDC stages. Thus, decreasing the number of the TDC stages should be taken into account for the modulator with a high clock rate. The novel implementation of the proposed TDC/DTC makes it possible to reduce the digital power consumption for a 1 GHz clock rate, as shown in Table III.

In Table IV, the simulated performance of the proposed modulator is compared with some other works. Because the performance of the proposed modulator is verified through the circuit-level simulations rather than the measurement results, in order to provide a fair comparison, only the simulation-based works are reported in this table. The reasonable figure-of-merit (FoM) of the proposed structure under the various corner cases and temperature variations confirms its performance as a good candidate for broadband and low-voltage applications.

8. CONCLUSIONS

In this paper, an NTF-enhanced continuous-time sigma-delta modulator using a digital friendly time-based approach is presented. The proposed TCSDM leverages an APWM as the VTC and a TDC as the time quantizer. A combination of the TDC with a DTC gives the possibility of avoiding the

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multi-bit DAC. A novel realization of the second-order noise-coupling technique using passive elements is introduced to enhance the noise-shaping order of the modulator by two, without adding a significant hardware. Furthermore, by combining the TDC and DTC, the robustness of the proposed modulator against the clock jitter is improved because of the invariance of the feedback pulse widths. Simulation results performed in both system and circuit levels confirm the effectiveness of the proposed NTF-enhanced TCSDM.

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