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Time-Mode Signal Quantization for Use in Sigma-Delta Modulators

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ABSTRACT

The rapid scaling in modern CMOS technology has motivated the researchers to design new analog-to-digital converter (ADC) architectures that can properly work in lower supply voltage. An exchanging the data quantization procedure from the amplitude to the time domain, can be a promising alternative well adapt with the technology scaling. This paper is going to review the recent development in time-based noise-shaping ADCs, so-called as time-based sigma-delta modulators. Two of the most important architectures named as voltage-controlled oscillator (VCO) -based and time-to-digital (TDC) -based sigma-delta modulators (SDMs) are selected to be reviewed in this paper. The intrinsic advantages and limitations of these structures are briefly explored. To confirm the effectiveness of the time-mode sigma-delta modulators, a TDC-based continuous-time sigma-delta modulator is proposed as an example and the related simulation results performed in MATLAB are illustrated. The simulation results show that the proposed modulator achieves a dynamic range of 67 dB over 30 MHz with the loop filter of order 2. The proposed TDC-based sigma-delta modulator shows the superiority of the time quantization approach in designing the wideband and less complex continuous-time SDMs.

KEYWORDS

Sigma-delta modulator, TDC, Time-based circuits, VCO.

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1- INTRODUCTION

The advance of CMOS technologies has resulted in restricting the voltage headroom of the circuits. As a consequence, the performance of voltage-based mixed-mode circuits scales poorly with technology. Nevertheless, the scaling, has led to the significant improvement in the time accuracy of digital circuits. In the time mode approach the analog variables are represented by the time information rather than the nodal voltages or branch currents. Improvement of the time accuracy, due to the technology scaling offers an attractive and technology-friendly alternative for conventional amplitude-mode signal processing. Analog-to-digital converters (ADCs) are the key components of mixed-mode systems which can be benefited from this superiority [1].

Time-mode circuits possess a number of intrinsic characteristics that are scaled well with CMOS technology, making them a promising and viable option to implement some of the key building blocks of mixed analog-digital subsystems such as ADCs and Phase-Locked Loops (PLLs). Among the time-based ADCs, time-to-digital converter (TDC) and voltage-controlled-oscillator (VCO) -based ADCs have emerged as attractive solutions due to their highly digital intensive circuit architecture [2].

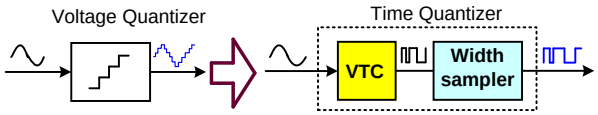

Fig.1. Transformation of the quantization from voltage domain to the time domain.

Sigma-delta modulators (SDMs) have attracted a lot of attention as a digital friendly structure for ADCs because the substantial part of the signal processing is performed in digital domain [3, 4]. By using the time-based signal processing approach, the shortcomings (i.e., higher power consumption, higher mismatches and etc.) related to the key component of the sigma-delta modulators can be significantly resolved. As is shown in Fig. 1, in the time-mode signal processing, an input voltage or the current is converted to a time variable using a voltage-to-time converter (VTC). The VTC can be realized using VCOs [5], PWMs [6], or voltage controlled delay units (VCDUs) [1]. The resultant time variable is then quantized using a width sampler such as time-to-digital converter (TDC) or a counter.

Architecturally, time-mode ADCs can be classified into the open-loop and closed-loop structures. Although the open loop time-mode ADCs can have short conversion time and lower power consumption, however, their performance is severely affected by the nonlinearity of the VTC and non-ideality of the sampler. In contrast, the closed-loop topology employs the negative feedback to improve the performance of the ADC.

Iwata et al. [7] showed that an input voltage can be multi-bit quantized using a multi-stage voltage-controlled ring oscillator in series with a counter. The TDC-based sigma-delta modulator is another type of time-mode ADCs. In this structure, the conventional quantizer is realized with the combination of a VTC and a multi-bit TDC. The TDC produces the digitized version of the pulse width. Unlike the VCO-based quantizers, where the inherent first order noise shaping is obtained without any feedback, the TDC-based quantizers do not have this feature. Thus, it is not usual to utilize the TDC-base quantizer in an open structure unless the lower resolution is needed.

This paper is organized as follows. In Sect. 2 an overview of the VCO-based quantizer is provided with highlighting their most important features. In Sect.3, TDC-based quantizer is introduced. A table for the sake of the comparison of several time-based ADCs is presented in this section. As a design example a TDC-based continuous-time sigma-delta modulator is proposed in Sect. 4, to show the effectiveness of the time quantization approach. Finally, Sect. 5 concludes the paper.

2- VCO-BASED QUANTIZATION

Integrators are the basic building blocks of the sigma-delta modulators and are usually designed using operational amplifiers (op-amps). Op-amps have design challenges that are becoming more severe with process scaling. VCOs inherently integrate their frequency in the form of an output phase. This represents an attractive alternative to op-amp-based integrators [8]. In a VCO, the frequency deviation from the oscillator's center frequency is proportional to the input, and hence, the phase deviation is proportional to the integral of the input. This way, the data is transferred from the voltage to the width of the VCO output pulses. The pulse width can be quantized by counting the number of its zero crossings. Generally, VCO-based ADCs are categorized into two groups. First is the phase-mode and the other is the frequency-mode VCO-based ADC. In the former, the VCO output pulses are digitized using a multi-bit counter while in the later, a chain of DFFs is applied for this target. As a comparison, frequency-mode VCO-based ADC offers a speed advantage due to the absence of counters. However, in the case of phase-mode, the

counter clock rate can be lower than the VCO maximum frequency in the event that, the criteria f_s>2*f_{max} should be satisfied in the frequency-mode VCO-based ADC. The phase-mode block diagram of the VCO-based ADC followed by its linearized model is illustrated in Fig. 2. Since the phase of the VCO is ideally proportional to its control voltage, the number of the cycles of the VCO in one sampling period T_s yields the digital representation of the sampled input voltage. Also, the frequency-mode one is shown in Fig. 3. As is clear, The VCO-based ADC typically consists of a sample-and-hold (S/H), a multi-stage ring VCO (RVCO), and a digitizer. The input is sampled and held by the S/H block and used to control the VCO.

Regarding that the VCO can be linearly modeled as an integrator [8], it can be shown that the output signal of phase-mode VCO-based ADC representing in z-domain is:

$$D_{out}(z)=\frac{1}{2\pi}[K_{VCO}V_{in}(z)+(1-z^{-1})E(z)] \qquad (1)$$

where V_{in} is the input signal, $E(z)$ is the z-transform of the error signal and K_{vco} is the conversion gain of the VCO.

Identical to the phase-mode one, the output signal of the frequency-mode VCO-based ADC can be stated as:

$$D_{out}(z)=K_{VCO}V_{in}(z)+(1-z^{-1})E(z) \qquad (2)$$

The form of the output signal in (1) and (2) reveals that the quantization noise, $E(z)$, is high-pass filtered and thus the first-order noise shaping is achieved. Thus this ADC can be classified as a sigma-delta modulator. It is worth noting that this superiority is obtained without any feedback loop or an extra amplifier. The equivalent number of the bits associated with the VCO-based sigma-delta modulator can be calculated from [9]:

$$n_{bit}=\log_2\left(\frac{N_{ph}\,f_{tune}}{f_s}\right) \qquad (3)$$

where f_{tune} is the frequency tuning range of the VCO, and N_{ph} is the number of the phases of the VCO which are involved in the quantization process. From (3) and according to the linear model, the SNR of the VCO-based can be derived as [9]:

$$SNR^{dB}=20\log\left(\frac{f_{tune}\,N_{ph}}{f_s}\right)+30\log(OSR)-3.41 \qquad (4)$$

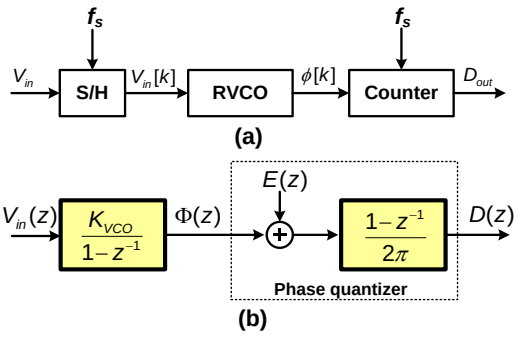

Fig. 2. Phase-mode VCO-based ADC, (a) the block diagram, (b) its linearized z-domain model [2].

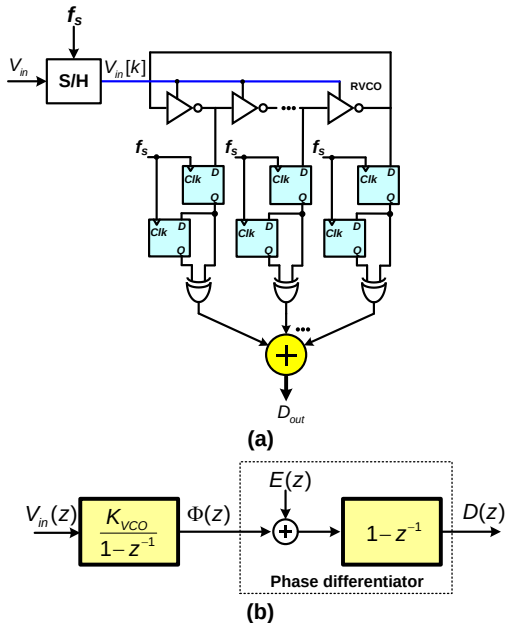

Fig. 3. Frequency-mode VCO-based ADC, (a) the block diagram,(b) its linearized model [7].

where, OSR is the oversampling ratio and is defined as $f_s/2f_{BW}$ and f_{BW} is the signal bandwidth. It implies that, as the number of the VCO phases increases (i.e., the multi-phase VCO-based ADC) the resolution of the modulator is enhanced.

This feature is more clarified through the system-level simulation of the modulator for two different cases (N_{ph}=1 and N_{ph}=5) as shown in Fig. 4. In this simulation, a differential frequency-mode VCO-based ADC is selected as a case study. The input signal is a sinusoidal one with an amplitude of 0.1 V, the sampling frequency is f_s=1 GHz and the K_{VCO}=1.5 GHz/V while the VCO center frequency is chosen as f_0=300 MHz.

Since the frequency of ring VCOs scales well with technology, the sampling frequency of VCO quantizers

can be made sufficiently large. As a result, large OSRs can be considered for these ADCs.

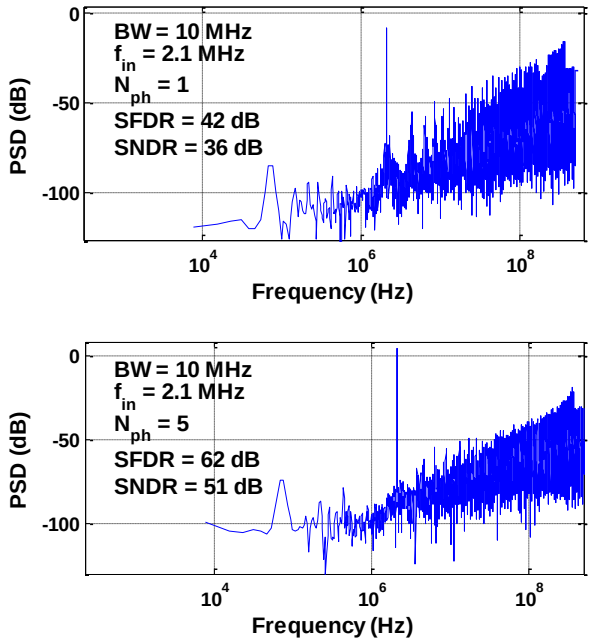

Fig. 4. Simulation results of a VCO-based ADC for the input signal amplitude of 0.1 V.

However, the performance of the VCO-based ADC is deteriorated by the nonlinear voltage-to-phase characteristic of the VCO. This adverse effect gets more severe when the variation of the input voltage is large. An intensive effort has been introduced in compensating this bottleneck while preserving the positive features of the VCO-based quantizers.

In [10], a VCO-based multi-bit quantizer is employed inside a continuous-time ΔΣ loop. This design partially solves the nonlinearity error of the VCO while generating implicit dynamic element matching of the feedback digital-to-analog converter (DAC) elements. Although the feedback loop serves to suppress VCO nonlinearity and phase noise, the signal-to-noise-plus distortion ratio (SNDR) of the overall ADC is still limited by VCO nonlinearity. In [11], a VCO-based quantizer is used along with a feedback DAC to linearize the VCO by reducing its input swing. In [12], four VCOs are used along with digital calibration to reduce the effects of VCO nonlinearity. The approach proposed in [13], the pulse width modulation (PWM) prior to the VCO forces the VCO to toggle between two frequencies, f_{low} and f_{high}. This way, the VCO operates linearly to improve the overall SNDR of the ADC. However, the nonlinearity of the PWM block can be a new problem needs to be cared. In [14], a multi-rated multi-stage structure for the sigma-delta modulator is proposed where the first stage is a conventional first order modulator, while the second stage is a VCO-based sigma-delta modulator. The control voltage of the VCO is the error signal generated in the first stage. Using this scheme, the nonlinearity of the VCO is significantly suppressed, since its input has a small swing.

3- TDC-BASED QUANTIZATION

TDCs convert a time-difference variable to a digital code. The use of TDCs in nuclear science research dates back to 1970s. The applications of TDCs, however, has extended well beyond nuclear science to digital storage oscillators, laser range finders , digital frequency synthesizers, and ADCs, to name a few [15, 16]. TDC-based sigma-delta modulators are another structures classified as time-mode ADCs. Here, the width of the pulses generated by a preceding VTC is quantized with the time resolution of T_Q.

In [17], a closed-loop continuous-time (CT) sigma-delta modulator employing a synchronous ramp-based pulse-width modulator (PWM) as the VTC and a multi-bit flash TDC as the sampler is introduced. Although some significant achievements are reported, this architecture suffers from some main problems mainly arising from the nonlinearity of synchronous PWM. In frequency domain, the synchronous ramp-based PWM waveform's spectrum contains the signal frequency, reference frequency and its harmonics and progressively higher order intermodulation products of the reference harmonics and signal frequency. The feedback pulse generated by the TDC is a sampled and held version of the PWM pulse with a sampling period of T_Q. This sampling process results in aliasing of the high frequency tones within the spectrum of the input PWM waveform. Hence, the noise floor is significantly increased resulting in the degradation of the modulator performance. The time-encoded structures in [18, 19] can also be categorized into wideband high performance PWM-based CT sigma-delta modulators. However, their sampling rates are in the order of multi-GHz resulting in significant power consumption in the quantizer. As a design example, a CT TDC-based sigma delta modulator is explored in the following section.

Table. 1 compares the performance of some recent work in time-based ADCs implemented in CMOS technology.

TABLE 1
PERFORMANCE COMPARISON OF TIME-MODE ADCS

Ref.	Tech (nm)	f_s (MHz)	BW (MHz)	SNDR (dB)	Power (mW)	FoM (fJ/step)
[20] *TCAS.I'* 09	180	140	0.4	38.2	0.8	14381
[21] *VLSI Symp.'* 07	130	950	20	55	38.4	2089
[22] *ISCAS'* 09	130	900	20	78	87	331
[23] *CICC'* 11	130	1200	4	77	13.8	298
[24] *ISSCC'* 09	65	250	20	60	10.5	321
[25] *IEEE Conf.'* 12	90	560	20	67.3	3.1	40.6
[26] *TVLSI'* 12	130	600	20	52.5	14.3	1043.8
[13] *VLSI Symp.'* 11	180	10	0.5	66	0.475	285.5
[27] *IEEE MTT-S'* 11	90	640	8	59	4.3	341.2
[28] *ESSCIRC'* 06	90	3.4	0.02	44.2	0.044	5670
[29] *JSSC'* 11	65	1200	600	20.4	2	104.2

4- PROPOSED DESIGN EXAMPLE

In order to further emphasize the superiority of the time-based encoding, the concept is elaborated for a TDC-based continuous-time sigma-delta modulator. The conceptual block diagram of the proposed modulator is depicted in Fig. 5. It shows how a conventional SDM is exchanged to a time-based one.

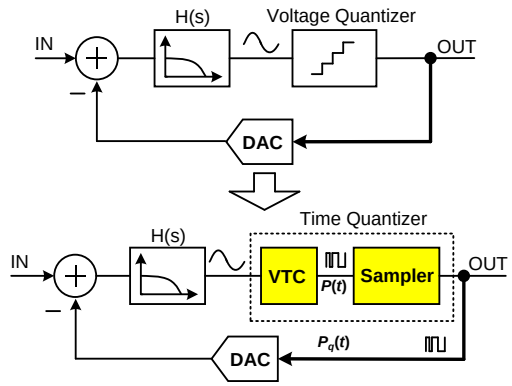

Fig. 5. An exchange of the voltage-mode CT sigma delta modulator to the time-mode one.

For the proposed time-based continuous-time modulator (TCSDM), an asynchronous PWM (APWM) is utilized as a VTC. The structure of the APWM is illustrated in Fig. 6. An APWM is similar to a single-bit sigma-delta modulator. It is a closed-loop nonlinear system, transforms the information in the amplitude axis into the time axis. An APWM consists of an integrator, a hysteretic comparator, and a negative feedback loop. In the APWM loop, $A(s)$ represents a first order passive low-pass filer (LPF) and the comparator is a hysteretic one with the hysteresis factor of h. The hysteretic comparator is inherently a nonlinear positive feedback circuit which can be quasi-linearly modeled using describing functions (DFs) [30]. The nonlinearity of the comparator is denoted as $N(A,\varphi)$. APWM oscillates at the carrier frequency of f_c for a zero input signal. Applying the Barkhausen oscillation criterion for a zero input, the limit cycle and its amplitude will be obtained by solving of the following equation:

$$-1/N(A,\phi) = A(j\omega) \quad @\omega = \omega_c \tag{5}$$

Equation (5) can be solved graphically to find the value of the limit cycle frequency where the limit cycle can be determined from the crossing point of the $-1/N(A,\varphi)$ and $A(j\omega)$ curves. Assuming a first order $A(s)$ as $\omega_a/(s+\omega_a)$ the self oscillation frequency, f_c is obtained as:

$$\omega_c = \frac{\omega_a\left(2+\sqrt{4-\pi^2h^2}\right)}{\pi h} \approx \frac{4\omega_a}{\pi h} \tag{6}$$

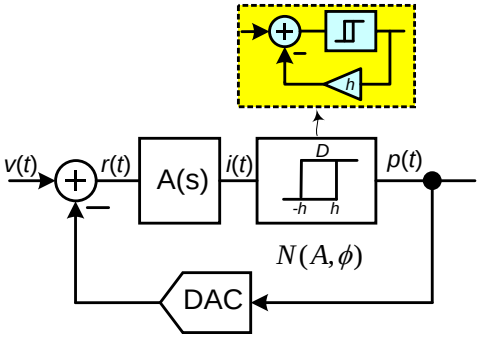

Fig. 6. The block diagram of an APWM.

The oscillation frequency or a limit cycle denoted by f_c is the main design parameter that determines the spectral purity and the quality of the amplitude-to-time transformation. The spectral properties of the APWM can be determined through an analysis of limit cycle oscillations.

Notating the APWM output signal with $p(t)$ the sampler quantizes it as $p_q(t)$ with the quantization error of $E_Q(t)$. The associated waveforms of this phenomenon is shown in Fig. 7. Here it is assumed that the resolution of the time-based sampler is T_Q.

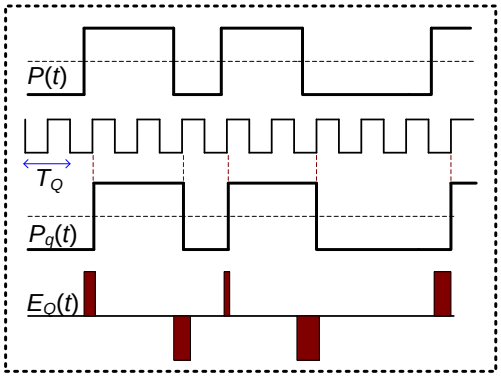

Fig. 7. Quantization of the pulse widths by a time-based sampler.

In an APWM, the output signal is a lossless representation of its input, since the information is stored in the pulse width. However, the sampling will introduce an error even if the sampling frequency is higher than the Nyquist rate. The average rate of the error occurrence is f_0 for a non-zero sinusoidal input signal. The power spectral density (PSD) of $E_Q(t)$ is needed to calculate the quantization noise effect of the sampler. However, it is difficult to make an exact analysis due to the redundancy of the error pulse widths. But fortunately, this is not really necessary to find an exact mathematical formula for this purpose [31]. For a sampler with the resolution of T_Q, the error signal, is approximated as:

$$e(t)=\sum_{n=-\infty}^{\infty} Q_n\,\delta(t-nT_0)\;;\quad -2T_Q<Q_n<2T_Q \qquad (7)$$

where Q_n is the amplitude of the error pulses and T_0 is the inverse of the instantaneous frequency of the APWM ($T_0=1/f_0$). Hence, a rough approximation of the error single-sided PSD is given in [31] as:

$$S_e(f)\approx\frac{8}{3f_0}\left(\frac{f_0}{f_Q}\right)^2 \qquad (8)$$

where $S_e(f)$ is the approximated PSD of the error signal and f_Q is the virtual sampling rate of the time-based sampler (i.e., $f_Q=1/T_Q$).

For an APWM oscillating at the limit cycle of f_c, the output signal of the filter, $H(s)$, is sampled with the frequency of f_c rather than f_s. This means that the loop does not have to handle the sample frequency but only the oscillation frequency, f_c. As a result, a new parameter named as over-cycling ratio (OCR) is utilized instead of a well-known oversampling ratio (OSR) in the proposed TCSDM. The OCR is defined as $f_c/2f_B$ where f_B is the signal bandwidth. The approximated signal-to-noise ratio of the TCSDM based on the APWM which utilizes a resonator-based LPF for $H(s)$, is stated as [32]:

$$SNR\simeq\frac{3}{8}U_p^2(L-0.5)^2\frac{2L+1}{\pi^{2L}}\left(\frac{f_Q}{f_c}\right)^2 OCR^{2L+1} \qquad (9)$$

where, U_p is the input signal amplitude and L is the order of the filter, $H(s)$.

For an APWM the minimum required sampling frequency, f_Q for the proper detection of the pulse edges is four times the f_c [32]. For wideband TCSDMs a higher f_c is required, giving rise to the minimum required value of f_Q, (e.g., multi-GHz). A poly-phase sampler can be a suitable alternative for this realization [32]. The poly-phase sampler, shown in Fig. 8, composed of an N-stage time-to-digital converter (TDC), followed by a digital-to-time converter (DTC). The resolution of the TDC is T_Q (i.e., $T_Q=1/f_Q$). The TDC is clocked at the rate of f_s where $f_s=f_Q/N$. The TDC comprised of a chain of delay cells with the resolution of T_Q and a DFF-based shift register. Also the DTC is combined of two multi-input OR gates and two resettable RS flip-flop. Utilizing the double-sampled DFFs in the TDC gives the possibility of reducing f_s as $f_s=f_Q/2N$ [33]. A merged structure of TDC/DTC receives input signal, $p(t)$ and outputs its quantized version as $p_q(t)$. Although the TDC performs as multi-bit quantizer, the output of the poly-phase sampler is a single-bit stream. This way the multi-bit DAC is no longer needed and the DAC-linearizing techniques are not necessary. This makes it possible to resolve the need of multi-bit DAC at the feedback path.

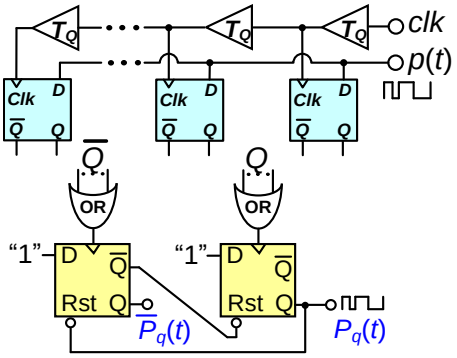

Fig. 8. The proposed poly-phase sampler combined of a TDC and a DTC.

The finalized structure of the proposed TCSDM is illustrated in Fig. 9. The coefficients k_1, $I_{1,2}$ and g, realizes the second order $H(s)$. The passive LPF represented as $L_f(s)=\omega_f/(s+\omega_f)$ is employed in the feedback branch. It suppresses the high frequency tones of $p_q(t)$ before being injected to the feedforward path.

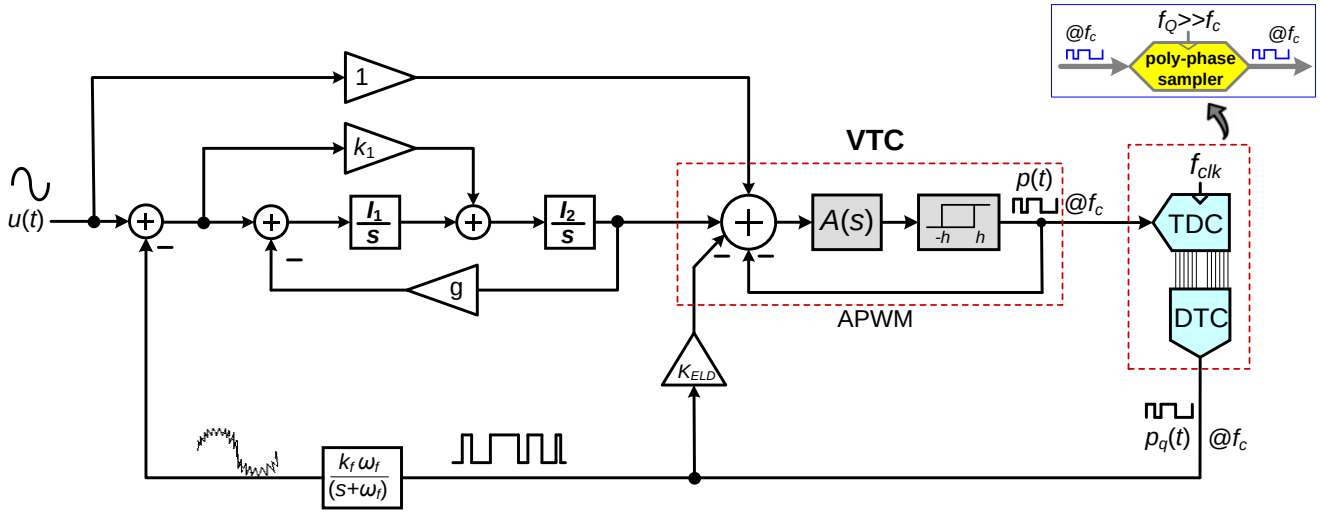

Fig. 9. The block diagram of the proposed TDC-based sigma-delta modulator

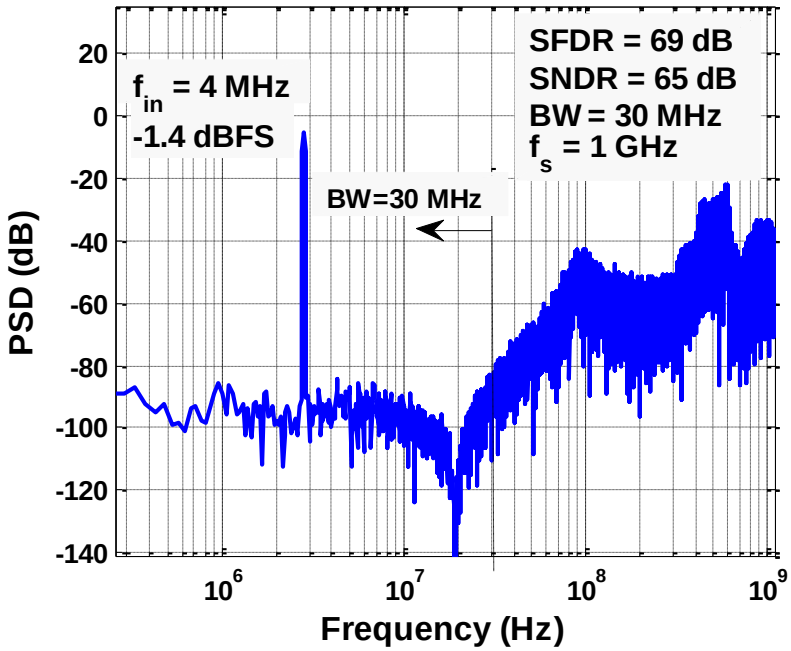

Fig. 10. PSD of the proposed TCS

This is required since the high frequency tones may destabilize the oscillatory VTC. Furthermore, $L_f(s)$ decreases the modulator's sensitivity to the clock jitter. The coefficient K_{ELD} is applied to compensate for the excess loop delay (ELD) of the modulator and thus stabilizing the structure.

In the proposed design example the modulator loop filter is of order 2, the TDC resolution is 80 psec, the PWM center frequency, f_c, is set to be 500 MHz while the TDC clock rate is 1 GHz. The simulated spectrum result shown in Fig. 10, confirms that there is a second order noise shaping in the modulator output signal and the achieved SNDR is 65 dB in a 30 MHz bandwidth. The point is that, this SNDR is obtained without using any complex and high power analog comparators, since the TDC is a fully digital and low power circuit.

5- CONCLUSION

In this paper, a brief review is devoted to the newly-developed generation of the ADCs, named as time-based ADCs. The advantages of the time-based quantization approach are introduced. Two kinds of well-known time-based sigma-delta modulators, VCO-based and TDC-based ADCs, are reviewed and their advantage and disadvantages are highlighted. As a design example, a closed-loop continuous-time TDC-based sigma-delta modulator is proposed and its simulation results are given to confirm the effectiveness of the time-based approach.

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