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An NTF-enhanced time-based continuous-time sigma-delta modulator

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Abstract Translation of the amplitude axis to the time axis can be a promising approach to alleviate the analog-to-digital converter's resolution problems in low-voltage CMOS circuits. From this point of view, a noise-coupled time-based continuous-time sigma-delta modulator (TCSDM) based on the asynchronous pulse width modulator (APWM) and the time-to-digital converter (TDC) is presented. Noise-coupling is realized by extracting the time quantization error of the TDC and injecting its delayed version to the input of the APWM. By using a novel implementation of the noise-coupling technique in the proposed TCSDM, the modulator's noise-shaping order is improved by one. Unlike the conventional noise-coupled sigma-delta modulators, in the proposed structure, the need of an extra subtractor at the quantizer input is resolved through merging the excess loop delay compensation path with the proposed noise-coupling branch. Comparative analytical calculations and behavioral simulation results are presented to verify the performance of the proposed time-based modulator. To confirm the validity of the proposed structure, the effects of main circuit non-idealities in the modulator's performance are taken into consideration and the related simulation results are investigated. A digital-friendly implementation of the quantizer in the proposed modulator makes it suitable for low-voltage nanometer CMOS technologies.

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1 Introduction

Recent developments in mobile computing and wireless internet have led to a significant growth in demand for portable computers and smart phones that need low cost and low-power wireless standards. Design of high resolution analog-to-digital converters (ADCs) suitable for broadband applications is always in the scope of the researcher's attention. Sigma-delta modulators have attracted a lot of attention as digital-friendly structure for ADCs since the substantial part of the signal processing is performed in digital domain. Continuous-time (CT) sigma-delta modulators are widely used to digitize moderate to high bandwidth analog signals due to their efficient power consumption and silicon die area [1]. However, the conventional mostly-analog structures suffer from the CMOS technology scaling problems. The voltage headroom reduction not only increases the voltage error and reduces the signal-to-noise ratio (SNR), but also it deteriorates the effect of the nonlinear behavior of transistors, and thus, reduces the dynamic range of voltage mode circuits [2].

With the advancement of CMOS technology, processing the signal in time domain becomes increasingly beneficial due to finer time resolution [3]. The intrinsic gate propagation delay time of digital circuits is the primary advantage of technology scaling. The increasing switching speed of MOS transistors offers an excellent timing accuracy such that the time resolution of digital circuits has well overcome the problems of the voltage resolution in analog circuits. As a result, the time-based quantizers have

emerged as a promising quantization architecture for CT sigma-delta modulators [4].

Architecturally, time-mode ADCs can be classified into the open-loop and closed-loop ADCs. Unlike the former, the latter employs the negative feedback to improve the performance. An open-loop time-mode ADC typically consists of a voltage-to-time converter (VTC), such as the voltage controlled oscillators (VCOs), and a time-to-digital converter (TDC). The input voltage is sampled by the VTC and converted to a pulse, whose width is proportional to the amplitude of the sampled input. The TDC produces the digitized version of the pulse width [5]. Although the open-loop time-mode ADCs can have short conversion time and lower power consumption, however, their performance is severely affected by the nonlinearity of the VTC and non-ideality of the TDC [6]. As a result, these ADCs typically have a poor signal-to-noise and distortion ratio (SNDR), and hence, some linearization techniques are essentially needed.

The TDC-based closed-loop CT sigma-delta modulator is another type of time-mode ADCs [7]. In this structure, the conventional quantizer is realized with the combination of a VTC and a multi-bit TDC. In [8], a closed-loop CT sigma-delta modulator employing a synchronous ramp-based pulse-width modulator (PWM) as the VTC and a multi-bit flash TDC as the sampler is introduced. Although some significant achievements are reported, this architecture suffers from some main problems mainly arising from the synchronous PWM. In frequency domain, the synchronous ramp-based PWM waveform's spectrum contains the signal frequency, reference frequency and its harmonics and progressively higher order intermodulation products of the reference harmonics and signal frequency. The feedback pulse generated by the TDC is a sampled and held version of the PWM pulse with a sampling period of T_Q (the time resolution of TDC). This sampling process results in aliasing of the high frequency tones within the spectrum of the input PWM waveform. Hence, the noise floor is significantly increased resulting in the degradation of the modulator performance.

In the proposed time-based continuous-time sigma-delta modulator (TCSDM), an asynchronous PWM (APWM) is employed as the VTC without a reference clock, resolving the mentioned challenges in [8]. A multi-bit flash TDC which utilizes dual-edge triggered D-flip flops (DEDFFs) is applied to digitize the APWM output signal. Using DEDFF can enhance the time resolution of the TDC since it works on both rising and falling edges. This way, the time resolution becomes finer in comparison with a TDC based on a simple DFF. A digital-to-time converter (DTC) combined with the TDC emulates the performance of the multi-bit digital-to-analog converter (DAC), avoiding the DAC nonlinearity problems.

The proposed structure also introduces the novel implementation of the noise-coupling idea to enhance the modulator performance without the changes reported in [9] and [10].

The paper is organized as follows. An overview of the time-based sigma-delta modulator and a detailed description of the proposed VTC are presented in Sect. 2. In Sect. 3, a noise transfer function (NTF) enhancement technique is introduced. An analytical approach of the error approximation is given in Sect. 4. System level simulation results of the proposed TCSDM are presented in Sect. 5. Section 6 discusses the main circuit non-idealities. The comparative points of the proposed modulator are highlighted in Sect. 7. Finally, Sect. 8 concludes the paper.

2 Voltage-to-time conversion

The simplified block diagram showing the exchange of a conventional voltage-mode CT sigma-delta modulator to a time-based one is illustrated in Fig. 1. A time-based quantizer consists of a VTC to perform the amplitude to time mapping and a digital circuit to digitize the widths of the pulses generated by the VTC. More details of the structure will be given in the following sections.

2.1 Asynchronous pulse width modulator (APWM)

In the proposed structure, an APWM is employed to realize the VTC due to its better spectral profile in comparison with the synchronous ramp-based PWM. An APWM which is similar to a single-bit sigma-delta modulator is shown in Fig. 2. It is a closed-loop nonlinear system which transforms the information in the amplitude axis into the time axis. An APWM consists of an integrator, a hysteretic comparator, and a negative feedback loop. For a sinusoidal

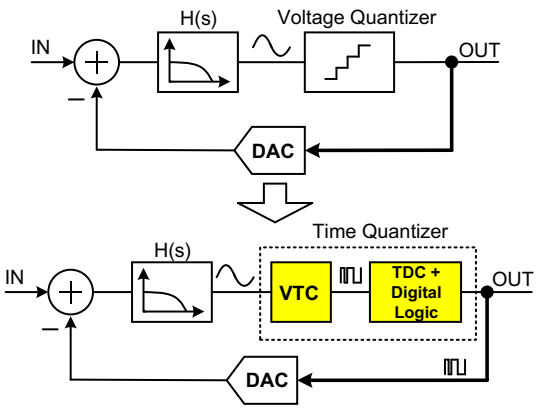

Fig. 1 An exchange of the voltage-mode CT sigma-delta modulator to the time-mode one

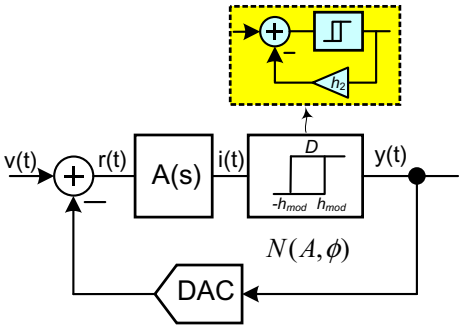

Fig. 2 The structure of an APWM replaced as the VTC in Fig. 1

input signal of $v(t)$, the time-dependent duty cycle of the output signal denoted by $D(t)$ is obtained as [11]:

$$D(t) = \frac{W(t)}{T(t)} = \frac{1}{2}(1 + \mathrm{v}(t)) \tag{1}$$

where both the pulse width, $W(t)$, and the pulse period, $T(t)$, are continuous and time-dependent functions. Unlike the synchronous PWM, due to the absence of the clock signal, the output of the APWM is a continuous-time and discrete-amplitude signal. Since the time is not quantized or sampled, the quantization noise is not attributed to its output signal [12]. As a result, neither SNDR nor SNR factors is calculated for APWMs while SFDR is still valid. In the APWM, the amplitude to time transformation is realized through its inherent self oscillation. The oscillation frequency or the limit cycle denoted by f_c is the main design parameter that determines the spectral purity and the quality of the amplitude-to-time transformation. The spectral properties of the APWM can be determined through the analysis of limit cycle oscillations.

2.2 Limit cycle frequency of the APWM

The hysteretic comparator is inherently a nonlinear positive feedback circuit which can be quasi linearly modeled using describing functions (DFs) [13]. Applying Tsypkin's method [14] is more accurate than DFs in calculating the limit cycle oscillations especially for lower orders of $A(s)$. However, due to the simplicity of the DF analysis, the DF method is found to be more suitable for the analysis of the APWM. The application of a DF is justified if the frequency of the input signal is significantly lower than f_c.

Regarding an APWM loop as the feedback structure, the existence of a limit cycle oscillation is determined according to the gain-phase relation famed as Barkhausen criterion. Since the APWM is a nonlinear element due to the presence of a hysteresis, the self-oscillation conditions may be satisfied for a zero input. For a hysteretic comparator, the describing function $N(A,\varphi)$ is given by [11]:

$$\begin{aligned} N(A,\phi) &= \frac{4D}{\pi A} e^{-j\sin^{-1}(h_1/A)} \\ &= \frac{4D}{\pi A}\sqrt{1-(h_1/A)^2} - j\frac{4Dh_1}{\pi A^2}; \quad (A \geq h_1) \end{aligned} \tag{2}$$

where h_1 is the hysteresis factor shown in Fig. 2, D is the level of the hysteresis window and A is the amplitude of the input signal. Applying the Barkhausen oscillation criterion for a zero input, the limit cycle and its amplitude will be obtained by solving of the following equation:

$$-1/N(A,\phi) = A(j\omega) \quad @\,\omega = \omega_c \tag{3}$$

Equation (3) can be solved graphically to find the value of the limit cycle frequency where the limit cycle can be determined from the crossing point of the $-1/N(A,\varphi)$ and $A(j\omega)$ curves. Assuming a first order $A(s)$, the self oscillation frequency, f_c, is obtained as:

$$\begin{aligned} &A(s) = \omega_a/(s+\omega_a) \quad \Rightarrow \\ &\omega_c = \frac{\omega_a\left(2+\sqrt{4-\pi^2 h_1^2}\right)}{\pi h_1} \approx \frac{4\omega_a}{\pi h_1} \end{aligned} \tag{4}$$

Increasing the degree of the filter may give a better SFDR at the expense of higher power consumption and also the poor stability. Hence, it is not usual to increase the degree of $A(s)$ higher than three. For a sinusoidal input signal of $Asin(\omega t)$, the instantaneous switching frequency of the APWM will be time-dependent and it can be calculated as [11]:

$$f(t) = f_c\left(1 - \mathrm{v}^2(t)\right) \tag{5}$$

And also the average instantaneous frequency denoted by f_0 can be stated as [11]:

$$f_0 = f_c\left(1 - 0.5A^2\right) \tag{6}$$

2.3 Hysteresis adjusting of the comparator

For an APWM with a constant hysteresis factor, the output switching frequency, f_0, is decreased when the input signal level is increased. The variation of f_0 may deteriorate the loop gain and linearity performance or even cause the instability problem in a higher order modulator [14]. An alternative to this variation is to make it constant. This can be achieved through applying an extra negative feedback branch (h_2) around the hysteretic comparator (Fig. 2). The value of this extra branch can be calculated by equating the relations (4) and (6) as:

$$\frac{4\omega_a}{2\pi^2 h_1} = \frac{4\omega_a}{2\pi^2 (h_1 - h_2)}\left(1 - 0.5A^2\right) \quad \Rightarrow \quad h_2 = 0.5A^2 h_1 \tag{7}$$

This extra compensation branch depends on the input signal amplitude and forces the average instantaneous

frequency to be equal to the limit cycle frequency as the input signal amplitude is changed. By using this extra branch, a new hysteretic comparator with a different hysteresis factor denoted as $h_{dynamic}$ is obtained as:

$$h_{dynamic} = h_1 - h_2 = (1 - 0.5A^2)\, h_1 \tag{8}$$

As it is clear from (8), the value of $h_{dynamic}$ varies versus the input signal amplitude. Comparators with variable hysteresis are reported in [15–17], where the hysteresis factor is adjusted by controlling the gate voltage of the control transistors. However, it should be noted that the maximum deviation of f_0 occurs when the input signal amplitude is at its maximum level and it is negligible for small input amplitudes. This way, we may modify $h_{dynamic}$ by substituting A with the maximum stable amplitude (MSA) level as:

$$h_{\mathrm{mod}} = (1 - 0.5(\mathrm{MSA})^2)\, h_1 \tag{9}$$

where h_{mod} is the modified hysteresis factor which is a constant value. Although by using h_{mod} instead of $h_{dynamic}$, the deviation compensation of f_0 is not completely fulfilled, the deviation is negligible for small input amplitudes. Hence, it is worth using a constant hysteresis factor rather than a dynamic one from the implementation point of view. By using the new hysteresis value for the comparator, the instantaneous frequency of the APWM, f_0, becomes approximately equal to the free running frequency, f_c, namely $f_0 \approx f_c$.

3 NTF enhancement through noise-coupling

The SNR of a sigma-delta modulator is improved if the order of the loop filter, $H(s)$, is increased. But this improvement is achieved at the expense of lower stability. The NTF enhancement through the noise-coupling is another technique to increase the noise-shaping order of a sigma-delta modulator. In this technique, the signal transfer function (STF) does not change and the order of the loop filter remains the same. This enhancement is achieved by extracting the quantization error and then coupling its filtered or delayed version into the forward path of the modulator. This way, the new NTF for a noise-coupled (NC) sigma-delta modulator can be stated as [9]:

$$NTF_{\mathrm{NC}} = (1 - G(z))NTF \tag{10}$$

where NTF_{NC} is the NTF of the enhanced sigma-delta modulator and $G(z)$ is the transfer function of the filter in the noise-coupling branch. Considering a simple delay block such as z^{-1} for $G(z)$, the NTF of the enhanced sigma-delta modulator is improved by one order according to (10).

Unlike the realization of the noise-coupling technique in discrete-time (DT) sigma-delta modulators, it is not so straight forward to take the advantage of this idea in CT sigma-delta modulators. This is because of the difficulty in implementing the analog subtractor. In [10], the discrete-time noise-coupling branch using a switched-capacitor circuit and a clocking scheme is utilized to realize the noise-coupling in a CT sigma-delta modulator. Although it is shown that the noise-coupling is achieved but the introduced modulator is not a fully continuous-time since the noise-coupling branch utilizes a discrete-time active subtractor. This makes it an unsuitable choice for wideband and low power applications.

In the proposed TCSDM, a new way of noise-coupling realization, which is suitable for a CT sigma-delta modulator, is introduced. This is elaborated in the following section.

3.1 Proposed NTF-enhanced TCSDM

The conceptual block diagram of the proposed TCSDM with excess loop delay (ELD) compensation and NC branches is shown in Fig. 3. The ELD effectively increases the order of the loop filter, potentially de-stabilizing the modulator and degrading its noise-shaping performance. This can be compensated by using a fast feedback branch comprising of a delay and gain block around the quantizer [18]. In Fig. 3, the branch with a delay of T_{d1} is applied for the ELD compensation.

The sampler with a rate of f_Q quantizes the edges of the VTC output pulses. Furthermore, the two-level output signal of the VTC is subtracted from the output of the sampler. This way, the time quantization error is extracted at the output of the subtractor. If this error is injected to the VTC after a delay of T_{d2}, the noise-coupling concept would be realized. The extended version of the modulator is illustrated in Fig. 4. As shown in Fig. 4, since the output signal of the APWM is a two-level signal, the two branches of the NC part can be easily separated. Doing this, the summing node at the input of the APWM can serve both the ELD and NC branches. This way, the need of an extra subtractor in the NC path is resolved.

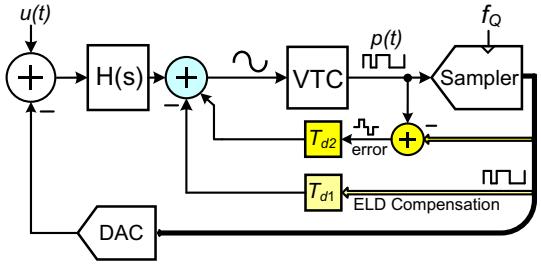

Fig. 3 Conceptual schematic of the proposed TCSDM with ELD compensation and noise-coupling branches

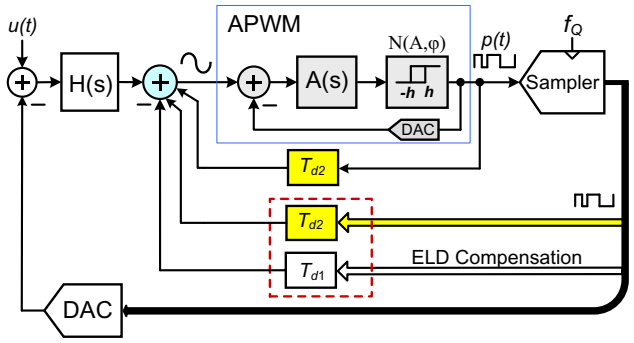

Fig. 4 Extended version of the proposed TCSDM based on the APWM

3.2 Modification of the proposed NTF-enhanced TCSDM

The delay blocks of T_{d1} and T_{d2} in Fig. 3 can be represented as z^{-Td} in discrete-time domain, where T_d is determined by the modulator output rate. However, at high sampling frequencies, namely over 1 GHz, it is difficult to implement an accurate digital delay circuit as a representation for the delay blocks. On the other hand, since the quantizer of the proposed modulator works asynchronously, the rate of the feedback square pulses is defined by the modulator limit cycle and not by the given clock frequency. As a result, using the conventional D flip-flops (DFFs) synchronized by an external clock signal may not be an effective method to realize the delay blocks.

An alternative solution is introduced if the delay blocks are realized using passive elements. This way, the delay block may be implemented by a simple analog delay such as e^{-sTd}. This can be realized by a first-order passive low-pass filter (LPF) such as $\alpha\omega_p/(s+\omega_p)$ where ω_p is the pole of the filter and α is the gain adjusting constant. The delay of the LPF is determined by the value of ω_p (i.e. $T_{delay} = 1/\omega_p$). This approach is applicable if the signal frequency is sufficiently lower than the bandwidth of the LPF. Otherwise, it would not be an effective alternative to the delay blocks. To ensure this, the characteristic of the LPF is represented by the following equation:

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{\alpha\,\omega_p}{s+\omega_p} \tag{11}$$

For a sinusoidal input signal with an angular frequency of ω_{IN} and peak amplitude of V_p, the output of the LPF is given by:

$$v_{out}(t) = \frac{\alpha V_p}{\sqrt{1+(\omega_{IN}T_{delay})^2}} \times \sin\left(\omega_{IN}\left(t-T_{delay}\right)\right);$$
$$T_{delay} = RC \tag{12}$$

If $\omega_{IN} << 1/T_{delay}$, which is the usual case in sigma-delta modulators, then we have:

$$v_{out}(t) \approx \alpha V_p \sin\left(\omega_{IN}\left(t-T_{delay}\right)\right) \tag{13}$$

This indicates that, owing to the oversampling in sigma-delta modulators, the LPF output signal is delayed by a factor which is independent of the amplitude and frequency of the input signal.

Using the analog delay blocks, the structure shown in Fig. 4 can also be more simplified if we assume $T_{d1} = T_{d2}$. This way, the branches surrounded with a dashed line in Fig. 4 can be combined together and a block with a gain of 2 is inserted in the ELD compensation path to represent these two branches. On the other hand, all of the internal branches can be merged in the inherent summing node of the APWM. By this simplification, the extra summer at the input of the time quantizer is also eliminated.

The modified block diagram of the proposed noise-coupled TCSDM using analog delays is shown in Fig. 5. As it is clear, the inherent feedback path of the APWM is now in parallel with the NC branch. These two branches are subtracted in the summing node of the APWM. As a result, these two paths are combined resulting in the following relation:

$$1-\frac{\alpha\omega_p}{s+\omega_p} = \frac{s+(1-\alpha)\omega_p}{s+\omega_p} \approx \frac{s}{s+\omega_p} \tag{14}$$

As it is clear, the combination of these two branches, highlighted in Fig. 5, represents a high pass filter (HPF). By this modification, the ultimate block diagram of the proposed TCSDM is more simplified from the implementation aspect, showing the effectiveness of the proposed noise-coupled TCSDM.

3.3 An example of the finalized structure of the proposed NTF-enhanced TCSDM

As an example for the proposed TCSDM, the third-order loop filter is utilized as illustrated in Fig. 6. Here, the sampler with the rate of f_Q is replaced by the combination

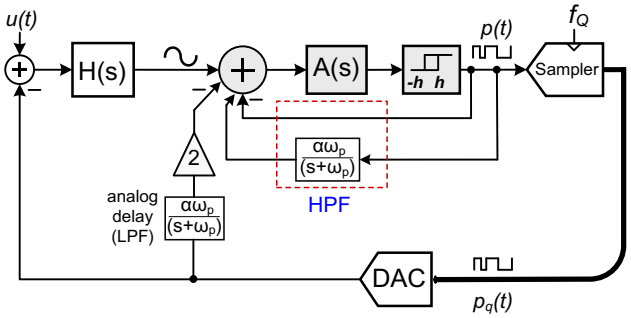

Fig. 5 The simplified version of the proposed noise-coupled TCSDM using analog delays and combining NC and ELD compensation branches

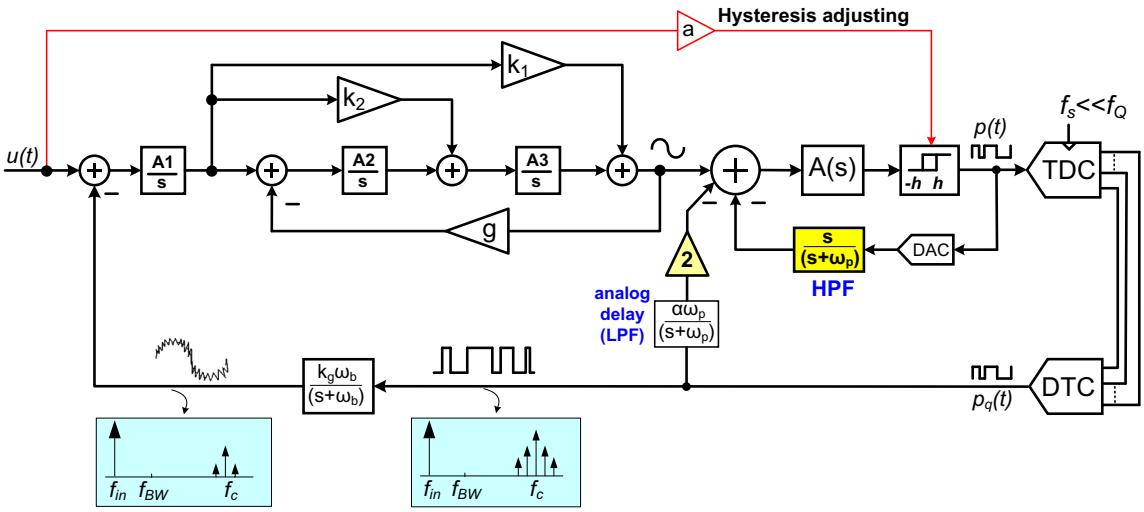

Fig. 6 A complete block diagram of the proposed third-order noise-coupling TCSDM

of TDC and DTC. The clock rate of the TDC is f_s where $f_s << f_Q$. This will be more explained in the following section.

It should be mentioned that, the APWM oscillates properly if its input signal is slower enough compared to its output signal, $p(t)$ [19]. It means that high frequency components should be attenuated before the summing node at the input of the APWM. For this to be satisfied, the combination of a DAC and a finite impulse response filter (FIR DAC) [4] or a first-order passive LPF such as $k_g\omega_b/(s + \omega_b)$ is utilized in the feedback path to filter out the high frequency components around the limit cycle frequency of $p_q(t)$. Here, k_g is the adjusting gain factor which is obtained through the simulation procedure and ω_b is the filter cut-off frequency and it is selected to be to some extent higher than the desired bandwidth. As will be shown later, this filter can also improve the clock jitter immunity of the modulator [19].

Here, it is worth mentioning that by exploiting LPFs in the ELD compensation and NC branches, not only the required delays of these paths are realized, but also they can filter out the high frequency tones of $p(t)$. This makes the APWM to oscillate properly at the rate of the limit cycle.

4 Time quantization and error approximation

4.1 Time quantization

Although the amplitude-to-time mapping of an APWM can be very accurate, the output may not be applicable for digital processing without the pulse widths quantization. The combination of a sample and hold circuit and a digital decimation filter can be applied for this target [11]. But in practice, extremely high sampling rates may be needed to quantize the data at the edges of the APWM output signal. However, several solutions have been suggested to decrease the clock rate of the time quantizer [12], [20].

In this paper, a multi-stage delay-line-based TDC is proposed to replace the classic sampling stage. As described in the previous section, the APWM block generates pulses whose widths are proportional to the amplitude of the input signal. Since the VTC block is completely asynchronous, the time is not quantized and the output contains no quantization noise. The TDC generates a digital code that corresponds to the time edges of the pulse and provides a "time-quantized" feedback signal. The quantization of the pulse width is required to ensure that the feedback signal corresponds to the quantized output code of the TDC. Otherwise, the noise shaping concept may not be satisfied. The main advantage of using the TDC is that it can digitize fine pulse widths in the order of picoseconds at relatively low clock rates. Moreover, the TDC is mostly composed of digital components such as inverters and latches, and hence, it can be benefited from the high speed and low power consumption of digital circuits [21].

4.2 Time-to-digital converter structure

In an N-level TDC, the combination of a delay line and N latches divide the phase of the input clock into N-1 similar parts and outputs a quantized version of the input pulse width [22]. The structure of the proposed N-stage TDC is illustrated in Fig. 7(a). In this TDC, the clock signal propagates through the cascade of digital delay cells with delays of T_Q, whose outputs are fed to the *Clk* input of the flip-flops array. An N-stage TDC clocked at f_s can be conceived as a mere DFF with the virtual sampling clock of

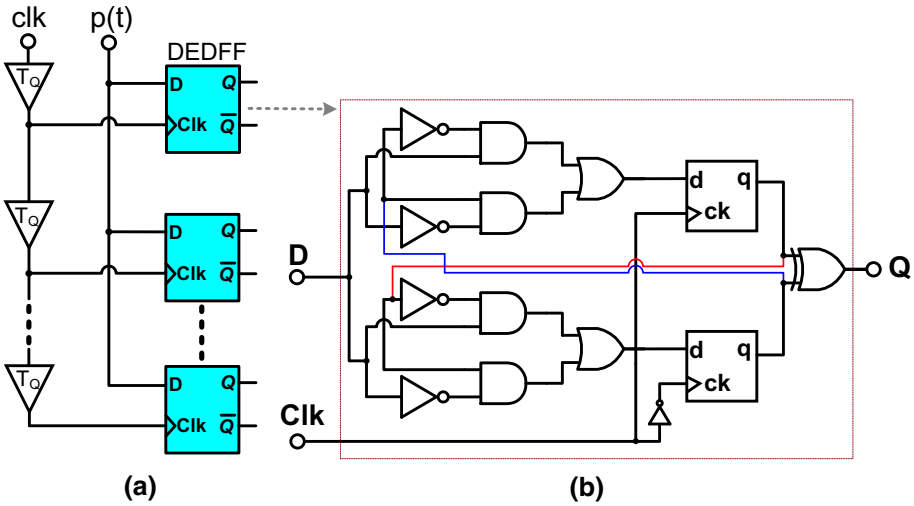

Fig. 7 **a** The block diagram of the proposed DEDFF-based multi-stage TDC, and **b** the gate level implementation of the DEDFF

$f_Q = N \times f_s$. It can be shown from (1) that the width of the APWM pulses can be calculated as:

$$W = \frac{T_c}{2}\left(\frac{1}{1 - \mathrm{v}(t)}\right) \tag{15}$$

where W is the width of the pulses, T_c is the period of the limit cycle frequency obtained for zero input signal [$v(t) = 0$]. It can be concluded from (15) that the width of the pulses can be varied as $T_c/4 < W < \infty$. The TDC must be able to detect all of the edges of the APWM output signals, even those of the smallest pulse. Hence, the minimum TDC sampling frequency for which all of the APWM widths can be quantized should be $f_s \geq 4f_c$. As mentioned before, the sampling frequency of a classic TDC is $f_s = f_Q/N$. This value of the sampling rate may be undesirably high for high limit cycle frequencies according to $f_s \geq 4f_c$. Thus, it is preferred to change the TDC structure in a way that the needed sampling clock is reduced.

In the proposed TDC, all of the latches are based on dual edge triggered DFFs (DEDFFs). By using DEDFFs instead of simple DFFs, both the rising and falling edges of the pulse widths are quantized. This way, the effective sampling frequency of the TDC is doubled. In other words, in a DEDFF-based TDC, the minimum required sampling frequency is halved as $f_s = f_Q/2N$. Decreasing the minimum required TDC sampling frequency relaxes the design of the TDC latches and also has a significant effect in the power consumption reduction. As shown in Fig. 7(b), the DEDFF consists of two multiplexers (MUX) and two DFFs which are combined in a back to back structure.

4.3 Digital-to-time converter

The output signals of the TDC are injected into the DTC. The DTC block shown in Fig. 8(a) works as a parallel to serial converter to recombine the asynchronous samples back to one quantized square wave signal to feed a single-bit DAC. It is comprised of two N-input OR gates and two resettable DFFs clocked by the output of two OR gates. The output signal of the DTC denoted as $p_q(t)$ is the same as the output of the APWM. The signal $p_q(t)$ is the time quantized version of $p(t)$. The TDC has a multi-bit structure and may need a multi-bit DAC to generate the feedback signal. However, by using a DTC and merging the TDC outputs to make a single-bit two-level stream, the need for a multi-bit DAC is resolved. This way, a 1-bit DAC is adequate for the design, and hence, the nonlinearity problem of the multi-bit DACs will not be a challenge anymore.

4.4 Loop filter topology selection

The CT loop-filter, $H(s)$, which determines the order of the modulator can be implemented using a chain of integrators with either feedback or feedforward branches [23]. The feedforward architecture has the disadvantage that its closed-loop frequency response has a peaking at high frequencies due to the zeros in the signal path. In the feedback structure which has L feedback paths, the frequency response is monotonic without any frequency peaking. Furthermore, the anti-aliasing degree of the feedback structure is of the order L while this is only one when the filter topology is feedforward. On the other hand, in the feedforward structures, the signal component at the output of the loop filter integrators is reduced and the modulator sensitivity to the integrator nonlinearities is decreased [23]. Moreover, feedforward filters are the best solution when implementing low-power modulators, since only one feedback path is provided, and hence, only one DAC is theoretically required. The transfer function of a feedforward structure is as follows:

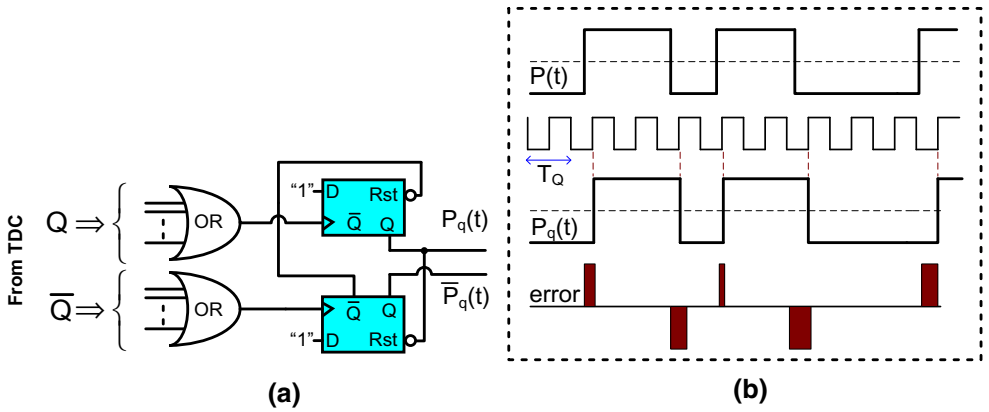

Fig. 8 **a** The block diagram of the proposed DTC, and **b** sampling of the pulse modulated square wave and the time quantization error

$$H_{FF}(s) = \frac{I_1 k_1 s^{L-1} + I_1 I_2 k_2 s^{L-2} + \cdots + I_1 I_2 \cdots I_L k_L}{s^L} \quad (16)$$

where L is the filter order, I_i and k_i are the integrator gains and feedforward coefficients, respectively. The loop filter design is commonly performed in discrete-time domain by realizing the desired $H(z)$ as $NTF(z) = 1/(1 + H(z))$ via the delta-sigma toolbox [24].

4.5 Time quantization error approximation

The APWM output signal is a lossless representation of its input, since the information is stored in the pulse width. However, the sampling in TDC will introduce an error even if the sampling frequency is higher than the Nyquist rate. The difference between the signals $p(t)$ and $p_q(t)$ is considered as the time quantization error. The average rate of the error occurrence is f_0 for a non-zero sinusoidal input signal. As shown in Fig. 8(b), the error signal is similar to the pulse amplitude modulated (PAM) signal. The power spectral density (PSD) of this error is needed to calculate the quantization noise effect of the TDC/DTC. However, it is difficult to make an exact analysis due to the redundancy of the error pulse widths. But fortunately, this is not really necessary to find an exact mathematical formula for this purpose [11]. For a TDC with the resolution of T_Q, the error signal, $e(t)$, is approximated as a series of impulse trains:

$$e(t) = \sum_{n=-\infty}^{\infty} Q_n \, \delta(t - nT_0), \quad -2T_Q < Q_n < 2T_Q \quad (17)$$

where Q_n is the amplitude of the error pulses and T_0 is the inverse of the instantaneous frequency of the APWM ($T_0 = 1/f_0$). Hence, a rough approximation of the error single-sided PSD is given in [11] as:

$$S_e(f) \approx \frac{8}{3f_0}\left(\frac{f_0}{f_Q}\right)^2 \quad (18)$$

where $S_e(f)$ is the approximated PSD of the error signal and f_Q is the virtual sampling rate of the time-based sampler.

4.6 SNR calculation of the proposed TCSDM

For an APWM oscillating at the limit cycle of f_c, the output signal of the filter, $H(s)$, is sampled with the frequency of f_c rather than f_s. This means that the loop does not have to handle the sample frequency but only the oscillation frequency, f_c. As a result, a new parameter named as overcycling ratio (OCR) is utilized instead of the well-known oversampling ratio (OSR) in the proposed TCSDM. The OCR is defined as $f_c/2f_B$ where f_B is the signal bandwidth. It is applied in order to design the coefficients of the loop filter and also to approximate the SNR. The OCR has a significant effect on the performance of the modulator [11].

It is usual to approximate the SNR of the CT sigma-delta modulators according to discrete-time counterparts using the impulse invariance transformation (IIT) [18]. The NTF of the discrete-time equivalent of an *Lth*-order sigma-delta modulator is as $(1 - z^{-1})^L$. Applying the same approach in classic discrete-time sigma-delta modulators, the SNR of the modulator can be approximated. The NTF of the time-based sigma-delta modulator shown in Fig. 1 is calculated as:

$$NTF(z) = \left(1 - z^{-1}\right)^L \approx \left(2\pi \frac{f}{f_0}\right)^L \quad @f << f_0 \quad (19)$$

According to the PSD approximation of the time quantization error in (18), the noise power of an *Lth* order TCSDM within the bandwidth of f_B can be obtained as:

$$P_e = \int_0^{f_B} S_e(f)|NTF(f)|^2 df = \int_0^{f_B} \frac{8}{3f_0}\left(\frac{f_0}{f_Q}\right)^2 |NTF(f)|^2 df$$

$$P_e = \frac{8}{3} \times \frac{(2\pi)^{2L}}{2L+1} \times T_Q^2 \times f_0^2 \times \left(\frac{f_B}{f_0}\right)^{2L+1} \quad (20)$$

For a sinusoidal input signal with the peak amplitude of U_p, the signal power is $U_p^2/2$. Thus, the first approximation of the SNR can be represented as:

$$SNR \triangleq \frac{P_s}{P_e} = \frac{3}{16} U_p^2 \times \frac{2L+1}{(2\pi)^{2L}} \times \frac{1}{T_Q^2} \times \frac{1}{f_0^2} \times \left(\frac{f_0}{f_B}\right)^{2L+1} \tag{21}$$

It is preferable to rewrite the Eq. (21) regarding the self oscillation frequency, f_c. Considering the hysteresis compensation technique as mentioned before, f_0 may be replaced by f_c. Hence, the new formula for SNR is defined as:

$$SNR = \frac{3}{8} U_p^2 \times \frac{2L+1}{\pi^{2L}} \times \left(\frac{f_Q}{f_c}\right)^2 \times OCR^{2L+1}, \quad OCR = f_c/2f_B \tag{22}$$

Here, a purely differentiating NTF was assumed which does not ensure an optimal noise shaping. For a given *L*th-order modulator, the optimal NTF can be found by minimizing the quantization noise power in the signal bandwidth. The optimal NTF zeros are always located on the unit circle ($|z_n| = 1$), where the damping factor is zero. They are either at DC or complex-conjugate and cause the NTF frequency response to have a notch at the frequencies of the optimal zeros [24]. It can be shown that if a pair of the NTF zeros is optimally placed in the desired bandwidth, the SNR will be enhanced. As a result, the SNR introduced in (22) is multiplied by $(L - 0.5)^2$ [25].

As mentioned before, the noise shaping of the *Lth*-order NTF-enhanced TCSDM using the noise-coupling is improved by one order for a first order noise-coupling. In other words, the SNR of the *Lth*-order NTF-enhanced TCSDM is similar to the SNR of the non-enhanced TCSDM with the order of $L + 1$. Thus, the SNR of the proposed *Lth*-order noise-coupled TCSDM with a zero-optimized NTF denoted as SNR_{NC} is approximated as:

$$SNR_{NC} = \frac{3}{8} U_p^2 \times \frac{2L_{NC}+1}{\pi^{2L_{NC}}} \times (L_{NC} - 0.5)^2 \times \left(\frac{f_Q}{f_c}\right)^2 \times OCR^{2L_{NC}+1} \tag{23}$$

where L_{NC} is equal to $L + 1$. As it is clear, SNR_{NC} depends on the virtual sampling rate (f_Q) of the TDC. It may be straight forward to calculate the SNR_{NC} versus the clock frequency, f_s. This way, the new formula for SNR_{NC} is obtained as:

$$SNR_{NC} = \frac{3}{8} U_p^2 \times \frac{2L_{NC}+1}{\pi^{2L_{NC}}} \times (L_{NC} - 0.5)^2 \times \lambda^2 N^2 \times \left(\frac{f_s}{f_c}\right)^2 \times OCR^{2L_{NC}+1} \tag{24}$$

where λ is a constant which is 1 for the DFF-based TDC and 2 for the DEDFF-TDC and N is the number of the TDC delay stages.

4.7 Upper margin of the quantization noise

The total noise of the time-based quantizer owing to the circuit imperfections is also shaped by the loop filter. However, the integral of this noise over the signal bandwidth denoted as P_Q should be less than the half of the least significant bit (LSB) power. For the maximum input signal of $U_{OL} = OL \times U_{max}$ where OL is the overload factor and U_{max} is the half of the input signal full scale ($U_{max} = FS/2$), the modulator's LSB is calculated as $U_{OL}/2^{ENOB}$, where ENOB stands for the effective number of bits. Thus, the upper limit of the quantizer inband noise power is obtained as:

$$P_{Q\max} = \left(\frac{V_{LSB}}{2}\right)^2 = \left(\frac{U_{OL}}{2^{ENOB+1}}\right)^2, \quad U_{OL} = OL \times U_{\max} \tag{25}$$

According to (25), the maximum allowed power spectral density of the zero-optimized TCSDM quantization noise denoted as $S_{e,NC}(f)$, assuming $f_0 \approx f_c$, is given by:

$$S_{e,NC}(f) < \left(\frac{U_{OL}}{2^{ENOB+1}}\right)^2 \left[\frac{(L_{NC} - 0.5)^2 (2L_{NC}+1)\, OCR^{2L_{NC}+1}}{\pi^{2L_{NC}+1}}\right] \tag{26}$$

where $L_{NC} = L + 1$.

5 System-level simulation results of the proposed TCSDM

The performance of the proposed TCSDM without noise-coupling is approximated in (22). As is shown, the SNR of this structure without noise-coupling depends on the *OCR*, the loop-filter order (*L*), the TDC resolution, and the limit cycle frequency of the APWM. To show the performance of the proposed TCSDM, firstly the simulation results based on the ideal blocks are presented. To confirm the validity of the proposed structure, the main circuit non-idealities are also modeled and the related simulation results are discussed.

5.1 Simulation assumptions of the proposed TCSDM

Several behavioral simulations have been performed in MATLAB/SIMULINK in different cases to verify the performance of the proposed TCSDM in more details. According to (24), the effectiveness of the proposed TCSDM can be analyzed regarding to the several design parameters.

In all of the simulation steps, the TDC is an N-stage delay-based structure with the resolution of T_Q which is defined based on the characteristic of a 90 nm CMOS technology [8]. Three possible values of 50, 80, and 100 ps are selected for T_Q during the simulation procedure. To study the significance of the sampling frequency, the clock rate of the DEDFF-based TDC ($f_s = f_Q/2N$) is varied from 0.8 to 1.5 GHz according to the number of the TDC delay stages. Furthermore, the limit cycle frequency effect on the modulator spectral purity is also investigated. The validity of the noise-coupling technique is also elaborated via comparing the dynamic range of the NTF-enhanced second-order TCSDM with non-enhanced third-order one. The signal bandwidth of the modulator is chosen as 30 MHz and also the loop filter structure is a feedforward topology in all simulations.

5.2 Comparative simulation results

The simulated output spectrum and dynamic range of the non-enhanced 2nd and 3rd order TCSDM along with the NTF-enhanced 2nd order TCSDM for a −1.5 dBFS input signal is illustrated in Figs. 9 and 10, respectively. The associated system level parameters are also summarized in Table 1. As expected, the spectrum and the dynamic range of the NTF-enhanced 2nd order TCSDM is improved. As is clear there is an undistinguishable difference between the performance of the NTF-enhanced 2nd order and the non-enhanced 3rd order TCSDM. This confirms that the proposed noise-coupling technique is successful in improving the noise-shaping of the TCSDM by one order.

The SNDR of the proposed TCSDM across the input signal amplitude under the various cases is illustrated in Fig. 11 with the design parameters indicated in the related plots. These simulation results show that to achieve a higher dynamic range, one can make the resolution of the TDC finer. However, due to the technology limitations, it is not possible to decrease T_Q as much as desired. On the other hand, increasing the TDC stages can also be an improvement factor. But, this comes at the expense of the higher power consumption and larger silicon area. Although increasing the value of f_c may improve the dynamic range, as mentioned before, for the stability problem, the ratio of f_Q/Nf_c should be at least higher than 4, implying the upper limit for the limit cycle frequency. In a brief, the simulation results show that one can achieve the desired dynamic range by making a good compromise between the design parameters.

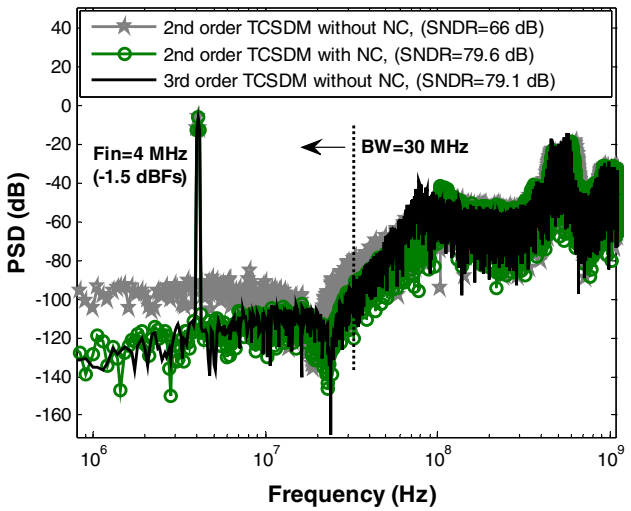

Fig. 9 Simulated PSD of the second- and third-order TCSDMs

6 Effect of the circuit non-idealities

The circuit non-idealities of the time-based quantizer are shaped by the loop filter. One of the main advantages of the sigma-delta modulators is that the design requirements of the amplifiers are relaxed thanks to the noise-shaping property. However, the effect of main circuit non-idealities such as the amplifier finite DC gain (A_v), unity gain bandwidth (GBW), and the clock-related problems such as the jitter and also the delay variation of the ELD compensation path can degrade the modulator performance. In this section, the non-idealities of various building blocks are examined and the dynamic range limitations are explored using the system level simulations.

6.1 Finite DC gain and limited gain bandwidth of the integrator amplifiers

The integrators shown in Fig. 6 can be implemented using active-RC or Gm-C structures. In our proposed macro-model utilized for simulation purposes, the active-RC implementation was assumed for all integrators. Typically, the required amplifier gain-bandwidth product (GBW) for

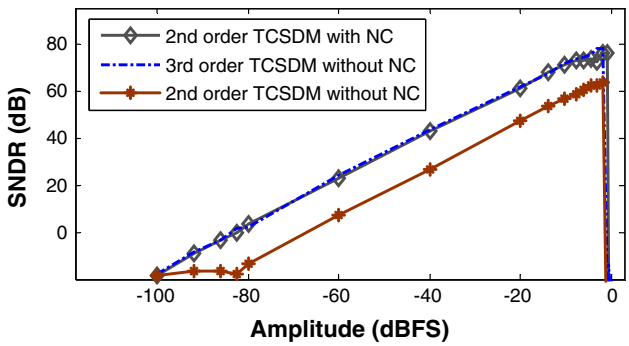

Fig. 10 Simulated SNDR versus the input signal amplitude

Table 1 TCSDM system level parameters for the simulation result in Fig. 9

Modulator structure	f_c (MHz)	A_1	A_2	A_3	$k_1 = k_2$	k_g	g	h	α	$\omega_p = \omega_b$ (Mrad/s)
2nd-order TCSDM without NC	500	0.76 f_c	1.61 f_c	–	1	1.6	0.046	0.1	1	$2\pi \times 50$
2nd-order TCSDM with NC	500	0.76 f_c	1.61 f_c	–	1	1.6	0.07	0.1	1	$2\pi \times 50$
3rd-order TCSDM without NC	500	2.14 f_c	0.917 f_c	0.47 f_c	1	1.7	0.22	0.1	1	$2\pi \times 50$

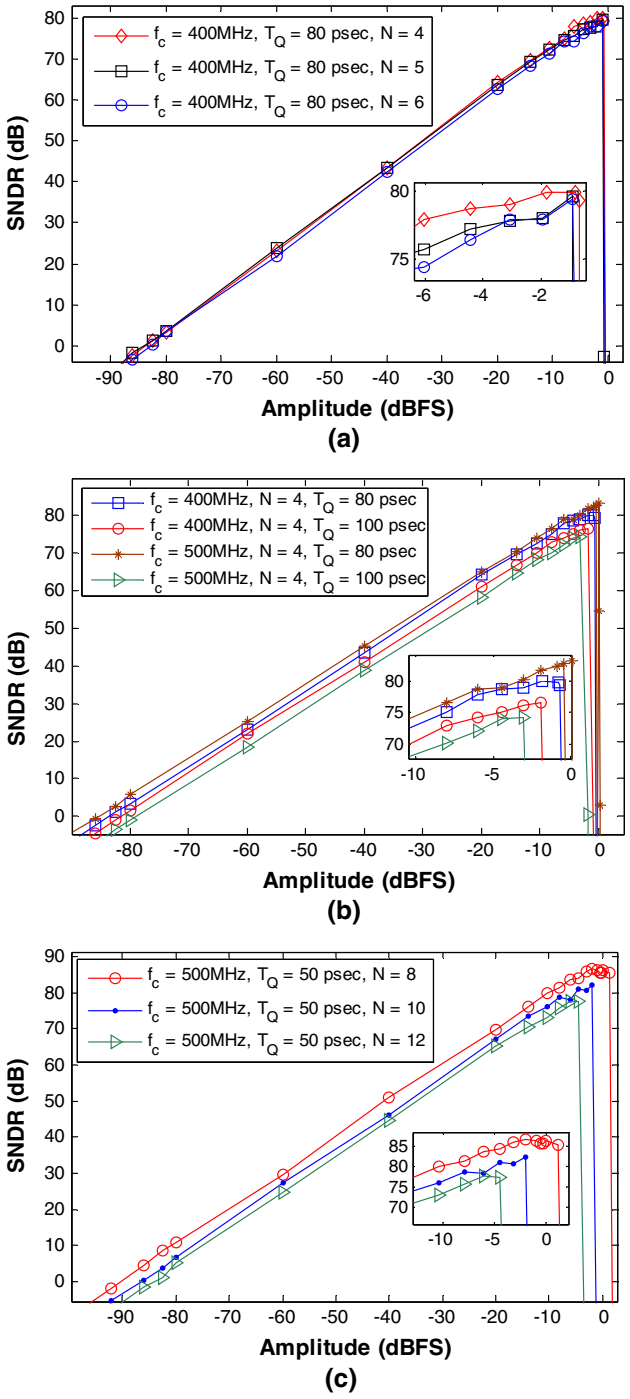

Fig. 11 Comparison of the SNDR versus the input signal of the proposed third-order TCSDM shown in Fig. 6 under the variation of the main design parameters ($f_s = 1/2N$ for all)

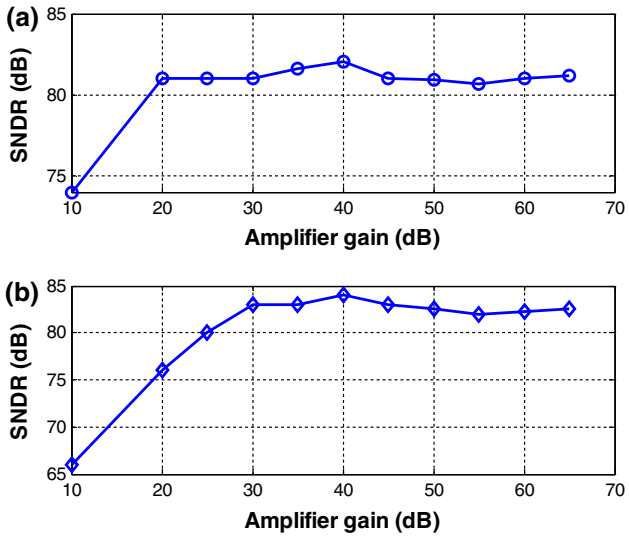

Fig. 12 Simulated SNDR for different DC gains of integrator amplifiers: **a** SNDR across A_{V1} while $A_{v2} = A_{v3} = 50$ dB, $A_{V4} = 25$ dB and $GBWs = 1$ GHz for all, and **b** SNDR across the first 3 amplifiers DC gains while $A_{V4} = 25$ dB and $GBWs = 1$ GHz for all

CT sigma-delta modulators is at least two times the sampling frequency.

The simulation results illustrated in Fig. 11 are obtained assuming infinite *GBW*s for all amplifiers. However, these results may be changed if the finite *GBW* amplifiers are considered for the integrators. The non-ideal integrator is modeled using the behavioral models introduced in [26]. Here, we assume the integrator amplifier as a first-order system denoted by $A(s) = A_v(\omega_{-3dB}/s + \omega_{-3dB})$, where A_v is the amplifier DC gain. Regarding the structure of the proposed TCSDM, $(L + 1)$ amplifiers may be needed in an Lth-order structure. The additional amplifier is used in the last summing node prior to the APWM.

In Fig. 12, the SNDR of a third-order NTF-enhanced TCSDM versus the DC gain variation of the first amplifier denoted as A_{v1} is depicted. In this simulation, the DC gain of the other amplifiers is also limited and it is assumed to be 50 dB for both A_{v2} and A_{v3} and 25 dB for A_{v4}. The variation of the SNDR across the GBW of the last amplifier is also illustrated in Fig. 13, while its DC gain is assumed to be $A_{v4} = 25$ dB. In this simulation, the GBW and DC gain of the other amplifiers are assumed as 40 dB and 1 GHz, respectively. Although the DC gain and noise

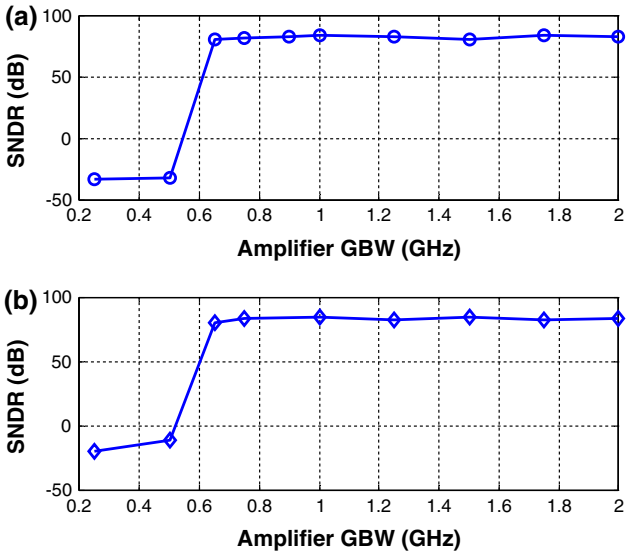

Fig. 13 Simulated SNDR for different *GBW*s of integrator amplifiers: **a** SNDR across GBW of the last integrator while $A_{v1} = A_{v2} = A_{V3} = 40$ dB, $A_{V4} = 25$ dB and $GBW_{1,2,3} = 1$ GHz, and **b** SNDR across the variation of the *GBW* of all integrators amplifiers while $A_{v1} = A_{v2} = A_{V3} = 40$ dB and $A_{V4} = 25$ dB

constraints of the summing amplifier are more relaxed, but its speed and slewing requirements are more severe than all due to its several input branches.

6.2 Delay variation of noise-coupling and ELD compensation paths

As discussed before, one of the most important parameters that can degrade the modulator performance is the excess loop delay. The main contribution of the ELD comes from the propagation delay in the TDC digital logic and the excess phase of the loop filter and the APWM. Considering the ELD, the loop filter should be redesigned to make the modulator stable. This requires an additional feedback path around the quantizer to ensure the controllability of the structure [18]. It is worth mentioning that one of the main drawbacks of the CT sigma-delta modulators are their sensitivity to the RC-product variations. The RC variation is mainly due to the various reasons (e.g. the process, temperature and power supply changes). As a result, usually the on-chip or even off-chip trimming circuits are considered to compensate for these variations.

As explained before, in the proposed modulator, the feedback delay blocks are realized through the passive LPFs where the time constants are determined by their RC product. The effect of the RC variation on the modulator performance is shown in Fig. 14. As it is seen, the degradation of the SNDR is negligible for an acceptable range of the delay variations confirming the robustness of the proposed modulator. Nonetheless, since the proposed

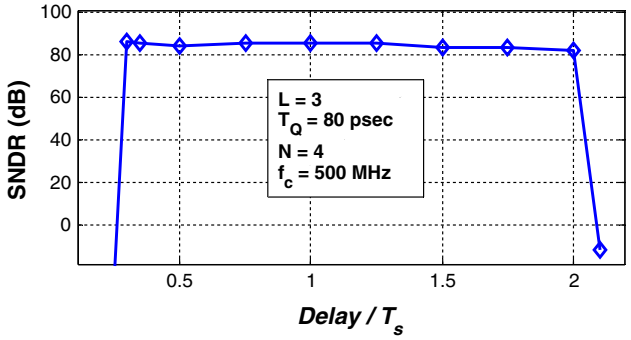

Fig. 14 Simulated SNDR under the delay variation of the ELD compensation and NC branches

modulator uses a CT structure, the trimming circuits are still needed in a real implementation.

6.3 Clock jitter

In a sigma-delta modulator, the clock jitter error at the quantizer input is also shaped. But, the jitter error in the main DAC is not shaped by the loop filter since it is directly appeared at the input. As a result, the clock jitter remains as one of the performance limiting parameters in CT sigma-delta modulators [18]. Clock jitter causes a slight random variation in the amount of the injected charge per clock cycle, and thus, adds a random phase modulation in the output bit stream. Due to this phase modulation, the out-of-band noise may be folded into the inband frequencies resulting in an increased noise floor and a degraded stability. This error can be modeled as a random phase modulation of the feedback pulses [18]. For a non-return-to-zero (NRZ) DAC, the error sequence can be written as:

$$\begin{aligned} e_j(n) &= [y(n) - y(n-1)]\,\Delta t_N = \Delta y\,\Delta t_N \\ \Delta t_N &= \frac{\Delta t(n)}{T_s}\ ; \quad \text{Normalized} \end{aligned} \tag{27}$$

where $y(n)$ is the amplitude of the modulator digital output, Δy is a discrete-time and discrete-amplitude signal which represents the variation of the DAC output at every clock cycle. $\Delta t(n)$ is the time deviation of the DAC pulse edge at the nth sample time which is assumed to be Gaussian with a variance of $\sigma^2_{\Delta t}$. From (27), $\sigma^2_{\Delta t}$ can be represented as:

$$\frac{\sigma^2_{\Delta t}}{T_s^2} = \frac{\sigma^2_{ej}}{\sigma^2_{\Delta y}} \tag{28}$$

For a sinusoidal input signal with the peak amplitude of A_p and assuming an NRZ voltage DAC, if the SNR in baseband is completely limited by the white jitter noise rather than the noise-shaped quantization noise, it can be written [18]:

$$P_j = \int_{-f_B}^{f_B} \frac{\sigma_{ej}^2}{f_s} |STF(f)|^2 \, df \approx \int_{-f_B}^{f_B} \frac{\sigma_{ej}^2}{f_s} \times 1 \, df = \frac{\sigma_{\Delta t}^2 \times \sigma_{\Delta y}^2}{T_s^2 \times OSR} \tag{29}$$

where P_j is the noise power accounts for the clock jitter. Regarding (29), the signal-to-jitter noise ratio (SNR_j) is obtained as:

$$SNR_j \triangleq \frac{P_s}{P_j} = 10 \log \frac{A_p^2/2}{\left\{\frac{\sigma_{\Delta t_N}^2 \times \sigma_{\Delta y}^2}{OSR}\right\}} \tag{30}$$

The relations approximated in (29) and (30) are for conventional voltage-based quantizers. But, in the proposed architecture where the TDC-based quantizer is utilized, the result may be to some extent different from those mentioned above. Since the TDC outputs are merged by a DTC, some jitter rejection may be expected. In other words, since both the rising and falling edges of the feedback pulse denoted as $p_q(t)$ carry approximately the same time shift due to the clock jitter within a clock period, the clock jitter affects only the position of the feedback pulse and the pulse width remains approximately unchanged. The effect of random pulse position modulation of a PWM waveform is cumbersome to analyze with equations [8]. Thus, the necessary insight can be achieved through simulations. The SNDR limitation due to the clock jitter using the model introduced in [27] is plotted in Fig. 15 where the clock jitter is modeled as an additive Gaussian noise. A significant robustness of the SNDR is achieved in the proposed TCSDM compared to the conventional CT sigma-delta modulators such as [18]. This superiority is obtained thanks to the invariance of the pulse width in the presence of clock jitter and also due to utilizing of an LPF in the feedback path of the modulator.

6.4 TDC/DTC non-ideality

Due to the important role of the TDC/DTC in the proposed modulator, the non-ideality of this block can be a critical point. The main non-ideality of this block can be attributed to the non-accurate TDC delay units, T_Q. As depicted in Fig. 8, the input of the TDC/DTC is a two-level signal denoted as $p(t)$ and its quantized output signal is $p_q(t)$.

It can be stated that the TDC/DTC works properly if the quantization error signal, $e(t) = p(t) - p_q(t)$, is produced in any condition as shown in Fig. 8(b). The area under the error signal is denoted as the quantization noise power. If for any reason such as the significant variation of T_Q or the malfunctioning of the flip-flops, the error signal is not produced or its area deviates significantly from its ideal case, then we can say the TDC/DTC does not work properly. In this case, the modulator may be unstable. In order to study this condition, the SNDR of the TCSDM with $L_{NC} = 4$ against the variation of the TDC delay units is plotted in Fig. 16 for two different cases. The good robustness of the performance against the reasonable variation of the delay units confirms the effectiveness of the proposed modulator.

Furthermore, the circuit-level implementation of the TDC/DTC is provided using TSMC 90 nm CMOS technology in order to perform the Monte–Carlo simulations. The achieved results are depicted in Fig. 17. Figure 17(a) shows the variation of the error signal and Fig. 17(b) illustrates the area under the error signal for 1000 iterations. As it is clear, the variation of the error signal is negligible and also the variance of the histogram is very small. This verifies the robustness of the proposed modulator against the TDC/DTC non-ideality.

7 Comparative points of the proposed TCSDM

Practical design limitations of the conventional voltage-based sigma-delta modulators made us to propose a time-based modulator to better exploit the potential of the CMOS technology scaling. As discussed, the noise-shaping order of the proposed TCSDM using an *Lth*-order loop filter is enhanced by one by using the noise-coupling in time

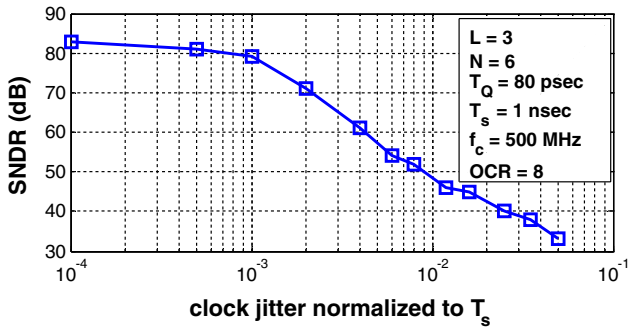

Fig. 15 Simulated SNDR versus the clock jitter

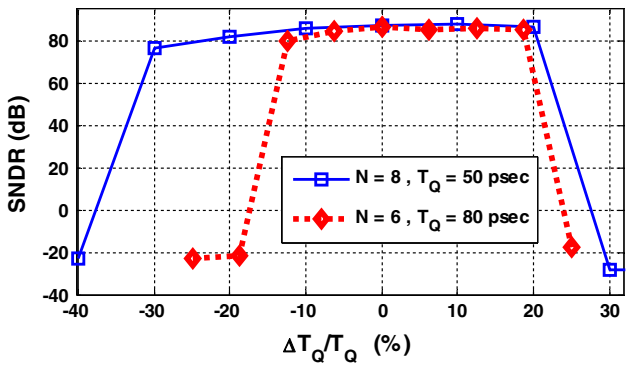

Fig. 16 SNDR under the variation of the TDC delay units (T_Q) for a noise-coupled 3rd order TCSDM in two different cases

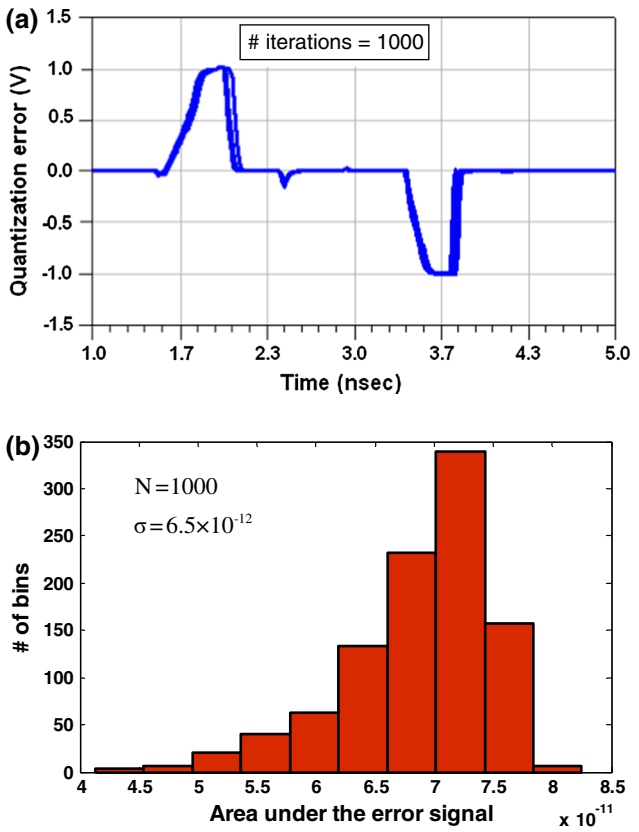

Fig. 17 Monte–Carlo simulation for the circuit-level implementation of the TDC/DTC: **a** one section of the error signal, and **b** histogram of the area under the error signal

domain. Although the clock rate of the proposed time-based quantizer is similar to that of the conventional voltage-based structures, its elements can be implemented using digital circuits offering a significant superiority from the point of speed, power dissipation, and programmability view.

A serious problem of the modulators with multi-bit output is the inherent nonlinearity of the multi-bit feedback DAC. This nonlinearity directly appears at the input of the modulator without any shaping. Although this severe problem may be relaxed by using the dynamic element matching (DEM) techniques, but these techniques are not efficient for low OSR CT sigma-delta modulators [28]. In contrast, in the proposed TCSDM, thanks to the combination of the TDC and DTC, the feedback signal is a two-level single bit while the output of the TDC is still multi-bit. Therefore, a single bit DAC is needed which is inherently linear.

Furthermore, the clock jitter immunity of the proposed TCSDM is much better than that of the conventional voltage-based structures. This is achieved by merging the TDC output signal with a DTC and generating a two-level bit stream whose width is approximately remains unchanged under the existence of the clock jitter.

As a comparison, the fabricated third-order CT sigma-delta modulator in [8] is considered. It employs a synchronous PWM and a delay-line-based 4-bit TDC with $N = 50$. It consumes 10.5 mW power from a 1.2 V power supply at 250 MHz sampling frequency and achieves 60 dB SNDR in 20 MHz bandwidth. The reported figure of merit (FoM = power/2 × BW × 2^{ENOB}) is 319 fJ/conversion-step. Although this small FoM shows the superiority of this work over the comparable voltage-mode CT sigma-delta modulators, the power consumption is still high owing to the complexity of 50-stage TDC. In contrast, the proposed TCSDM requires much less TDC quantization levels making it more beneficial from the point of power consumption. On the other hand, the proposed quantizer utilizes a noise-coupling technique which can achieve the same degree of noise-shaping reported in [8] with only two integrators resulting in more power saving. Thus, if the proposed noise-coupling quantizer is used in the modulator of [8], the modulator's FoM may be improved.

8 Conclusion

In this paper, an NTF-enhanced CT sigma-delta modulator using a digital friendly time-based approach is proposed. The proposed TCSDM exploits an APWM as the voltage-to-time conversion (VTC) and a TDC as the time quantizer in its loop. A combination of the TDC with a DTC gives the possibility of producing a single bit feedback signal. A novel realization of the noise-coupling technique in time domain is introduced to enhance the noise-shaping order. This is achieved without any stability degradation and also adding a significant hardware. Furthermore, by combining the TDC and DTC, the robustness of the proposed modulator against the clock jitter is improved due to the invariance of the feedback pulse widths. Simulation results taking into the consideration of both ideal and non-ideal blocks confirm the effectiveness of the proposed NTF-enhanced TCSDM.

References

1. Mitteregger, G., Ebner, C., Mechnig, S., Blon, T., Holuigue, C., & Romani, E. (2006). A 20-mW 640-MHz CMOS continuous-time ADC with 20-MHz signal bandwidth, 80-dB dynamic range and 12-bit ENOB. *IEEE Journal of Solid-State Circuits, 41*(12), 2641–2649.
2. Fei, Y. (2014). Design techniques for time-mode noise-shaping analog-to-digital converters: a state-of-the-art review. *Analog Integrated Circuits and Signal Processing, 79*, 191–206.
3. Straayer, M., & Perrott, M. H. (2009). A multi-path gated ring oscillator TDC with first-order noise shaping. *IEEE Journal of Solid-State Circuits, 44*(4), 1089–1098.

4. Pakniat, H., & Yavari, M. (2013). A time-domain noise-coupling technique for continuous-time sigma-delta modulators. *Analog Integrated Circuits and Signal Processing, 78*, 439–452.
5. Iwata, A. (1999). The architecture of delta sigma analog-to-digital converters using a VCO as a multi bit quantizer. *IEEE Transactions on Circuits and Systems-II: Express Briefs, 46*(8), 941–945.
6. Li, G., Tousi, Y., Hassibi, A., & Afshari, E. (1999). Delay-line-based analog-to-digital converters. *IEEE Transactions on Circuits and Systems-II: Express Briefs, 56*(6), 464–468.
7. Straayer, M. Z., & Perrott, M. H. (2008). A 12-bit, 10-MHz bandwidth, continuous-time ΔΣ ADC with a 5-bit, 950-MS/s VCO-based quantizer. *IEEE Journal of Solid-State Circuits, 43*(4), 805–814.
8. Dhanasekaran, V., Gambhir, M., Elsayed, M. M., Sanchez-Sinencio, E., Silva-Martinez, J., Mishra, C., et al. (2011). A continuous-time multi-bit ΔΣ ADC using time domain quantizer and feedback element. *IEEE Journal of Solid-State Circuits, 46*(3), 639–650.
9. Lee, K., Bonu, M., & Temes, G. C. (2006). Noise-coupled delta-sigma ADCs. *Elect. Letters, 42*(3), 1381–1382.
10. Wang, Y., & Temes, G. C. (2009). Noise-Coupled continuous-time delta-sigma ADCs. *Electronics Letters, 45*(6), 302–303.
11. Roza, E. (1997). Analog-to-digital conversion via duty-cycle modulation. *IEEE Transactions on Circuits and Systems-II: Express Briefs, 44*(11), 907–914.
12. Daniels, J., Dehaene, W., Steyaert, M., & Wiesbauer, A. (2010). A/D conversion using asynchronous ΣΔ modulation and time-to digital conversion. *IEEE Transactions on Circuits and Systems-I: Regular Papers, 57*(9), 2404–2412.
13. Weibo, L., Orino, Y., Shinnosuke, H., & Minoru, K. K. (2013). Design of a self-oscillating PWM signal generator with a double integration loop. *IEEE Transactions on Circuits and Systems-I: Regular Papers, 60*(8), 2064–2073.
14. Gelb, A., & Velde, W. V. (1968). *Multiple-input describing functions and non-linear system design*. New York: McGraw-Hill.
15. Wang, Z. (1991). CMOS adjustable Schmitt trigger. *IEEE Transactions on Instrumentation Measurement, 40*(3), 601–605.
16. Katyal, V., Geiger, R., & Chen, D., (2014). Adjustable hysteresis CMOS Schmitt trigger. In *Proceedings of the IEEE International Symposium Circuits Systems* (pp. 1938–1941).
17. Jingxue, L., & Ranjit, G. (2011). Design and Analysis of a self-oscillating class D audio amplifier employing a hysteretic comparator. *IEEE J Solid-State Circuits, 46*(10), 2336–2349.
18. Cherry, J. A., & Snelgrove, W. M. (1999). *Continuous-time delta-sigma modulators for high-speed A/D conversion*. Dordrecht: Kluwer Academic Publisher.
19. Vuyst, B. D., & Rombouts, P. (2011). A 5-MHz 11-bit self oscillating ΣΔ modulator with a delay-based phase shifter in 0.025 mm^2. *IEEE J Solid-State Circuits, 46*(8), 1919–1927.
20. Hernandez, L., & Prefasi, E. (2008). Analog to digital conversion using noise shaping and time encoding. *IEEE Transactions on Circuits Systems I, Regular Papers, 55*(8), 2026–2037.
21. Lin, Y., & Ismail, M. (2012). Time-based all-digital sigma-delta modulators for nanometer low voltage CMOS data converters. *Analog Integrated Circuits and Signal Processing, 73*, 801–808.
22. Roberts, G. W., & Ali-Bakhshian, M. (2010). A brief introduction to time-to-digital and digital-to-time converters. *IEEE Transactions on Circuits and Systems-II: Express Briefs, 57*(3), 153–157.
23. Ortmanns, M., & Gerfers, F. (2005). *Continuous-time sigma-delta A/D conversion*. Berlin/Heidelberg: Springer.
24. Schreier, R., & Temes, G. C. (2005). *Understanding delta-sigma data converters*. Wiley/IEEE Press: Piscataway.
25. Hamoui, A., & Martin, K. W. (2004). High-order multi-bit modulators and pseudo data-weighted-averaging in low-oversampling ΣΔ ADCs for broad-band applications. *IEEE Transactions on Circuits and Systems-I: Regular Papers, 51*(1), 72–85.
26. Malcovati, P., Brigati, S., Francesconi, F., Maloberti, F., Cusinato, P., & Baschirotto, A. (2003). Behavioral modeling of switched-capacitor sigma-delta modulators. *IEEE Transactions on Circuits and Systems-I: Regular Papers, 50*(3), 352–364.
27. Ashry, A., & Aboushady, H. (2009). Fast and accurate jitter simulation technique for continuous-time ΣΔ modulators. *Electronics Letters, 45*(24), 1218–1219.
28. Baird, R. B., & Fiez, T. S. (1995). Linearity enhancement of multi-bit ΔΣ A/D and D/A converters using data weighted averaging. *IEEE Transactions on Circuits and Systems-II: Express Briefs, 42*(12), 753–762.

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