A Linear Wideband CMOS Balun-LNA with Balanced Loads

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***Abstract*— This paper presents a novel structure on balun-LNAs which has a differential output with symmetric loads without any need for current bleeding circuit. The proposed structure is based on the common-gate (CG) common-source (CS) cascode LNA with identical transconductances for the CG and CS stages using a positive feedback for input matching compensation. This paper also introduces a new linearity improvement technique based on post distortion and derivative superposition linearization techniques without affecting the input impedance matching condition or requiring considerable power overhead. By this way, despite other linearity improvement techniques, the voltage gain not only is not decreased but is also improved. The proposed balun-LNA structure is designed in a 65 nm CMOS technology and covers the frequency range of 0.47-3.3 GHz. It has symmetrical loads with the maximum S_{21} of 22 dB and a minimum noise figure (NF) of 2.57 dB. The achieved third-order input intercept point (IIP3) and second-order input intercept point (IIP2) are about +2.81 dBm and 29.27 dBm, respectively. The circuit consumes 8.33 mA from a nominal supply voltage of 1.5 V, and excluding the pads, it occupies 0.057 mm^2 silicon die area.**

***Index Terms*— CMOS Balun-LNA, positive feedback, linearity improvement, symmetrical loads.**

I. Introduction

LOW-NOISE amplifier (LNA) is the first active block in wireless receivers, which is needed to amplify the received signal from the antenna without adding much noise to it. LNAs should also provide good input impedance matching, sufficient and flat gain, high linearity, and low noise figure (NF) over the desired bandwidth. Among different LNAs, balun-LNAs have become more demanding during the past decades since they provide a differential output, which leads to have higher common-mode rejection ratio (CMRR) and lower second-order distortion, without any need for a passive balun that has loss and takes up a large space increasing the cost.

In recent studies, several broadband active balun-LNAs have been reported. The basic common-gate common-source (CG-CS) balun-LNA is presented in [1], in which the CG transistor provides the input impedance matching and the CS transistor cancels the noise and distortion generated by the CG transistor while providing a differential output. To reduce the NF of the balun-LNA, the noise of the CS transistor should be decreased since in this structure, the NF is almost determined by the CS transistor. By increasing the size and the transconductance of the CS transistor, its noise contribution is highly decreased. Fig. 1(a) shows the proposed structure in [2] in which the size of the CS transistor is N times larger than that of the CG transistor resulting in reduced NF compared to [1]. In [2], to have a differential output, the load resistor in CS stage should be N times smaller than the load resistor of the CG stage. This leads to a mismatch in phase and gain of the differential output nodes, and hence, increases the second-order distortion and makes the noise-cancellation less perfect. Moreover, this structure suffers from high power consumption due to the large current of CS stage.

A local feedback is used in [3] between the CG and CS stages to boost the transconductance of the CG transistor and reduce the power consumption. Nonetheless, this structure suffers from the gain and phase mismatches in differential output nodes owing to the asymmetrical load resistors. In [4], a balun-LNA with balanced loads has been introduced which is shown in Fig. 1(b). In this structure, a modified current bleeding technique is employed to have the same current at differential output branches. As a result, the LNA has symmetrical loads and a differential output without any phase or gain imbalances. Nonetheless, this structure suffers from high power consumption like [2] and also needs a large power supply voltage. In [5], the structure presented in [4] is improved by boosting the transconductance of the CG stage using a local feedback, as it implies the current bleeding circuit, to decrease the power consumption and also mitigate the supply voltage requirement. In addition, the cross-coupled cascode stage is utilized to improve the gain and phase mismatches at the differential output. In [6], a new current bleeding circuit has been proposed where pMOS transistors are used instead of nMOS transistors to decrease the effect of the current bleeding circuit's resistance on V_{out-}. In [7], a dual-loop feedback with an active combiner is utilized for providing wideband input matching with power efficiency. It also uses a multi-gated transistor to compensate the nonlinearity of the main CS stage.

This brief introduces a balun-LNA with symmetrical loads without using any current bleeding circuit, which makes the design of the LNA challenging. A novel linearity improvement technique is also introduced which improves the third-order input intercept point (IIP3) and voltage gain simultaneously with consuming negligible additional current since it works in the weak inversion region. The proposed

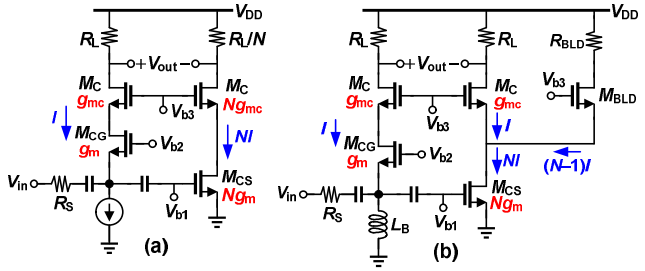

Fig. 1: (a) Conventional CG-CS balun-LNA topology [2] and (b) balun-LNA with a modified current bleeding technique and balanced loads [4].

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linearity enhancement technique is based on post distortion and derivative superposition linearization methods.

The rest of the paper is organized as follows. Section II describes the structure of the proposed balun-LNA in details. Section III provides the post-layout simulation results, and finally, Section IV provides the conclusion.

II. Structure of The Proposed Balun-LNA

The schematic of the proposed balun-LNA is depicted in Fig. 2. The purpose of this structure is having symmetrical loads without using any additional current bleeding circuit which its current control is challenging. For having balanced loads without any current bleeding circuit, the current and transconductance of both CG and CS stages should be identical. However, designing a balun-LNA in which the transconductance of both CG and CS stages is the same is very challenging because of the following reasons. The transconductance of the CS transistor should be large as mentioned in Section I to achieve low NF. On the other hand, the transconductance of the CG transistor should be 20 mA/V owing to the input impedance matching condition. To overcome this challenge and satisfying the input matching condition, this paper employs a positive feedback (M_F) transistor to compensate the input matching and allow the CG transistor to have a larger transconductance [8]. Under this condition, the transconductance of both CG and CS transistors can be identical and high enough to reduce the NF. As a result, a differential output with symmetrical resistor loads can be achieved. In Fig. 2, $M_{C1,2}$ cascode transistors are employed to improve the input-output isolation and LNA stability. $M_{a1,2}$ transistors are biased in weak inversion region to improve the linearity which improves the voltage gain of the LNA at the same time while consuming negligible current. The L_B is an external RF chock that places the source of the CG transistor (M_{CG}) at dc ground. The details of the input impedance matching condition, voltage gain, NF, and linearity of the proposed balun-LNA are presented in the following.

A. Input Impedance Matching

It can be shown that the following condition is needed to provide the input impedance matching:

$$R_S = \frac{1}{g_{m,CG} - g_{m,F}(g_{m,CG}R_L - 1)} \quad (1)$$

where R_S is the source impedance, $g_{m,CG}$ and $g_{m,F}$ are the transconductance of the CG and positive feedback (M_F) transistors, respectively, and R_L is the symmetrical load resistor. As it is seen, by using the positive feedback transistor, another degree of freedom is added to the input matching condition to allow the CG transistor to have large transconductance, which would be identical to the CS branch.

B. Voltage Gain

Without using linearity improvement transistors ($M_{a1,2}$), under the input matching condition, and by neglecting the drain-source resistance of MOS transistors, the voltage gain of the proposed LNA is obtained as follows.

$$A_v = (g_{m,CG} + g_{m,CS})R_L/2 \quad (2)$$

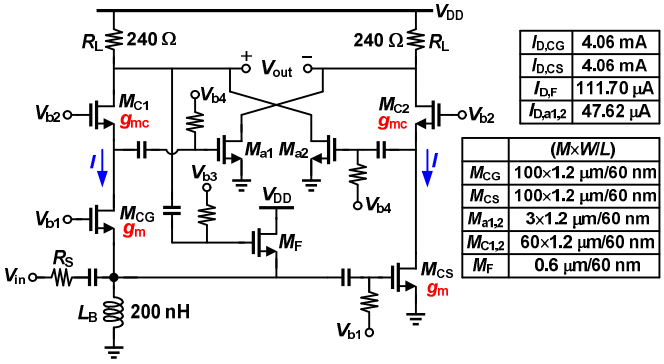

Fig. 2: Proposed CMOS balun-LNA.

where $g_{m,CG}$ and $g_{m,CS}$ are the transconductance of the CG and CS transistors, respectively. The differential outputs are balanced when $g_{m,CG} = g_{m,CS} \equiv g_m$. This condition is also needed to cancel the thermal noise effect of CG transistor at differential output. Therefore, with considering this condition, the voltage gain of the proposed LNA without $M_{a1,2}$ transistors is simplified as $A_v = g_m R_L$.

After adding linearity improvement $M_{a1,2}$ transistors, the differential voltage gain is obtained as

$$A_v = g_m\left(1 + g_{m,a}/g_{m,c}\right)R_L \quad (3)$$

where g_m is the identical transconductance of M_{CG} and M_{CS} transistors. $g_{m,a}$ and $g_{m,c}$ are the transconductance of $M_{a1,2}$ and $M_{C1,2}$ transistors, respectively. According to (3), $M_{a1,2}$ transistors can increase the voltage gain of the proposed balun-LNA because they add another positive term to the voltage gain relation. In the design of the proposed balun-LNA, voltage gain is improved about 10% (0.8 dB) by selecting the size of the cascode transistors 60% that of the CG and CS transistors in order to increase the effect of $M_{a1,2}$ transistors in gain improving.

C. Noise Analysis

As mentioned before, the noise generated by the CG transistor can be totally cancelled at the differential output when the input impedance matching and differential output balance conditions are met. The noise generated by cascode transistors is negligible because most of their noise is rotated in their loops and does not appear at the output. The noise effect of $M_{a1,2}$ transistors can be neglected due to their very small size. Therefore, the noise factor of the proposed balun-LNA is almost determined by the CS stage, positive feedback transistor, and load resistors. It is calculated as:

$$NF = 1 + \frac{\gamma}{g_m R_s} + \gamma g_{m,F} R_s + \frac{1}{g_m^2 R_L R_s} + \frac{(1 + g_m g_{m,F} R_L R_S)^2}{g_m^2 R_L R_s} \quad (4)$$

The second and third terms of (4) stand for the thermal noise of M_{CS} and M_F transistors, respectively, and the fourth and fifth terms represent the thermal noise of R_L at the differential output nodes. It is worth mentioning that the noise of the R_L does not appear at the differential output identically owing to the effect of the positive feedback transistor. According to (4), the NF can be decreased by increasing the amount of load resistors and CS transistor's transconductance, and decreasing the positive feedback's transconductance.

D. Linearity Analysis

The linearization technique introduced in this paper is based on the mixture of two post distortion and derivative superposition linearization methods. In the derivative superposition method, the linearity improvement transistor is biased in the weak inversion region, and it is placed in parallel with the input transistor [9]. Since the input transistor is in the saturation region and the linearity improvement transistor is in the weak inversion region, the sign of the second-order derivative transconductance (g_m'') is opposite in these two transistors. As a result, the total g_m'', which is the sum of the g_m'' of the main and linearity improvement transistors, is zero in one interval by properly designing of the aspect ratio and bias of the linearity improvement transistors. Hence, this method can improve the linearity of the circuit by removing the third-order intermodulation component. One of the advantages of this linearity technique is its low power consumption since the linearity improvement transistor is biased in weak inversion region. But this technique affects the input impedance matching of the LNA because the linearity improvement transistor is located at the input of the LNA.

In the post distortion linearity improvement technique, the linearity improvement transistor is biased in the saturation region, and it is placed at the output of the main transistor [9]. One of the advantages of this technique is that it does not affect the input matching because the linearity improvement transistor is not placed at the input of the LNA. However, in this technique, the LNA voltage gain is reduced due to the $1/g_{m,a}$ impedance which is added by the linearity improvement transistor at the output of the main transistor and this effect is exacerbated when the transconductance of this linearity improvement transistor is increased. In addition, in this method, the power consumption is higher than the derivative superposition technique owing to the biasing of the linearity improvement transistor in the saturation region. In [10], a new linearization method is proposed to simultaneously improve the IIP3 and voltage gain by utilizing two cross-coupled diode-connected pMOS transistors at the cascode nodes which cancel out the nonlinearity of input pairs.

In the proposed linearization scheme in this paper, which is shown in Fig. 2, $M_{a1,2}$ linearity improvement transistors are placed at the output of the main transistors like the post distortion method, and they are biased in weak inversion region like the derivative superposition technique. Therefore, it does not affect the input impedance matching and results in less power consumption. As a result, by using the proposed linearization method, not only do we have the advantages of the two post distortion and derivative superposition linearization methods, their side effects are also alleviated, and the voltage gain of the LNA is simultaneously improved. In comparison with [10], in the proposed scheme, the linearity improvement transistors are nMOS and their drains are directly connected to output nodes instead of the cascode nodes in order to cancel out the total nonlinearity of input and cascode transistors, together, at the output, and this is one of the advantages of the proposed linearity improvement technique over [10].

In order to investigate the proposed technique in improving the linearity and voltage gain, the current of the negative output branch in Fig. 2 is given by:

$$i_{out-} = i_{CS} + i_{a1} \tag{5}$$

where i_{CS} and i_{a1} are the currents of the M_{CS} and M_{a1} transistors, and under the input impedance matching condition, they can be written as below.

$$i_{CS} = g_m \frac{v_{in}}{2} + g_m' \frac{v_{in}^2}{4} + g_m'' \frac{v_{in}^3}{8} \tag{6}$$

$$i_{a1} = g_{m,a} v_1 + g_{m,a}' v_1^2 + g_{m,a}'' v_1^3 \tag{7}$$

where v_1 is the source voltage of the M_{C1} transistor. The v_1 voltage can be obtained in terms of v_{in} by writing another KCL at the source voltage of the M_{C1} transistor as follows.

$$v_1 = \frac{g_m}{g_{m,c}} \frac{v_{in}}{2} + \frac{g_m'}{g_{m,c}} \frac{v_{in}^2}{4} + \frac{g_m''}{g_{m,c}} \frac{v_{in}^3}{8} \tag{8}$$

By inserting v_1 from (8) in (7), i_{a1} can be obtained in terms of v_{in} as well. Hence, the current of negative output branch is obtained in terms of v_{in}. The current of positive output branch can also be obtained similarly. By subtracting i_{out-} from i_{out+}, the differential output current is acquired as follows.

$$\begin{aligned} i_{out} &= i_{out+} - i_{out-} = -g_m \left(1 + g_{m,a} / g_{m,c}\right) v_{in} \\ &- \left[\frac{g_m''}{4} \left(1 + \frac{g_{m,a}}{g_{m,c}} \right) + \frac{g_m g_{m,a}' g_m'}{2 g_{m,c}^2} + \frac{g_m^3 g_{m,a}''}{4 g_{m,c}^3} \right] v_{in}^3 \end{aligned} \tag{9}$$

According to relation (9), by biasing $M_{a1,2}$ transistors in the weak inversion region, the sign of $g_{m,a}''$ will be positive while the sign of g_m'' is negative. As a result, it is possible to reduce the third-order intermodulation term, and hence, to improve the IIP3. In addition, the first term in (9), which is the linear component of the current, shows that the voltage gain is also increased by adding the linearity improvement transistors. It is also noteworthy to mention that by subtracting i_{out-} from i_{out+}, the second-order intermodulation term is eliminated from the differential output current. So, adding $M_{a1,2}$ transistors has no effect on the second-order intermodulation at the differential output current. According to the post-layout simulation results, which are presented in the next section, the proposed linearization technique improves the value of IIP3 of the proposed LNA 5.22 dB with only 95.24 μA additional current consumption. It also enhances the voltage gain of the LNA by the amount of 0.8 dB (10%).

III. Simulation Results

The proposed balun-LNA is designed for wideband receivers covering the frequency range of 0.5-3 GHz. In the design of the CG, CS, and positive feedback transistors, it is considered to meet the input impedance matching condition and in the meantime having the lowest noise figure with considering the limitation of power consumption and voltage headroom. The size of the cascode transistors is selected sixty percent that of the CG and CS transistors to increase the effect of $M_{a1,2}$ transistors in gain improving, as it can be seen in (3). The bias and size of $M_{a1,2}$ transistors are selected by considering the following conditions. First, to maintain in the

weak inversion region, their bias voltage should be a little below the threshold voltage but not too small to prevent entering the cut-off region. Second, for having low NF, the size of these transistors should be as low as possible. Third, based on the IIP3 improvement condition, the g_m'' of these transistors should cancel out the g_m'' of main transistors in the desired bandwidth. Hence, the bias voltage about 350 mV and aspect ratio of 3×1.2 µm/60 nm is selected for $M_{a1,2}$ transistors based on considering three above-mentioned conditions.

It is also worth mentioning that in the proposed balun-LNA in Fig. 2, a wide-swing cascode current mirror is utilized to bias the main CG, CS, and cascode transistors (V_{b1} and V_{b2}) and two simple current mirrors are used to bias the positive feedback and linearity improvement transistors (V_{b3} and V_{b4}).

The aspect ratio and bias current of the transistors is also shown in Fig. 2. The circuit level post-layout simulations of the proposed balun-LNA are carried out with Spectre RF using a 65 nm RF-CMOS technology with 1.5 V supply voltage. Fig. 3(a) shows the layout of the proposed balun-LNA. In this design, poly resistors and metal-insulator-metal (MIM) capacitors are used to realize the required resistors and capacitors, respectively. The simulated NF, S_{21}, and S_{11} in different process corner cases, supply voltage and temperature (PVT) variations are depicted in Fig. 3(b) and Fig. 4. According to these figures, over the whole frequency range of 0.47-3.3 GHz, the NF of the proposed balun-LNA is below 3.5 dB with the minimum of 2.57 dB, input matching is totally established, and the S_{21} is higher than 19.45 dB with the maximum of 22 dB in all process corner cases.

Fig. 5(a) illustrates the simulated K_f and Δ stability factors. Since K_f is larger than 1 and the magnitude of Δ is less than 1 over a large frequency range, the proposed LNA is unconditionally stable. Fig. 5(b) illustrates how the cancelation of second-order derivative superposition terms happens by biasing input and linearity improvement transistors in different regions and carefully selecting their bias voltage. The main and IM3 curves and also the IIP3 value versus the input signal frequency with 10 MHz spacing are shown in Fig. 6(a) and Fig. 6(b), respectively. As it is seen, the IIP3 has a positive amount in the whole frequency range. Fig. 6(c) and Fig. 6(d) show Monte Carlo simulation results of IIP3 before and after adding $M_{a1,2}$ transistors with the main RF tone at 1 GHz and 10 MHz spacing. As it is seen, the proposed idea has improved the IIP3 by the amount of 5.22 dB.

The main and IM2 curves and the Monte Carlo simulated IIP2 of the proposed balun-LNA are shown in Fig. 7 with the main RF tone at 1 GHz with 10 MHz spacing. As it is seen, the proposed balun-LNA has a high IIP2 for having symmetrical loads and identical transconductances for both CG and CS stages.

Table I summarizes the post-layout simulation results of the proposed balun-LNA in PVT conditions. As it is clear, the proposed LNA is well robust against PVT variations. Table II represents a comparison between the proposed balun-LNA and some of the previous wideband balun-LNAs. According to Table II, the proposed structure has a much higher linearity than the previous structures, with almost the same or even lower NF, and is the only balun-LNA with symmetrical loads that has positive IIP3 introduced so far. In comparison with [16] which has introduced an inverter-based shunt-feedback balun-LNA, the proposed balun-LNA has the advantage of having symmetrical loads and also a 6.51 dB higher IIP3. Compared to [4, 5, 12] which are all balun-LNAs with balanced loads, the proposed balun-LNA has a higher BW, higher IIP3, and lower power consumption than [4, 12] and about 5 dB higher IIP3 than [5]. Compared to [13] which has a positive IIP3, the proposed structure not only has the advantage of having balanced loads, but also a lower NF (about 1.2 dB) and higher bandwidth.

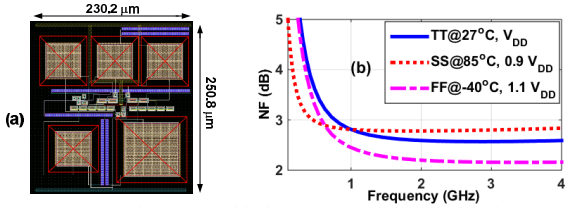

Fig. 3: (a) Layout of the proposed balun-LNA, and (b) simulated NF.

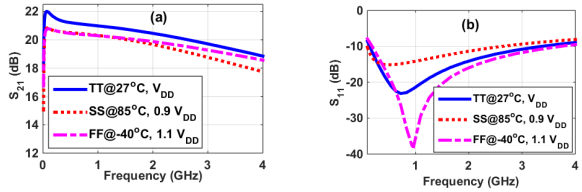

Fig. 4: Simulated (a) S_{21}, and (b) S_{11} of the proposed balun-LNA.

Table II: Performance comparison with several wideband CMOS balun-LNAs.

Reference	CMOS Process	V_{DD} (V)	Frequency (GHz)	S_{21} (dB)	S_{11} (dB)	NF (dB)	IIP3 (dBm)	IIP2 (dBm)	Symmetric load	Power (mW)	Area (mm^2)	FoM (dB)
JSSC'08 [2]	65 nm	1.2	0.2-5.2	13-15.6	<-12	2.9-3.5	0	>20	No	21	0.01	9.59
TCAS-I'10 [3]	130 nm	1	0.2-3.8	16-19[b]	<-9	2.8-3.4	-4.2	-	No	5.7	0.025	13.24
TMTT'10 [12]	130 nm	1.2	0.05-0.86	17-18[b]	<-11	2.5-3	-0.5	29.5	Yes	30	0.042	2.90
TMTT'12 [13]	130 nm	1.2	0.1-2	13.6-16.6	<-10	3.8-5	0.5	24	No	3	0.075	13.66
MWCL'14 [14]	180 nm	1.8	DC-1.4	15-16.4	<-12	3-4[b]	-13.3	11	No	12.8	0.038	-6.49
ELL'16 [11]	180 nm	1.8	0.01-1.7	16.7-19.7	<-10	1.93-2.8	1.13	-	No	25.2	0.092	11.62
TCAS-I'19 [4]	65 nm	2.2	0.05-1	24-30	<-12	2.3-3.3	-4.1	20.6	Yes	19.8	0.045	14.27
AEUE'19 [15]*	180 nm	1.2	0.18-2	15-20.8	<-8	2.65-3.8	-4.91	28.57	No	4.9	0.04	12.34
TCAS-I'20 [5]	65 nm	1	0.05-1.3[b]	24-27.5[b]	<-12	2.3-3[b]	-2.2[b]	19.6[b]	Yes	5.7	0.046	20.27
RFIC'20 [16]*	28 nm	1	6-10	20-23	<-10	Min: 2.4	-3.7	-	No	7.4	-	17.95
TCAS-II'21 [17]	180 nm	1.8	0.13-0.93	16.6-19.6	<-10	3.6-5	-8.5	>12	No	3	0.18	4.25
This Work*	65 nm	1.5	0.47-3.3	19.45-22	<-10	2.57-3.5	+2.81	29.27	Yes	12.5	0.057	19.29

*Post-layout simulation results. [b] Measured results including the measurement buffer.

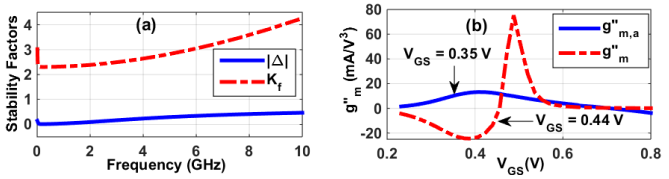

Fig. 5: (a) K_f and Δ stability factors of the proposed balun-LNA, (b) cancellation of nonlinear terms in the proposed linearization scheme.

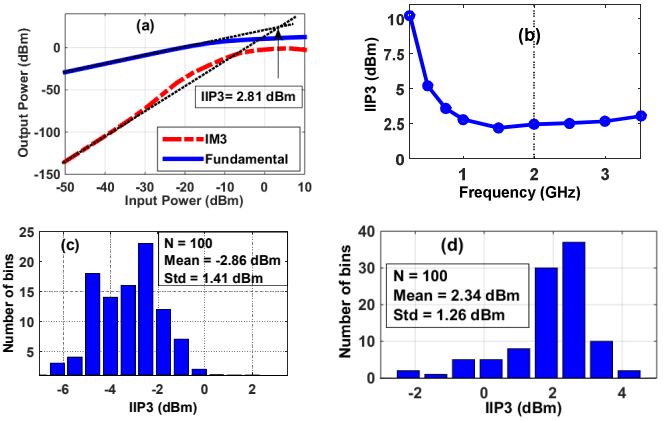

Fig. 6: (a) Simulated IIP3, (b) IIP3 versus the input signal frequency with 10 MHz spacing; IIP3 Monte Carlo simulation results (c) before and (d) after utilizing the proposed linearity improvement technique.

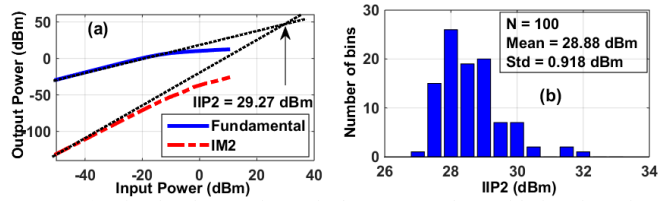

Fig. 7: (a) Simulated IIP2 in typical corner and considering intentional mismatch, (b) IIP2 Monte Carlo simulation results of the proposed balun-LNA.

Table I: PVT simulation results.

Parameter	TT @ 27°C, V_{DD}	SS @ 85°C, 0.9 V_{DD}	FF @-40°C, 1.1 V_{DD}
BW_{-3dB} (GHz)	0.013-3.8	0.016-3.9	0.012-5
S_{21} (dB)	22	20.83	20.77
NF_{min} (dB)	2.57	2.78	2.16
IIP3 (dBm)	+2.81	–0.25	–0.9
Power (mW)	12.5	10.55	14.35

The following figure of merit (FoM) defined in [8] is used in Table II to have a better comparison.

$$FoM(dB) = 10 \times \log \frac{S_{21}\,(abs) \times IIP3\,(mW) \times BW\,(GHz)}{(F-1)(abs) \times P_{DC}(mW)} \qquad (10)$$

where S_{21} is the maximum magnitude of power gain, BW is the bandwidth of the LNA, F is the magnitude of the minimum NF over the entire bandwidth, and P_{DC} is the LNA's power consumption.

IV. Conclusion

In this paper, a new approach employing a positive feedback loop has been introduced for CMOS balun-LNAs to have symmetrical loads without using any additional current bleeding circuit. Moreover, a new linearity improvement technique based on the post distortion and derivative superposition methods has been proposed to improve the IIP3. This linearization scheme also improves the voltage gain of the LNA with consuming negligible additional power.

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