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MASH ΣΔ modulators with a noise-shaped two-step ADC in the second stage

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ABSTRACT

In this paper, a multi-stage noise-shaping (MASH) sigma-delta (ΣΔ) modulator is proposed to be used in low oversampling ratio (OSR) applications. It utilizes a noise-shaped two-step (NSTS) analog-to-digital converter (ADC) in the second stage and benefits its inter-stage gain to provide an extra attenuation of the quantization noise such that the same specifications of a traditional modulator are achieved but with a lower order of noise-shaping. Furthermore, large number of bits is resolved in the second stage while equal number of comparators is used. Compared to the single-loop NSTS ADC, in the proposed structure, the complexity problem of the feedback path and coefficient spreading are eliminated. As an example, a MASH 2-1 sigma-delta modulator has been designed and simulated in a 90 nm CMOS process using Spectre. The achieved resolution is 13.44 effective number of bits in 6.25 MHz signal bandwidth while consuming 19.6 mW power from a single 1 V supply. The sampling frequency is 100 MHz and the simulated figure of merit is 141 fJ/conv-step which shows the efficiency of the proposed modulator.

1. Introduction

Sigma-delta modulators are known as their high accuracy is achieved by noise-shaping together with oversampling [1]. The oversampling property limits the signal bandwidth of these modulators whereas higher bandwidths are needed in recent applications. The modulator bandwidth can be enhanced by increasing the sampling frequency or reducing the oversampling ratio (OSR). But, a high sampling frequency increases the power consumption in the operational amplifiers and it is limited by the minimum achievable settling time of amplifiers in a given CMOS process. On the other hand, reducing the OSR requires a high-order noise-shaping while it makes the modulator prone to instability problems. Multi-stAge noise-SHaping (MASH) modulators, by using several low-order loop filters, can solve the instability problem while providing a high-order noise-shaping. But, this architecture is sensitive to the mismatch between the analog parameters and their corresponding terms in digital section, and hence, they need an accurate analog circuit design.

Another technique to enhance the modulator's resolution without facing instability problems is increasing the quantizer number of levels. But, the number of comparators and digital-to-analog converter (DAC) unit elements are exponentially increased for every additional bit in the quantizer since flash ADCs are often utilized. In [2], this issue is alleviated by realizing the quantizer with a two-step ADC instead of a conventional flash ADC. In addition to high stability of this implementation, some other benefits are also achieved such as two-order extra noise-shaping and providing an additional inter-stage gain to more attenuate the quantization noise while the number of amplifiers is decreased compared to the equivalent traditional modulator. However, this structure adds several branches entering to the first integrator and also the noise-shaped two-step (NSTS) ADC. The multiple branches (5 branches) entering to the first integrator together with the capacitor spreading (varies from 0.25 to 4 times the sampling capacitor) require extremely large capacitors to maintain the input-referred noise below the required quantity. This increases the power consumption of the first OTA compared to the first OTA of the traditional modulator. In the NSTS ADC, on the other hand, several input branches together with the inter-stage gain increase the total quantity of capacitors resulting in more power consumption [3,4]. The double noise-shaped segmentation also uses two DACs and by using a simple first-order transfer function before the fine DAC, the mismatch between the DACs is decreased [5]. However, it reduces the feedback factor of the OTA, increases the kT/C noise, and introduces glitch problems in the feedback path at higher speeds [5]. This limits its usage in wideband applications.

In this paper, a MASH L-1 sigma-delta modulator is proposed where a conventional loop filter and an NSTS ADC are utilized in the

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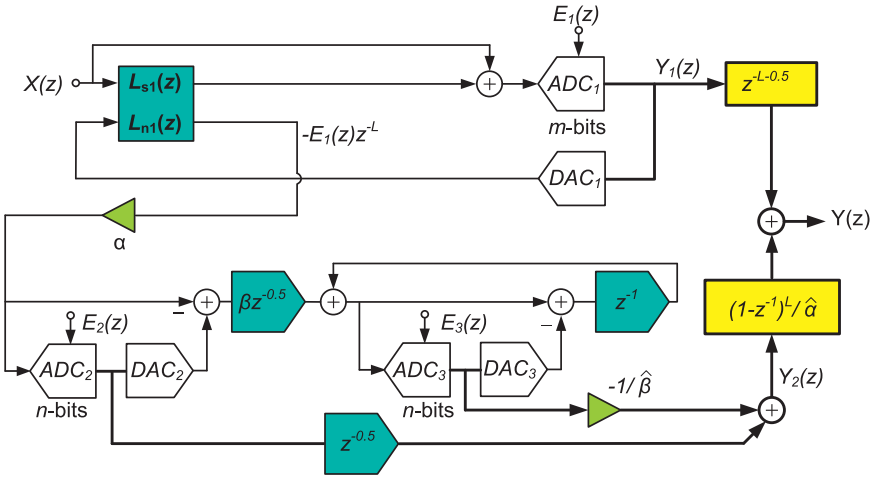

Fig. 1. Proposed MASH L-1 sigma-delta modulator.

first- and second-stages, respectively. It is shown that in low OSRs, the proposed modulator can provide an equal or even more signal-to-quantization noise ratio (SQNR) than the traditional MASH L-2 modulator while using one-order lower noise-shaping. Compared to the implementation in [2], the number of feedback path branches is reduced to one and this branch does not enter to the first integrator, and hence, it does not increase the thermal noise of the first integrator. Moreover, in the proposed structure, the input branches of the NSTS ADC are reduced to one solving the problem of several input branches of the NSTS ADC in [2].

The paper is organized as follows. In Section 2, the structure of the proposed MASH sigma-delta modulator is described and it is compared with the conventional structure. A design prototype is provided in Section 3. The circuit level simulation results are presented in Section 4, and finally, Section 5 concludes the paper.

2. Proposed MASH L–1 ΣΔ modulator

2.1. Proposed modulator structure

The proposed sigma-delta modulator is shown in Fig. 1. It has an Lth-order low-distortion loop filter [6] in the first stage and an NSTS ADC in the second stage. Like all two-step ADCs, the quantization noise of the course ADC (E_2) is cancelled and the final quantization noise of the NSTS ADC is related to the fine ADC (E_3). The first and second stage outputs of the modulator are calculated as

$$Y_1(z) = X(z) + (1 - z^{-1})^L E_1(z) \tag{1}$$

$$Y_2(z) = -\alpha z^{-L-0.5} E_1(z) + \left(z^{-0.5} - \beta z^{-0.5}\frac{1}{\hat{\beta}}\right)E_2(z) - \frac{1}{\hat{\beta}}(1 - z^{-1})E_3(z). \tag{2}$$

Consequently, the total modulator's output is obtained as

$$Y(z) = z^{-L-0.5}Y_1(z) + \frac{1}{\hat{\alpha}}(1 - z^{-1})^L Y_2(z) = z^{-L-0.5}X(z) + \frac{1}{\hat{\alpha}\hat{\beta}}(1 - z^{-1})^{L+1}E_3(z). \tag{3}$$

In these relations, $\hat{\alpha}$ and $\hat{\beta}$ are the digital estimates of α and β, respectively. As it is seen, there are two inter-stage gains to attenuate the quantization noise of the fine ADC. The first inter-stage gain (α) is related to the MASH structure and the second inter-stage gain (β) is provided by the NSTS ADC. Compared to [2] and also traditional MASH modulator, the proposed structure has an additional inter-stage gain making the modulator more efficient in low oversampling ratios. To have a comparison, the traditional MASH L-2 modulator shown in Fig. 2 is considered. Using the same procedure, the total output of this

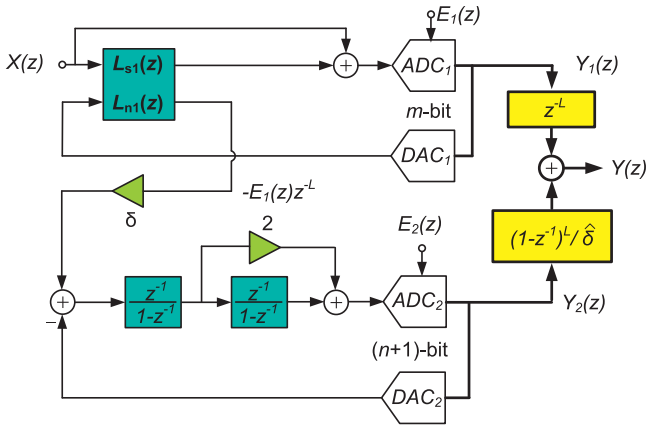

Fig. 2. Conventional MASH L-2 sigma-delta modulator.

modulator is obtained as

$$\begin{aligned} Y(z) &= z^{-L}Y_1(z) + \frac{1}{\hat{\delta}}(1 - z^{-1})^L Y_2(z) = z^{-L}[X(z) + (1 - z^{-1})^L E_1(z)] \\ &\quad + \frac{1}{\hat{\delta}}(1 - z^{-1})^L[-\delta z^{-L}E_1(z) + (1 - z^{-1})^2 E_2(z)] \\ &= z^{-L}X(z) + \frac{1}{\hat{\delta}}(1 - z^{-1})^{L+2}E_2(z) \end{aligned} \tag{4}$$

According to the relations (3) and (4), the traditional modulator has one higher order noise-shaping while the proposed structure has an additional inter-stage gain. The inter-stage gain has a fixed effect on the attenuation of the quantization noise independent of the OSR. Every doubling of the inter-stage gain results in 6 dB enhancement in SQNR. By contrast, the effect of increasing the modulator's order is the OSR dependent. In low OSRs, the SQNR improvement due to the additional order will be less effective [1]. Therefore, the SQNR provided by the proposed modulator in low OSRs is comparable with the traditional modulator (or more in extremely low OSRs) while it has a less order. In [2], there is one inter-stage gain while it provides one extra order of noise-shaping. So, the noise attenuation provided by [2] will be close to the proposed structure in low OSRs while it faces several circuit design issues.

2.2. System level simulations and comparisons

The proposed and conventional modulators are simulated using MATLAB by considering second-order loop filter in the first stage. The first inter-stage gain of both structures (α and δ) is considered to be 16 and the gain of the NSTS ADC is assumed to be 4 (β=4). Four-bit

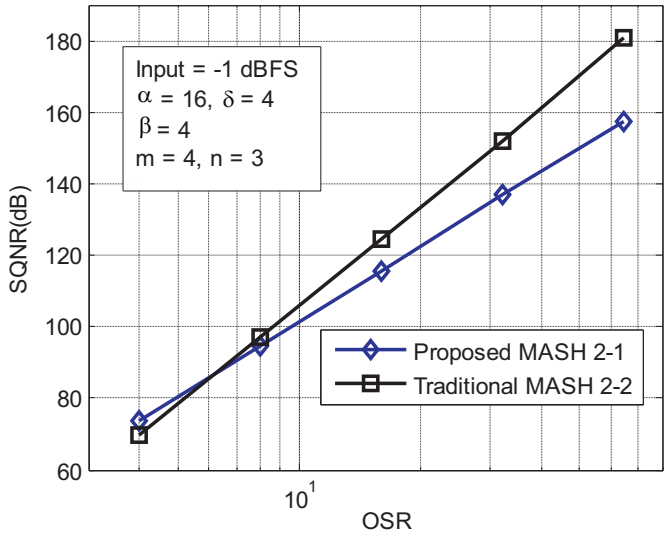

Fig. 3. SQNR of the proposed and traditional modulators versus the OSR.

quantizers are used in the first stages and a 4-bit quantizer is utilized in the second stage of the traditional modulator. Two 3-bit quantizers are employed in the second-stage of the proposed modulator. The simulated SQNR of both modulators is shown in Fig. 3 versus the OSR. As it is seen, in low OSRs, the SQNR of the proposed modulator is comparable with the traditional modulator. Similar situation also exist by the choice of other loop filters in the first stage. For example in L=1 and considering m=3, n=3, α=δ=8 and β=4, the SQNR of the conventional and proposed modulators is approximately equal in 16x OSR. On the other hand, with L=3, m=4, n=3, α=δ=8 and β=4, the SQNR of both structures will be equal in 4× OSR and the conventional modulator provides more SQNR in larger OSRs. As the simulations confirm, the proposed modulator provides similar specifications in low OSRs in comparison with the traditional MASH modulator although it utilizes one order lower noise-shaping. Being effective in low OSRs is an outstanding advantage of this work. It is worth to mention that the proposed sigma-delta modulator can also be utilized in large OSRs without any change since all NTF zeros are located at DC. Note that the gains could deviate from their ideal quantities, however system level simulations shows that for a 0.5% deviation in α, the SQNR will decrease about 4 dB and with the same deviation for β, the SQNR degradation is less than 0.1 dB.

The simulated SQNR of both modulators versus the input signal level with an 8× OSR is illustrated in Fig. 4. As it is clear, the maximum

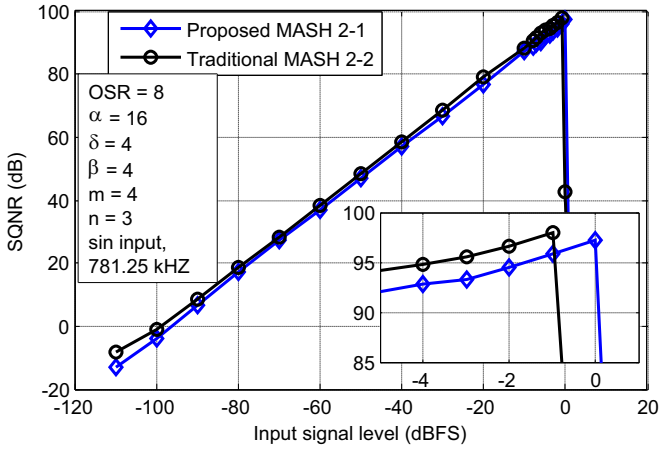

Fig. 4. Dynamic range of the proposed MASH 2-1 and traditional MASH 2-2 sigma-delta modulators.

input signal amplitude in the proposed modulator is one dB more than the traditional scheme. This is owing to using higher quantization bits and also the redundancy in the second-stage NSTS ADC. So, the second stage modulator can tolerate larger input level in comparison with the conventional modulator owing to the larger inter-stage gain. This results in large signal swing in the second stage modulator, and hence, needing higher slew rate and bandwidth in the second stage amplifiers. On the other hand, the circuit non-idealities and noise of the second stage amplifiers are shaped by the first stage loop filter. Hence, the second stage modulator needs smaller capacitors and tolerates more settling errors in the amplifiers. Therefore, the required amplifiers in the second stage modulator will not be power consuming owing to the small capacitors and more relaxed settling errors.

The NSTS ADC is actually a first-order modulator with a high number of quantization bits. So, it can accept higher levels of input signal. In other words, in the proposed structure, a 6-bit quantization is provided by the NSTS ADC while using a 6-bit quantizer in the traditional MASH 2-2 increases the required number of the comparators. The NSTS ADC has the benefit of redundancy [7] and it is able to accept even higher quantities than its full-scale without overloading. The redundancy is provided by the choice of a smaller β which theoretically could be supposed as 8 but it is chosen to be 4. The high level of input voltage increases the SQNR and also reduces the size of capacitors in the first integrator, and hence, reduces the first OTA power consumption. Note that the first integrator is often the most power consuming block in sigma-delta modulators. Considering the power budget, some portions of this saved power can be used in the second stage modulator. Consequently, the amplifier used in the second stage modulator will not increase the overall power consumption of the modulator.

The simulated SQNR of both modulators versus the open-loop DC gain of amplifiers utilized to realize the integrators and active adders is shown in Fig. 5. As it is seen, the same DC gain is required in the first stage of both modulators and the third OTA in the proposed structure needs a higher DC gain amplifier than the conventional MASH 2-2 modulator. Nonetheless, in the proposed MASH 2-1 modulator, the required number of amplifiers is three while four amplifiers are needed in the conventional MASH 2-2 modulator.

The mismatch among the unit elements in the front-end multi-bit DAC can considerably degrade the modulator performance. To alleviate this issue, DAC linearization techniques such as data weighted averaging (DWA) [8] should be utilized. The simulated output spectrum of the proposed modulator before and after using the DWA algorithm and assuming 0.2% mismatch among the DAC unit capacitors is shown in

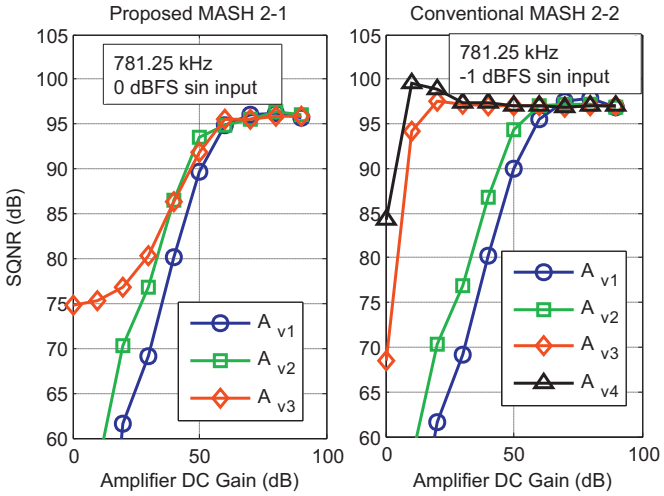

Fig. 5. SQNR versus the open-loop DC gain of amplifiers.

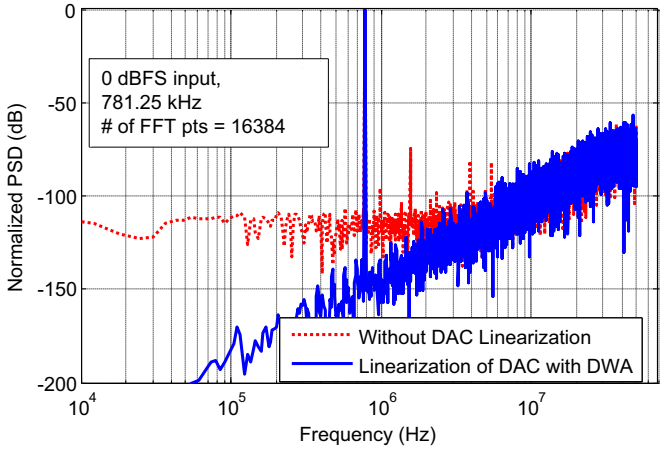

Fig. 6. Simulated output spectrum before and after using the DWA algorithm.

Fig. 6. Without using the DWA algorithm, the SNDR drops to 72.5 dB while after its usage, the SNDR is improved to 93.5 dB which is approximately 3 dB lower than the ideal simulated SQNR (95.7 dB).

3. Design prototype of the proposed modulator

3.1. System level design

As an example, the proposed MASH 2-1 shown in Fig. 7 is designed and simulated to reach 13-bit accuracy. The modulator is the same as the one simulated in the previous section but its gains are adjusted to provide 2 times the quantization noise at the output of the second integrator. This new gain arrangement has two main advantages. First, the input-referred thermal noise power of the second integrator will be attenuated by four. Second, it simplifies the circuit level implementation of α. Although the new gain arrangement increases the output swing of the integrators but this will not be problematic according to the simulations presented at the following. In the second stage, the first inter-stage gain (α) is implemented using the reference scaling.

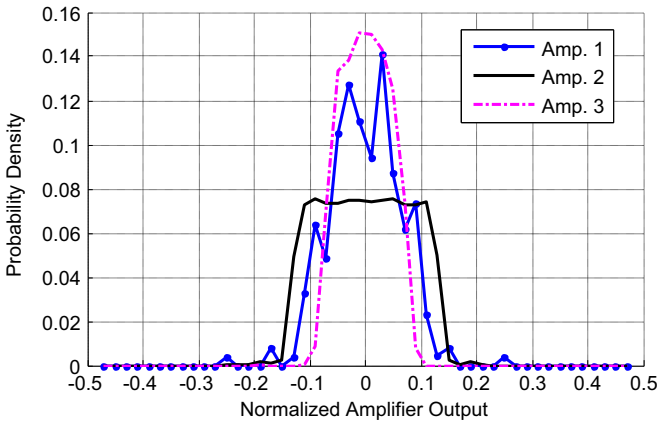

Fig. 8. Normalized output swing of the amplifiers (V_{Ref}=1 V).

The output swing of amplifiers based on behavioral simulations is shown in Fig. 8. Accordingly, the maximum normalized output swing of the first, second, and third OTAs are 0.25, 0.2 and 0.1, respectively. As is seen, the differential output swing of the amplifiers is at most $0.25V_{Ref}$ and the new arrangement of gains does not make the output swing to be problematic.

3.2. Circuit level design

In this section, the detailed circuit level design of the proposed MASH 2-1 modulator is presented.

3.2.1. Thermal noise and capacitor sizing

To achieve a power efficient design, the total SNDR of the modulator should be limited by the circuit noise rather than the quantization noise and distortion. The achieved SQNR by considering all circuit non-idealities is sufficient to reach 80 dB total SNDR which corresponds to 13-bit accuracy. So, the value of sampling capacitors is selected according to the circuit noise considerations. Accordingly, 1.1 pF and 0.11 pF sampling capacitors are needed in the first and second integrators, respectively. Therefore, 1.5 pF and 0.2 pF sampling capacitors are selected in the first and second integrators, respectively. The first integrator has 15 unit capacitors each with 0.1 pF value. The input-referred thermal noise of the first and second integrators (at

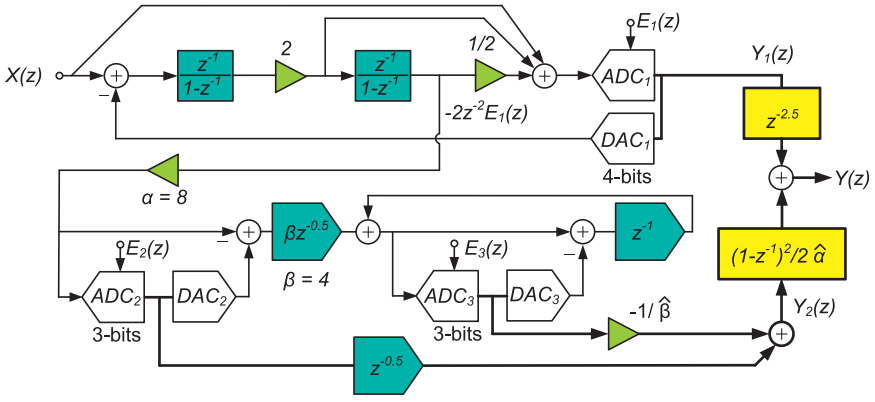

Fig. 7. Proposed MASH 2-1 sigma-delta modulator.

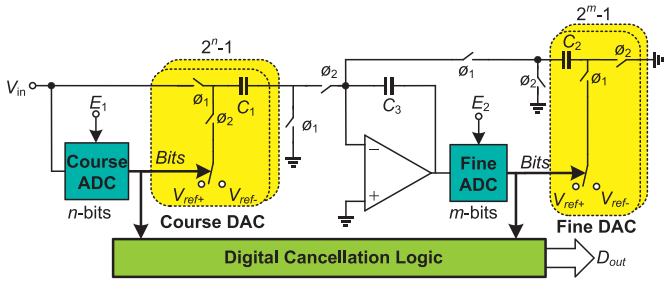

Fig. 9. Circuit implementation of the NSTS ADC [2].

85 °C) are 2.113×10^{-9} V^2 and 0.114×10^{-9} V^2, respectively. This leads to 83.45 dB SNR which provides a good safety margin for the distortion and other noise sources. Unlike the biomedical applications, the flicker noise is negligible compared to the thermal noise in high bandwidth applications as it could be simply removed in digital domain. The clock jitter could also act as a source of non-idealities. In Nyquist rate ADCs, for such accuracy, the clock jitter needs to be less than 3 ps [9] which can be realized without needing much more complexity. Furthermore, in oversampling applications due to slowness of the input signal compared to the clock frequency, the error due to the clock jitter will be lower making the implementation more relaxed.

3.2.2. Switched-capacitor implementation

To explain the switched-capacitor implementation of the proposed MASH 2-1 modulator, firstly the realization of the NSTS ADC is presented. According to Fig. 9, the noise-shaped two-step ADC has two internal ADCs with two corresponding DACs. Here, the course ADC resolves MSB bits and transfers the residue signal to C_3, and then, it is quantized by the fine ADC similar to the traditional two-step ADC. However, in the NSTS ADC, the fine stage quantization noise is also extracted and fedback to the C_3 capacitor with a negative sign. This

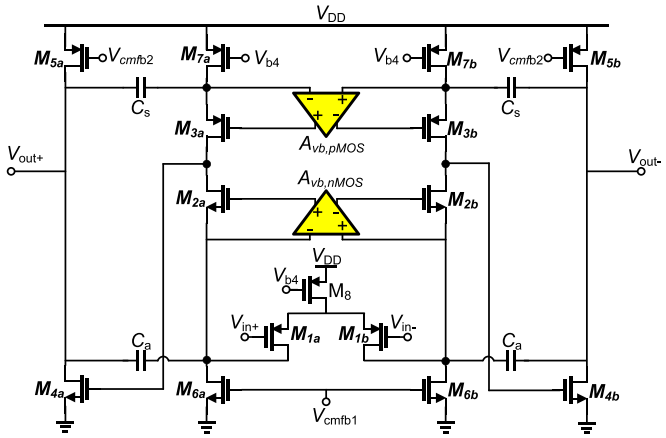

Fig. 11. Two-stage amplifier with gain-boosting.

extracted quantization noise is added to the residue of the coarse stage quantization noise with one clock delay, and consequently, it provides a first-order noise-shaping.

Considering the circuit implementation, at ϕ_1 the input signal is sampled on C_1 and it is quantized at the end of this phase. Next at ϕ_2, the residue of the coarse stage is transferred to C_3 and then at the end of this phase, it is quantized by the fine ADC. At the end of the following ϕ_1 phase, the C_2 capacitors transfer the negative DAC voltage to the value sampled on C_3. So, the fine residue voltage is sampled on C_3 and simultaneously the input voltage is sampled on C_1. Finally at the following ϕ_2 phase, the coarse residue is transferred to C_3 and it is added to the minus of the fine stage residue to provide a first-order noise-shaping. As shown in Fig. 9, the NSTS ADC only uses one OTA to extract both the quantization noise of the course and fine ADCs. The reduced number of capacitors is due to using the OTA sharing method proposed by [2] which offers a lower capacitance and reduces the number of switches.

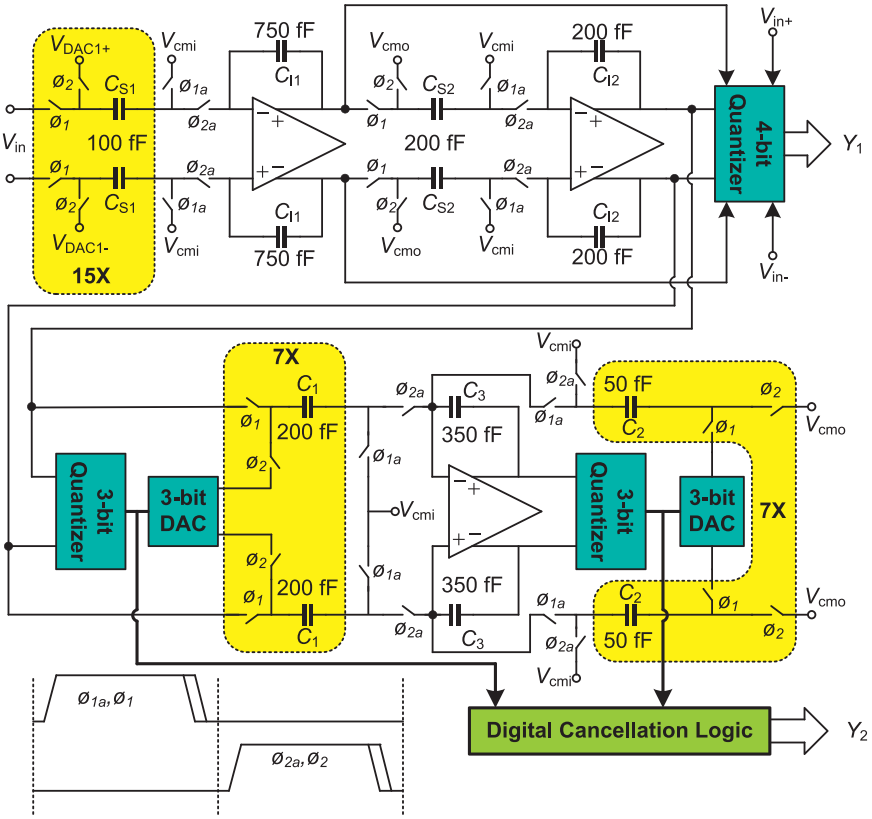

Fig. 10. Switched-capacitor implementation of the proposed MASH 2-1 sigma-delta modulator.

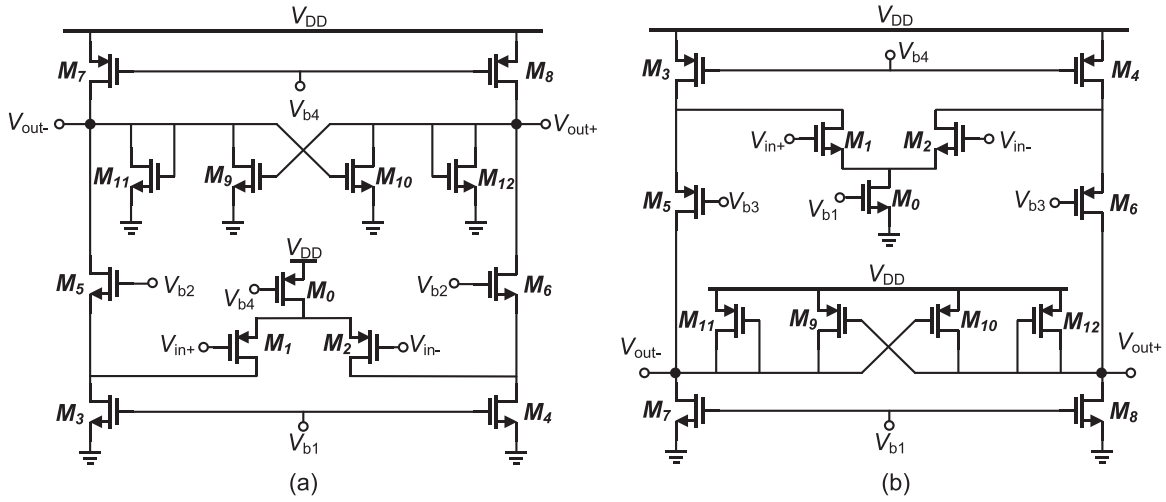

Fig. 12. (a) nMOS and (b) pMOS input pair gain-boosting amplifiers.

Table 1
Performance summary of the designed OTAs.

Amplifiers	DC gain	Unity gain bandwidth	Phase margin	Capacitive load	Power consumption
First amplifier	65.81 dB	1.45 GHz	67°	1.10 pF	6.8 mW
Second amplifier	64.96 dB	0.78 GHz	70°	2.00 pF	5.1 mW
Third amplifier	65.14 dB	1.38 GHz	80°	0.28 pF	4.4 mW

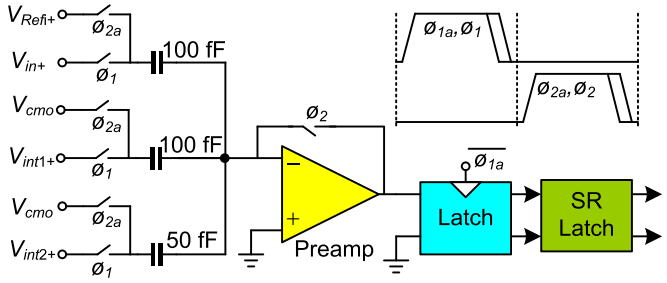

Fig. 13. Passive adder together with the preceding quantizer used in the first stage of the modulator (single-ended shown for simplicity).

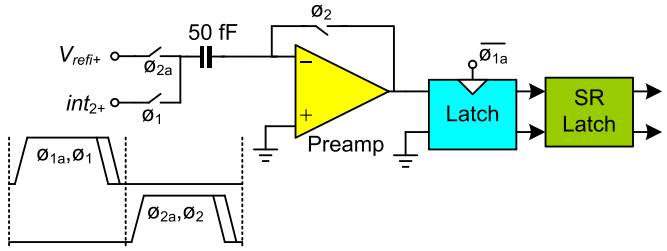

Fig. 14. Preamplifier cell together with the preceding quantizer used in the ADC_2 (single-ended shown for simplicity).

The switched-capacitor realization of the proposed MASH 2-1 modulator is shown in Fig. 10. The DAC_1 is implemented by dividing the first integrator sampling capacitors to 15 parts ($15C_{S1}$). As is seen, the first integrator uses 1.5 pF and 0.75 pF sampling and integrating capacitors, respectively, to provide a gain of two. The second integrator has a unity gain which is provided by using 0.2 pF in both sampling and integrating capacitors. In the NSTS ADC, by using 1.4 pF and 0.35 pF capacitors, the coarse ADC quantization error is multiplied by 4. The fine ADC error is transferred to C_3 by a unity gain similar to the system level realization shown in Fig. 7. This is provided by 0.35 pF capacitors.

Compared to the conventional MASH L-2 modulator which uses two or three OTAs in the second stage, the proposed structure needs

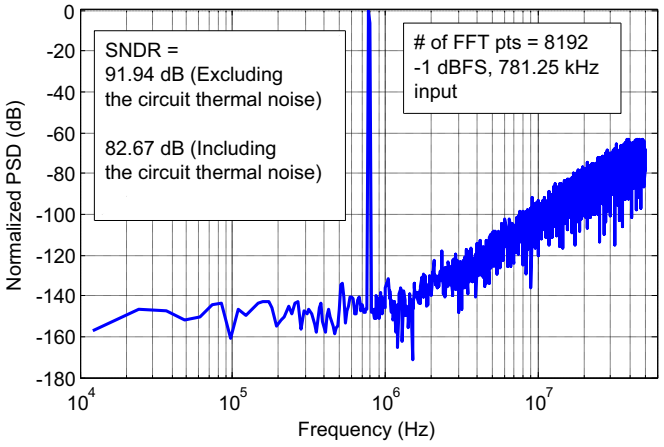

Fig. 15. The output spectrum of the proposed modulator excluding the circuit noise (TT @27 °C).

lower number of OTAs. This reduces the power consumption and relaxes the circuit design complexity. Compared to [2], since the NSTS ADC is used in the second stage of the MASH architecture, its output does not need to be fedback to the modulator input. Since adding any branch to the first integrator increases both the modulator noise and power consumption, here the advantages of the NSTS ADC are utilized while its drawbacks are alleviated.

3.2.3. *Operational transconductance amplifiers*

Based on the system level simulation results, at least 60 dB DC gain is needed in the amplifiers to avoid the SQNR degradation considerably. To provide such DC gain, a two-stage amplifier consisting of a gain-boosting folded-cascode amplifier in the first stage and a simple common-source amplifier in the second stage is utilized. The schematic of the amplifier is shown in Fig. 11. Two switched-capacitor common-mode feedback (CMFB) circuits are used to define the common-mode voltage of both stages at the desired level. Hybrid-cascode compensation [10] is used to stabilize the amplifier. Since the DC gain

requirements of three amplifiers are close to each other, this topology is used for all of them, but with the scaling of devices and bias currents to reduce the power consumption.

The boosting circuits are necessary because the desired gain is not achievable by a simple two-stage amplifier in the current technology. The schematic of the gain-boosting amplifiers for the nMOS and pMOS transistors are shown in Fig. 12 where the folded-cascode topology is used to provide high bandwidth and meet the desired input common-mode voltage. Both diode-connected and cross-coupled load transistors are used at the output to provide sufficient gain without needing an explicit CMFB circuit in the gain-boosting amplifiers. The bias voltages of the boosting and the main amplifier are provided using constant current biasing circuits. The simulated performance summary of the amplifiers is summarized in Table 1 where the power of the biasing and boosting circuits is also included.

3.2.4. Passive adder and preamplifier

The three input branches of the first stage quantizer need an adder. This adder can be implemented in an active or a passive form. The passive implementation is more power efficient, and so, it is used here. The implementation of the passive adder is shown in Fig. 13. It is a fully-differential circuit, but the single-ended version is shown here for the sake of simplicity. A two-stage preamplifier is utilized. It comprises of a differential amplifier with a diode-connected active load in the first stage and a differential amplifier with both of cross-coupled and diode-connected active loads in the second stage.

In the NSTS ADC, no passive adder is needed. But since the reference and input voltages are scaled down, the offset of the comparators will be troublesome. So, a preamplifier is also needed before the ADC_2 and ADC_3 quantizers. The preamplifier of the first stage is also used in the NSTS ADC. The switched-capacitor realization of the preamplifier circuits used in ADC_2 is shown in Fig. 14. The same structure is also used for ADC_3 but it works with the reverse clock phases.

Table 2
Performance summary of the simulated modulator.

Parameter	SS @85 °C	TT @27 °C	FF @−40 °C
SNDR	79.96 dB	82.67 dB	84.07 dB
ENOB	12.99 bit	13.44 bit	13.67 bit
Power dissipation	18.0 mW	19.6 mW	21.2 mW
FoM	177 fJ/conv-step	141 fJ/conv-step	130 fJ/conv-step
Sampling rate	100 MHz		
Oversampling Ratio	8		
Signal bandwidth	6.25 MHz		
Supply voltage	1 V		
Technology	90 nm CMOS		

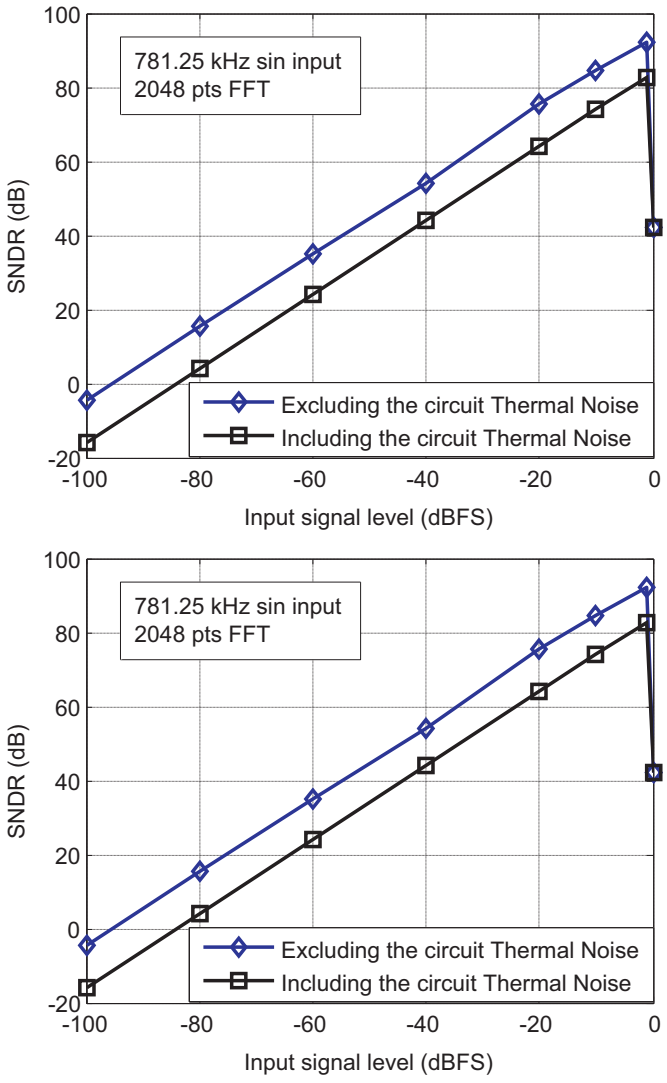

Fig. 16. Simulated SNDR versus the input signal level (TT @27 °C).

Table 3
ADC performance comparison.

Reference	Process (nm)	V_{DD} (v)	Modulator architecture	BW (MHz)	OSR	f_s (MHz)	SNDR (dB)	Power (mW)	FoM (fJ/conv-step)
TCASII'08* [13]	65	1	MASH 3–1	1	64	128	93	11.16	153
JSSC'09 [14]	90	1.2	Single-loop fourth-order	4	12.5	100	66.85	11.76	820
JSSC'09 [15]	180	1.8	MASH 0–3	3.125	8	50	73.9	24	950
JSSC'10 [16]	180	1.8	Delta-sigma pipelined	5	8	80	75.4	36	750
JSSC'10 [17]	90	1.2	MASH 2–1 Multirate	1.92	20	80	65.5	6.83	1170
JSSC'10 [18]	180	1.8	Incremental sigma-delta second-order	1	45	45	86.3	38.1	1460
JSSC'11 [19]	180	1.5	Single-loop third-order	1.05	24	50	78.2	2.9	210
JSSC'09 [20]	180	1.2	Sturdy-MASH 2–2	0.625	16	20	74.6	3.2	583
TCASI'12 [21]	130	1.3	VCO-based multi-rate MASH	4	12.5	100	77	13.8	300
JSSC'12 [22]	65	1.2	MASH 1–1–1–1	2.5	8	40	70.4	3.73	276
TCASI'12 [23]	130	1.2	MASH 2–2	5	13	130	75.7	16	320
CTA'13* [24]	90	1	MASH 3–2	10	8	160	79.4	35.7	230
JCSC'12* [25]	90	1	Sturdy MASH 2–2	10	10	200	78.9	37	250
AICSP'11 [26]	180	1.8	Single-loop third-order	6	8	96	60.7	6.18	580
JSSC'09 [27]	180	1.5	Third-order noise coupled	1.9	16	60	81	8.1	250
MWSCAS'09 [28]	90	1.2	MASH 2–2	31.25	8	500	70	140	866
TCASI'09* [29]	90	1.2	Second-order path coupled	2	15	60	56	1.56	750
JSSC'13 [30]	180	1.3	Noise-shaped pipelined	5.33	6	64	73.7	13.9	270
JSSC'13 [5]	130	1.2	Noise-shaped two-step integrating ADC	5	8	80	70.7	8.1	280
JSSC'14 [31]	65	1.25	MASH 1–0	15	8	240	67	37	674
AICSP'14*,a [32]	65	1	Single-loop third-order	10	32	640	87.3	21	55
ISCAS'14* [33]	65	1	MASH 2–2	10	50	1000	66.8	1.5	42
AICSP'14* [34]	65	1.2	Single-loop second-order	2	24	96	75.8	10.3	510
This work*	90	1	Proposed MASH 2–1	6.25	8	100	82.67	19.6	141

* Simulation results
[a] Excluding the power consumption of the digital calibration logic.

3.2.5. Switches implementation

Bootstrapped switches proposed in [11] are used for the input signal sampling to meet the targeted linearity. These switches provide an approximately constant on-resistance in different input voltages, and hence, provide a good linearity. For the first stage DAC, CMOS switches are used. Other switches are implemented by simple nMOS transistors.

4. Circuit level simulation results

The proposed MASH 2-1 sigma-delta modulator is simulated using Spectre in 90 nm UMC CMOS technology. The modulator output spectrum for −1 dBFS, 781.25 kHz input signal is shown in Fig. 15. The achieved SNDR is about 91.9 dB without considering the circuit noise. By considering the total circuit thermal noise, the whole SNDR of the modulator is about 82.7 dB corresponding to 13.4 ENOBs. The simulated SNDR versus the input signal amplitude is shown in Fig. 16. The achieved dynamic range is about 83 dB.

The DWA algorithm is not implemented in the circuit level but its power consumption can be estimated using [12] where a 4-bit DWA in a 90 nm CMOS process is realized. The power consumption of this reference is 2 mW in 320 MHz clock rate and 1.3 V power supply. Considering that the power consumption of a digital circuit is linearly related to its operating frequency and square of its supply voltage, the power consumption of the DWA logic is estimated as 0.37 mW.

The total average power consumption of the simulated modulator is about 19.6 mW where 16.3 mW is consumed by the amplifiers, 370 μW is consumed by the DWA logic, 300 μW is consumed by the resistive ladders, and the remaining is consumed by the preamplifiers and latches. The simulated performance of the proposed MASH 2-1 modulator in different process corner cases and temperature variations is summarized in Table 2, where the circuit thermal noise is also considered.

The performance of the designed modulator is compared with some recent similar state-of-the-art modulators using the following figure of merit (FoM). Their specifications are similar to the designed modulator as most of them have a bandwidth more than 1 MHz and SNDR above 68 dB.

$$FoM = \frac{Power}{2 \times BW \times 2^{ENOB}} \quad (5)$$

In this relation, BW denotes the signal bandwidth in Hz and the effective number of bits (ENOBs) is calculated as follows:

$$ENOB = \frac{SNDR\,(dB) - 1.76}{6.02} \quad (6)$$

As it is seen from Table 3, the proposed modulator has a very good figure of merit compared to the others. Note that this SNDR is achieved by only 3 orders of noise-shaping while the others with the same specifications such as the OSR, have 4 orders of noise-shaping. This relaxes the circuit design complexities since the proposed modulator needs lower number of OTAs to be designed and lower number of branches which relaxes the OTA specifications. Although these results are based on the circuit level simulations while some of the others are based on the measurement results, but the achieved outstanding FoM verifies the effectiveness of the proposed modulator.

5. Conclusions

In this paper, a MASH sigma-delta modulator is proposed which utilizes a noise-shaped two-step ADC in the second stage. The proposed modulator enhances the SNDR by using large number of quantization bits in the second stage and also two inter-stage gains. So, it is more efficient especially when a low OSR should be utilized since the resolution enhancement is less dependent on the OSR. Moreover, using a NSTS ADC in the second stage simplifies its realization in comparison with a single-loop modulator utilizing the NSTS ADC. The circuit level simulations verify the usefulness of the proposed modulator.

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