Analog Integr Circ Sig Process (2014) 81:805–814
DOI 10.1007/s10470-014-0434-6

MIXED SIGNAL LETTER

An error-feedback noise-shaping SAR ADC in 90 nm CMOS

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Received: 16 July 2014 / Revised: 15 September 2014 / Accepted: 20 October 2014 / Published online: 28 October 2014

Abstract In this paper, a new structure is proposed to utilize the noise-shaping in a charge redistribution successive approximation register (SAR) analog-to-digital converter (ADC). The proposed ADC is based on the error-feedback structure and it does not require any extra capacitor compared to the main SAR ADC and just by employing an operational transconductance amplifier (OTA), a first-order noise-shaping is provided. The closed-loop configuration of the OTA is similar to the flip-around scheme in which the dummy capacitor also acts as the sampling capacitor. In this configuration, the quantization noise of the ADC is sampled and transferred via the dummy capacitor without any charge sharing or capacitor interleaving, and so, the capacitors mismatch is alleviated in the feedback path. The proposed ADC is realized by employing a few number of capacitors and switches compared to the conventional SAR ADC. As a design example, the proposed noise-shaping SAR ADC is simulated in a 90 nm CMOS technology by employing a 3-bit SAR ADC. Simulation results with Spectre-RF shows 11.1-bit effective resolution in 1 MHz input bandwidth and 128 MHz sampling rate while consuming 208 μW power. The achieved figure of merit is 46.4 fJ/conv-step.

Keywords Charge redistribution SAR ADCs · Noise-shaping SAR ADC · Switched-capacitor circuits · Sigma-delta modulators · Decimation filters

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1 Introduction

Charge redistribution successive approximation register (SAR) analog-to-digital converters (ADCs) are widely used in low to medium bandwidths and resolutions. Demand for lower power consumption makes this ADC a good candidate for recent applications such as the biomedical and wireless sensor networks [1–4]. On the other hand, there are some problems associated with this ADC to achieve high resolution. In the charge redistribution DAC array, the number of required unit capacitors is exponentially increased with the ADC resolution resulting in a large sampling capacitor, and hence, a large chip area. Also, the large difference between the most significant bit (MSB) and the least significant bit (LSB) capacitors results in a poor matching [5] while it is an important issue to achieve high resolution. Moreover, a high accuracy comparator is needed and it is a great challenge in the design of high resolution SAR ADCs in nano-meter CMOS technologies [3].

To relax some of these problems, recently in [6], a 5-bit charge redistribution SAR ADC is utilized in a third-order error feedback noise-shaping structure [7] to realize an ADC with 9.5-bit effective resolution. To achieve noise-shaping, in this structure, an OTA and a few number of capacitors are added into the 5-bit SAR ADC. However, there are some drawbacks in this implementation such as the clocking complexity, using of interleaved capacitors, and needing a high DC gain (about 60 dB) and high gain bandwidth product (GBW) OTA with a low feedback factor (1/8). Besides, in this work, a passive sampling is performed while its attenuation effect and the way it has been compensated for are not mentioned. In other words, the passive sampling makes an attenuation factor of 1/8 in the quantization noise extraction since the sampled charge

into the dummy capacitor is shared with seven equivalent capacitors without any buffering or amplification. Moreover, this architecture suffers from the sensitivity to the coefficients variation of the error feedback structure.

Another noise-shaping SAR ADC is proposed in [8]. This structure also adds an OTA and a few capacitors to the main SAR ADC to provide the noise-shaping property resulting in a low capacitive load. In this ADC, the sampling capacitor is not discharged and due to the oversampling property, a low current is drained from the input signal source resulting in high input impedance. However, this technique defines a duration for the OTA gain instead of a minimum value, and hence, needing a careful circuit design. Besides, an interleaving together with a passive sampling are utilized in this work resulting in more sensitivity to the circuit non-idealities. The proposed noise-shaping SAR ADC in [9] needs a low quantity of capacitors, but it suffers from the clocking complexity since six different clock phases (φ_1-φ_6) are required. Moreover, the input signal is charge transferred via the OTA, and hence, the OTA non-idealities may produce signal dependent harmonics at the output spectrum.

To solve some of the above-mentioned problems, another structure is recently proposed in [10]. This structure is straightforward in the implementation and reduces the total number of capacitors while simultaneously relaxes the required OTA specifications. In this paper, a new first-order noise-shaping SAR ADC is proposed which offers some new enhancements over [10] such as alleviating the need for capacitor interleaving and providing a unity feedback factor for the OTA. Moreover, in the proposed ADC, the OTA input and output common-mode voltages can be different. This simplifies the OTA realization since in most OTAs, they should be different. Besides, the proposed ADC structure alleviates the capacitor mismatch in the feedback path, and hence, it is more suitable in high resolution ADCs.

The paper is organized as follows. Section 2 explains the structure of the proposed noise-shaping SAR ADC. In Sect. 3, some circuit level design considerations of the proposed ADC are provided. The circuit level design and simulation results of the implemented ADC prototype are presented in Sect. 4, and finally, Sect. 5 concludes the paper.

2 Proposed noise-shaping SAR ADC

2.1 Operation of the proposed noise-shaping SAR ADC

The system level block diagram of the proposed ADC excluding the output digital decimation filters is shown in Fig. 1(a). A typical circuit level implementation of this ADC is also illustrated in Fig. 1(b) where a 3-bit SAR ADC is utilized. It is worth mentioning that any arbitrary resolution can be used in the charge redistribution SAR ADC. In Fig. 1(a), α models the input signal attenuation due to the dummy capacitor deletion from the sampling process. This coefficient can be simply calculated as $(2^nC_u-C_u)/2^nC_u$ where n and C_u denote the resolution and unit capacitance of the DAC array, respectively. For example, this coefficient is 7/8 for a 3-bit DAC array. The coefficient β models the effect of the OTA finite DC gain which will be explained more later. In Fig. 1(b), V_{cmi} and V_{cmo} denote the input and output common-mode voltages of the OTA which can be selected differently.

According to Fig. 1(a), the quantization error of the SAR ADC is extracted and fedback to the modulator input by a unit delay. It is then subtracted from the input signal. The quantization error extraction is performed by adder-2 which is realized by the SAR ADC. It is then added to the input signal through adder-1 which is implemented by the OTA. Two non-overlapping clock phases with the similar duration times are used in the sampling and conversion phases. These clock phases are also utilized in the modulator, SAR control logic, and switches.

To explain the circuit operation, one cycle of the conversion sequence is investigated. Suppose that the input signal has been sampled into the charge redistribution DAC capacitors (i.e. C_d, C, $2C$, and $4C$) and the circuit is working in the conversion phase. So, according to Fig. 1(b), the top-plate of the charge redistribution DAC capacitors is only connected to the comparator input and their bottom-plate voltage is controlled by the SAR control logic. In other words, the DAC array is disconnected from the OTA in this phase because S_5 and S_6 switches are off and switches S_{1-4} reset both the OTA input and output voltages. By performing a binary search algorithm, the SAR control logic produces the output bits (B_2, B_1 and B_0) after three φ_{SAR} clock periods. In each φ_{SAR} clock phase, one of the capacitors ($4C$, $2C$, or C) is connected to the reference voltage as a trial bit and then the comparator decides that this trial bit is true or not. If it is true, no change is performed on the capacitor's connection. Otherwise, this capacitor is connected to the reversed reference voltage. The same procedure is performed by the following capacitors. To save the quantization error into the dummy capacitor, another φ_{SAR} clock period is used to apply the comparator's last decision into the DAC voltage [6, 8]. As shown in Fig. 1(c), the last clock period is specific to the SAR control logic and the comparator will not take any decision during this period.

In sampling phase, switches $S_{5,6}$ are on and S_{1-4} switches are off and the OTA is utilized in the closed-loop flip-around configuration. So, the stored quantization error voltage into the dummy capacitors is applied to the top-

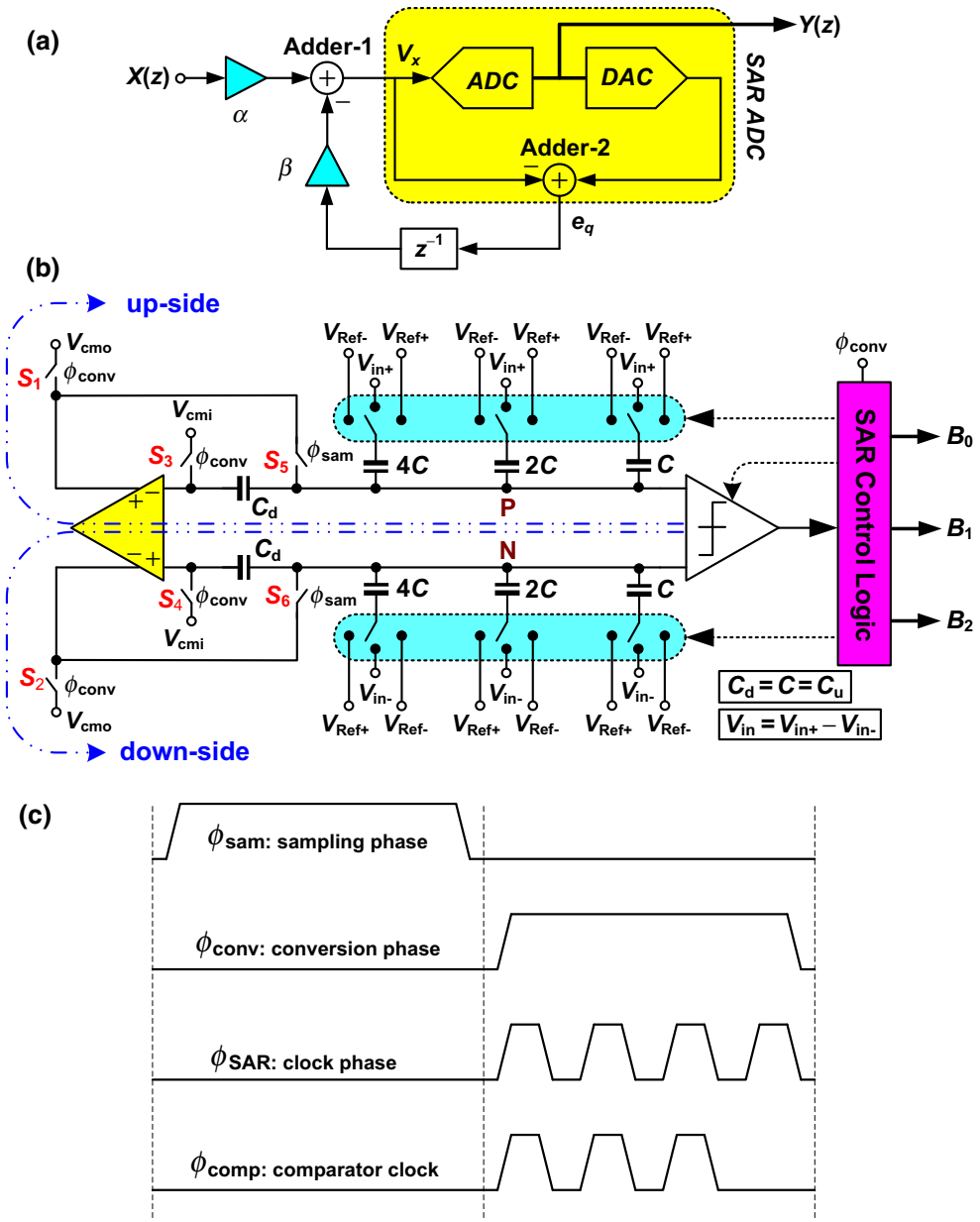

Fig. 1 **a** Block diagram, **b** a typical 3-bit switched-capacitor implementation and **c** clocking scheme in the proposed SAR ADC

plate of charge redistribution capacitors. On the other hand, the input signal is applied to their bottom plates. Hence, the voltage sampled on these capacitors is the input voltage minus the quantization error voltage related to the previous conversion phase. This voltage is shown by V_x in Fig. 1(a) and this sampling scheme realizes the adder-1 in Fig. 1(a). At the next conversion phase, the quantization error is directly added to this value, and hence, the ADC output after the next conversion phase is given by:

$$y[n] = \alpha V_{in}[n] + e_q[n] - e_q[n-1] \quad (1)$$

where $y[n] = (V_{\mathrm{Ref}}/2)B_2 + (V_{\mathrm{Ref}}/4)B_1 + (V_{\mathrm{Ref}}/8)B_0$. According to relation (1), a first-order noise-shaping of the SAR ADC quantization noise is achieved at the overall ADC output.

Since the quantization error is stored and transferred through the dummy capacitor itself, by placing it in the feedback path, a unity feedback factor is provided for the OTA.

2.2 Specifications and comparison

As mentioned in [11], one of the main drawbacks in error feedback noise-shaping ADCs is the capacitor mismatch in the feedback path which deviates the modulator's coefficients from the desired values. But, this is not happened in

the proposed ADC since there is only one feedback path which is realized by a single capacitor without any mismatch concern.

In previously published works in [6, 8], the quantization error is sampled into the dummy capacitor and it is then transferred to another capacitor. However, in the proposed technique, the quantization noise is stored into the dummy capacitor without transferring it to another capacitor. Therefore, the mismatch between the capacitors affects the quantization noise extraction in [6, 8], and hence, the feedback coefficient is changed while there is not such mismatch effect here.

Compared to the other noise-shaping SAR ADCs, the proposed structure is the most straightforward scheme in the implementation because it does not need any interleaving and extra capacitor and adds a few number of switches to the conventional SAR ADC. Moreover, in the proposed ADC, the input and output common-mode voltages of the OTA are decoupled from each other, and hence, it simplifies the OTA realization.

The main advantage of the proposed noise-shaping SAR ADC over the conventional SAR ADC is the reduced number of capacitors in the charge redistribution DAC array. This reduces the capacitor spreading and results in a better matching. To provide a fair comparison, a noise-shaping SAR ADC with an n-bit charge redistribution DAC array and a conventional m-bit SAR ADC are considered where both are assumed to be fully-differential. The in-band quantization noise power and total quantity of capacitors in the proposed noise-shaping SAR ADC are given by [12]:

$$\begin{aligned} Q_{NSSAR} &\simeq \frac{\pi^2}{3 \times OSR^3} \cdot \frac{V_{ref}^2}{12 \times 2^{2n}} \\ C_{NSSAR} &= 2^{n+1} C_u \end{aligned} \tag{2}$$

where OSR is the oversampling ratio. On the other hand, in a simple SAR ADC with an m-bit charge redistribution DAC array, the quantization noise power and total quantity of capacitors are calculated as [13]:

$$\begin{aligned} Q_{SAR} &= \frac{V_{ref}^2}{12 \times 2^{2m}} \\ C_{SAR} &= 2^{m+1} C_u \end{aligned} \tag{3}$$

To have the same signal-to-quantization noise ratio (SQNR), the following ratio between the total capacitors of these ADCs is achieved:

$$\frac{C_{SAR}}{C_{NSSAR}} \approx \sqrt{\frac{3 \times OSR^3}{\pi^2}} \tag{4}$$

As is seen, in the proposed ADC, the total required amount of capacitors can be substantially reduced by using a high oversampling ratio resulting in reduced silicon die area compared to the conventional SAR ADC. For example, with an OSR = 64, this area reduction ratio is about 256 which is a considerable reduction in the area of the charge redistribution DAC array.

However, the relation (4) can only be used when the kT/C thermal noise resulting from the DAC switches is less than the quantization noise. Otherwise, the value of unit capacitor in DAC array is calculated according to the circuit noise considerations and relation (4) cannot be used. This situation will be examined in Sect. 3.2. Nonetheless, in medium resolutions, the kT/C noise is not dominant and the relation (4) is still valid and in high resolutions, by using a large OSR, the required area in DAC array in the proposed ADC will be lower than that of the conventional SAR ADC.

The noise-shaping SAR ADC always needs a digital decimation filter to attenuate the out-of-band noise and also down sample the digitized output. As will be shown in the design example section, the decimation filter is not area consuming as much as the charge redistribution DAC array, and hence, the proposed noise-shaping SAR ADC is an area efficient structure. Furthermore, in the proposed ADC, the required anti-aliasing filter is more relaxed owing to use the oversampling in comparison with the conventional SAR ADC. In conventional SAR ADCs, the required accuracy for the comparator is as high as the total ADC. But, the proposed noise-shaping SAR ADC needs a more relaxed comparator since the comparator non-idealities such as the input-referred offset and noise are shaped similarly to the quantization noise. This simplifies the comparator design although it should be operated at a high sampling rate.

3 Circuit level design considerations

3.1 OTA specifications

The key parameters in OTA topology selection are the input and output voltage swing, minimum DC gain, and gain-bandwidth. In the proposed ADC, the maximum output swing of the OTA is about half LSB voltage of the SAR ADC which is obviously small. Therefore, a low output swing OTA is needed.

For a closed-loop unity-gain buffer, the OTA open-loop DC gain (A_v) reduces its gain (G) from unity to $G \approx 1-1/A_v$. On the other hand, the OTA realizes the feedback path of the modulator. So, the limited OTA DC gain changes the coefficient β in Fig. 1(a) from unity, and then, moves the noise transfer function (NTF) zero from unity to $1-1/A_v$ and this degrades the noise-shaping ability. Therefore, a minimum acceptable DC gain for the OTA is needed which can be obtained through behavioral system level simulations.

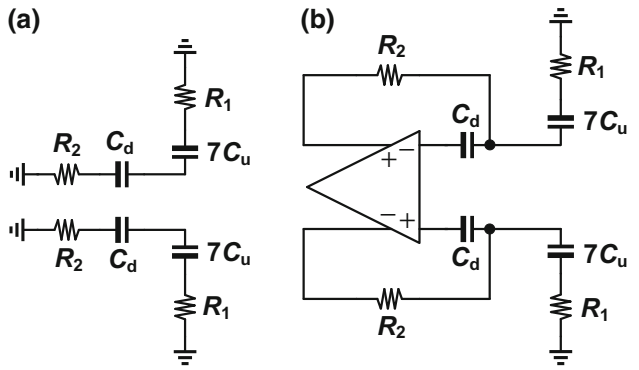

Fig. 2 Equivalent circuits for noise analysis **a** at conversion and **b** sampling phases

As shown in Fig. 1(b), the total load capacitance driven by the OTA is the DAC capacitors array excluding the dummy capacitor. Although the OTA load capacitance can be large when a high-resolution DAC array is utilized. But in this case, the LSB of the SAR ADC becomes small, and hence, the OTA needs to settle with a small output swing.

3.2 Thermal noise considerations

To analyze the circuit thermal noise, the equivalent circuit of DAC capacitive array and buffer are separately shown at conversion and sampling phases in Fig. 2(a) and (b), respectively. According to the equivalent circuit of Fig. 2(a), the squared root mean square (rms) of the thermal noise voltage stored into the dummy capacitors at the conversion phase is given by:

$$\overline{V_{n,sam}^2} \approx \frac{7}{8} \cdot \frac{kT}{C_u} \tag{5}$$

This noise is directly transferred to the output at the next phase like the quantization error. At the sampling phase, according to Fig. 2(b), the stored noise voltage on $7C_u$ is of concern since it is directly quantized by the comparator. This noise can be calculated as:

$$\overline{V_{n,conv}^2} \approx \frac{kT}{7C_u} \tag{6}$$

By summing the noise powers at two phases and considering the oversampling, the in-band thermal noise of the fully-differential structure is obtained as:

$$\overline{V_{n,\,in-band}^2} = \frac{1}{OSR}\left(\overline{V_{n,conv}^2} + \overline{V_{n,sam}^2}\right) \approx \frac{2kT}{C_u \times OSR} \tag{7}$$

The in-band thermal noise of the fully-differential conventional SAR ADC due to the sampling can be calculated as $2kT/(2^m.C_u)$. The input-referred thermal noise of the proposed structure is higher than that of the conventional SAR ADC when OSR $< 2^m$. So, the capacitance reduction will be lower than the relation given in (4) in cases that the thermal noise is dominant. It is worth mentioning that this situation does not occur in most cases because such high resolutions could not be achieved by SAR ADCs.

3.3 Charge redistribution array matching

In the proposed structure, the generated error due to the capacitor array non-idealities is similar to the conventional SAR ADC. So, unlike the quantization error, the error of capacitive DAC array is not shaped. Nonetheless, the matching requirements of charge redistribution DAC array in the proposed ADC may be slightly better than the simple SAR ADC because of lower parasitic capacitances and lower capacitor spread. By using the DAC error calculation addressed in [4, 14], the maximum standard deviation of differential nonlinearity (DNL) error related to the charge redistribution DAC array is approximated by:

$$\sigma_{DNL,\max} = \sqrt{2^N - 1}\frac{\sigma_u}{C_u} LSB = \sqrt{2^N - 1}\frac{\sigma\left(\frac{\Delta C}{C}\right)}{\sqrt{2}} LSB \tag{8}$$

where N is the expected resolution and σ_u is the standard deviation of the unit capacitor. σ is the standard deviation of capacitor mismatch and LSB is the least significant bit $(1/2^N)$ of the noise-shaping SAR ADC. To provide high yield, the condition of $3\sigma_{DNL,\max} \leq 0.5LSB$ should be satisfied. With respect to relation (8), the maximum acceptable deviation for the capacitors will be as:

$$\sigma_{\max}\left(\frac{\Delta C}{C}\right) = \frac{\sqrt{2}}{6\sqrt{2^N - 1}} \tag{9}$$

In brief, having the desired resolution, the standard deviation of the unit capacitor can be calculated from (9) and then its value can be obtained by selecting a capacitor with appropriate σ from the technology files. It is worth mentioning that the capacitor mismatch in simple SAR ADCs is similar. Since the difference between the MSB and LSB capacitors is lower in the proposed structure, it will have lower parasitic capacitance.

4 Design prototype and simulation results

A design prototype is provided to evaluate the effectiveness of the proposed noise-shaping SAR ADC. The design is targeted to achieve 11-bit accuracy with 1 MHz input signal bandwidth in a 90 nm CMOS process. The proposed ADC can be implemented with different combinations of the OSR and number of bits in the charge redistribution DAC array. According to the behavioral simulation results, the proposed ADC can provide a maximum SQNR of

70.5 dB with OSR = 64 and 3-bit SAR ADC. In all these simulations, α and β coefficients are assumed to be 0.875 and 1, respectively. It is worth mentioning that using simple SAR ADCs to obtain such accuracy is challenging due to the exponential growth of DAC capacitors and the comparator offset and noise.

There are two considerations for the selection of the unit capacitor in DAC array including the matching and thermal noise and the maximum of these two values should be considered. Considering the thermal noise in relation (7), to achieve an SNR of 70.5 dB, the unit capacitor value is approximately obtained as 5 fF. On the other hand, it should be larger than 30 fF to satisfy the required matching condition in DAC capacitive array according to the relation (9) and utilized 90 nm CMOS technology files for metal–insulator–metal (MIM) capacitors. Therefore, to achieve the desired resolution, the value of unit capacitor is chosen as 30 fF. Obviously, by this amount of unit capacitor, the thermal noise will be much lower than the quantization noise. So, the thermal noise has no effect on the selection of the unit capacitor in this design. By contrast, in low OSRs, the thermal noise can be considerable.

The minimum acceptable DC gain of the OTA is obtained by behavioral system level simulations. In this simulation, $\alpha = 7/8$ and β is considered as $1-1/A_v$. According to the simulation results, the minimum OTA DC gain of 40 dB is sufficient to prevent from the SQNR degradation. Therefore, owing to the needed low output swing and moderate DC gain, a telescopic OTA with a pMOS input pair is employed in this design which is shown in Fig. 3. The simulated OTA DC gain is 41.94 dB with 631 MHz unity gain bandwidth and 78.6° phase margin while driving a 0.21 pF capacitive load. The power consumption of the simulated OTA including the bias circuit is 82 μW.

The asynchronous logic proposed in [15] is used to realize the SAR control logic. This offers some advantages as follows. It uses lower number of transistors to achieve high speed with low power. In addition, due to the high

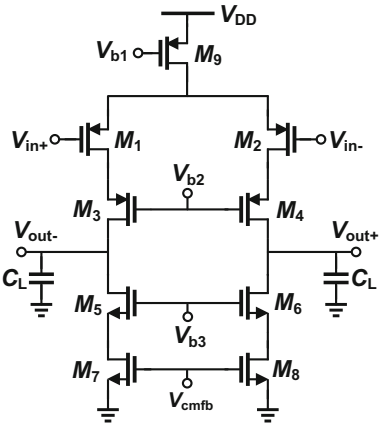

Fig. 3 Simulated OTA circuit

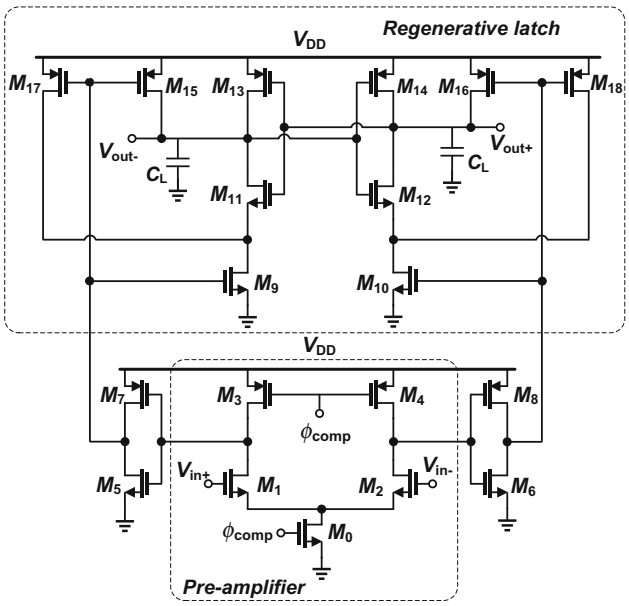

Fig. 4 Comparator circuit

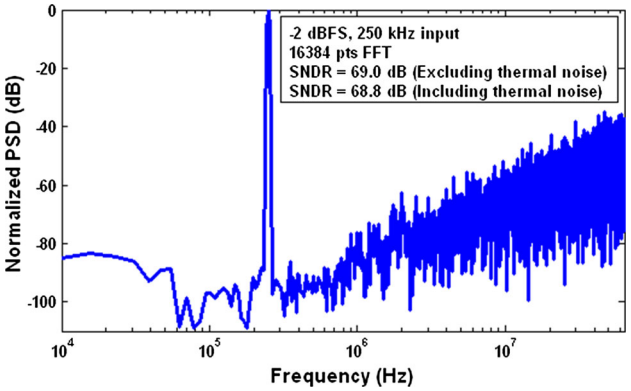

Fig. 5 Output spectrum of the simulated ADC excluding the circuit noise

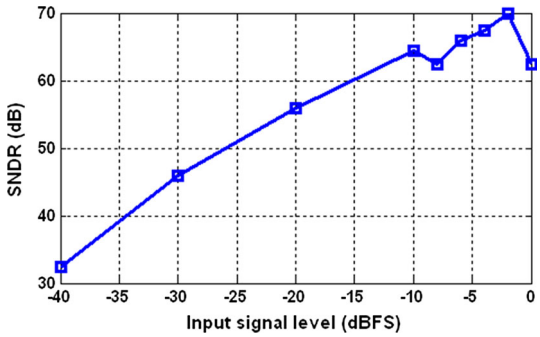

Fig. 6 Simulated SNDR versus the input signal level including the circuit noise

clock rate in the design prototype, the dynamic logic is used to further reduce the power consumption. From the clocking point of view, the asynchronous SAR ADC has the lowest complexity. It requires just two non-overlapping phases of sampling and conversion and all other clocks such as the high frequency comparator clock are generated by the logic. So, there is no need for a high frequency clock generation. Note that the power consumption in this situation is low because no high frequency clock is actually generated.

To provide the medium speed needed for the comparator, the high-speed latched comparator of [16] is used in this design which is shown in Fig. 4. This comparator comprises of an n-type input preamplifier and a dynamic regenerative latch. At the rising edge of the clock, the input differential voltage, V_{in}, is converted to the time and/or phase differences. Then the inverters, which are realized by $M_{5,7}$ and $M_{6,8}$ transistors, act as the amplifiers to provide the latch input signal. Hence, the amplified signal with a time difference is applied to the regenerative latch and due to the positive feedback, the back to back inverters force one of the output nodes to the ground and the other one to V_{DD} depending on the input signal polarity.

The designed ADC has been simulated in Spectre-RF with a 1 V reference voltage. A -2 dBFS and 250 kHz sinusoidal input signal was applied to the ADC. The simulated ADC power spectrum is shown in Fig. 5. The achieved maximum signal-to-noise and distortion ratio (SNDR) is 69.0 dB excluding the circuit noise. By considering the circuit noise, it becomes 68.8 dB which corresponds to 11.1 effective number of bits. The simulated ADC dynamic range by considering the circuit noise is illustrated in Fig. 6 showing a dynamic range of about 68.8 dB. The simulated ADC performance in different process corner cases and temperature variations is summarized in Table 1. The average total power consumption is about 208 μW where 82, 103, 18, and 5 μW are consumed by the OTA, DAC capacitive array, SAR logic, and

Table 1 Performance summary of the simulated ADC including the circuit noise

Parameter	TT @ 27 °C	FF @ −40 °C	SS @ 85 °C
SNDR	68.8 dB	69 dB	65.7 dB
ENOB	11.13 bit	11.17 bit	10.62 bit
Power dissipation	208 μW	206 μW	210 μW
FoM (fJ/conv-step)	46.4	44.7	66.7
Sampling rate	128 MHz		
Oversampling ratio	64		
Signal bandwidth	1 MHz		
Supply voltage	1 V		
Technology	90 nm CMOS		

Table 2 Performance comparison of the proposed ADC with several state-of-the-art converters

Reference	CMOS Process (nm)	Sampling capacitor (pF)	ADC architecture	BW (MHz)	Power (μW)	ENOB	FOM (fJ/conv-step)
JSSC'07 [1]	180	–	SAR	0.05	25	10.55	165
AICSP'10 [3]	180	15.36	SAR	0.05	3.8	9.40	56
JSSC'12 [8]	65	0.64	Noise-shaping SAR	11	806	10.00	35.8
AICSP'13 [10]	90	1.68	Noise-shaping SAR	0.05	4.53	10.68	27.6
CTA'12 [14]	350	–	SAR	0.001	0.130	9.40	96
CTA'11 [19]	250	36.68	SAR	0.028	1,683	11.04	14,389
ISSCC'10 [20]	130	–	SAR	11.25	2,990	11.35	50.8
EDSSC'09 [21][a]	350	11.52	SAR	0.01	38	11.90	497
ISSCC'10 [22]	65	0.53	SAR	25	820	9.11	30
JSSC'11 [23]	180	9.6	SAR	0.05	1.3	9.30	21
ISCAS'11 [24]	90	–	SAR	0.5	7	9.20	11.9
ISCAS'12 [25]	180	0.24	SAR	0.25	14.2	9.24	47
JSSC'12 [26]	180	2.3	SAR	0.1	1.04	9.34	8.03
ISSCC'10 [27]	45	–	SAR	0.25	800	11.0	781.2
AICSP'13 [28]	180	–	SAR	0.1	946.8	11.07	2,200
AICSP'13 [29][a]	180	11.78	SAR	0.05	6.21	9.55	82.8
This work[a]	90	0.24	Noise-shaping SAR	1	208.0	11.13	46.4
					301.3	11.05	71.0[b]

[a] Simulation results

[b] Including the power of the decimation filters

comparator, respectively. The estimated power consumption of the required decimation filter according to Appendix A is about 93.3 μW.

The following figure-of-merit (FoM) is utilized to compare the designed ADC with some of the recently reported SAR ADCs in Table 2:

$$FoM = \frac{Power}{2BW \times 2^{ENOB}} \quad (10)$$

where BW is the input signal bandwidth. The achieved FoM is 46.4 fJ/conv-step excluding the power consumption of the decimation filters and it is 71.0 fJ/conv-step by considering the power of decimation filters. Although, the FoM of the proposed ADC is slightly higher than some of them in Table 2, its power efficiency becomes more apparent if the power reduction of the anti-aliasing filter is considered. As mentioned before, due to using the oversampling, the required analog anti-aliasing filter in the proposed ADC is much simpler than the SAR ADCs without the noise shaping.

If a conventional SAR ADC is used to realize the above-mentioned design example, 4096 C_u capacitors are needed in the charge redistribution DAC array. Neglecting the capacitors routing, the required area for this amount of capacitors is calculated about 102,000 μm^2. While the required number of capacitors in the proposed ADC is about 8 C_u. However, the area needed for decimation filters in the proposed ADC should also be considered to provide a fair comparison. In Appendix A, the required area and power for the decimation filters for this designed ADC are estimated. According to this estimation, the needed area for decimation filters is about 28,514 μm^2. Therefore, as it is seen, the area of the proposed ADC is less than the conventional SAR ADC in this design example.

5 Conclusions

In this paper, a simple technique is proposed to extract the SAR ADC quantization noise, and hence, to realize a noise-shaping SAR ADC. To do so, an OTA with relaxed specifications such as DC gain, unity-gain bandwidth and output swing is needed. Compared to the conventional SAR ADC, the required area in the proposed ADC is considerably reduced. A design example was provided to show the effectiveness of the proposed ADC.

Appendix

In order to evaluate the decimation filters power and area overhead in the proposed ADC, this appendix is provided. The required decimation filters for the designed prototype

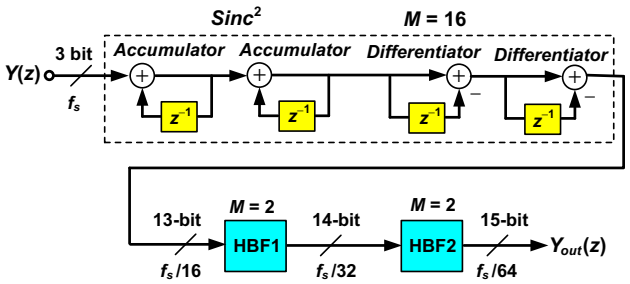

Fig. 7 Three-stage decimation filter

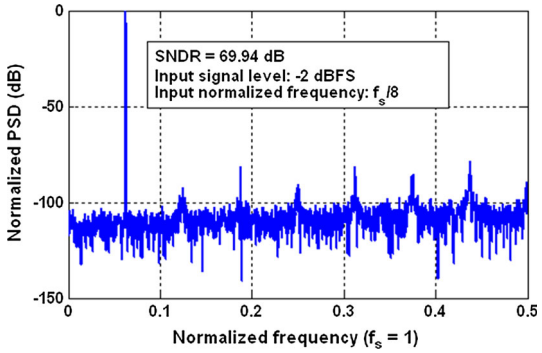

Fig. 8 Nyquist rate output spectrum of the designed ADC resulting from the system level simulations

are modeled in MATLAB and Simulink. As shown in Fig. 7, a multi-stage configuration for decimation filters is utilized which is more power efficient than a single-stage one [17]. A second-order Sinc filter with a 16 down-sampling ratio is used since the noise-shaping order in the proposed ADC is one. Two halfband filters are used to reduce the rate of the ADC output to the Nyquist rate. The first halfband filter is a 11th order digital filter which has seven taps. The order of the second halfband filter is 15th with nine taps. By using this decimation filter, the ADC maximum SQNR drops from the ideal 70.5 dB to about 69.9 dB which is degraded about 0.6 dB. The resulting output spectrum of the total ADC including the decimation filters is shown in Fig. 8.

To estimate the decimation filters power consumption and area, the design presented in [18] is utilized. In [18], OSR = 64, the input rate of the decimation filter is 3.072 MHz, a fourth-order Sinc filter is used with 20-bit resolution in filter taps. Moreover, the first halfband filter is a 10th order filter with 24-bit resolution in filter taps. The above-mentioned decimation filter has been fabricated in a 0.18 μm CMOS technology with 1.8 V power supply. To estimate the power consumption and the area according to this filter, some scaling coefficients must be used such as the following. The voltage reduction coefficient is 1/1.8. This coefficient has no effect on the area but it changes the

power consumption by its square. The technology scaling coefficient is 0.09/0.18. This coefficient changes both the area and dynamic power by its square. The resolution of the block (number of bits in the block) coefficient changes the power consumption and the area directly. The frequency scaling coefficient does not change the area but it reduces the dynamic power directly. Finally, the hardware changes coefficient (such as the filter order or number of taps) directly affects both the power consumption and area. Although we consider all power sources as dynamic and this makes the estimation highfalutin, but an overestimation coefficient with a quantity of 1.25 is also used to provide a conservative estimation.

The power consumption and area of the second-order Sinc filter in Fig. 7 are estimated as, respectively:

$$P_{Sinc2} = \underbrace{\left(\frac{1}{1.8}\right)^2}_{Voltage} \cdot \underbrace{\left(\frac{0.09}{0.18}\right)^2}_{Technology} \cdot \underbrace{\left(\frac{13}{20}\right)}_{No.\,of\,bits} \cdot \underbrace{\left(\frac{128}{3.072}\right)}_{Frequency} \cdot \underbrace{\left(\frac{1}{2}\right)}_{Hardware} \times 46.4 \times \underbrace{1.25}_{Overestimation} = 60.60\,\mu W \quad (11)$$

$$A_{Sinc2} = \underbrace{\left(\frac{0.09}{0.18}\right)^2}_{Technology} \cdot \underbrace{\left(\frac{13}{20}\right)}_{No.\,of\,bits} \cdot \underbrace{\left(\frac{1}{2}\right)}_{Hardware} \times 29985 \times \underbrace{1.25}_{Overestimation} = 3,066\mu m^2 \quad (12)$$

The power consumption and area of the first halfband filter are estimated as:

$$P_{HBF1} = \underbrace{\left(\frac{1}{1.8}\right)^2}_{Voltage} \cdot \underbrace{\left(\frac{0.09}{0.18}\right)^2}_{Technology} \cdot \underbrace{\left(\frac{14}{24}\right)}_{No.\,of\,bits} \cdot \underbrace{\left(\frac{4000}{96}\right)}_{Frequency} \cdot \underbrace{\left(\frac{7}{5}\right)}_{No.\,of\,taps} \times 5.9 \times \underbrace{1.25}_{Overestimation} = 19.38\,\mu W \quad (13)$$

$$A_{HBF1} = \underbrace{\left(\frac{0.09}{0.18}\right)^2}_{Technology} \cdot \underbrace{\left(\frac{14}{24}\right)}_{No.\,of\,bits} \cdot \underbrace{\left(\frac{7}{5}\right)}_{Hardware} \times 41941 \times \underbrace{1.25}_{Overestimation} = 10,703\mu m^2 \quad (14)$$

Since the number of coefficients of the second halfband filter is not specified in [18], its power consumption and area are calculated according to the first halfband filter as:

$$P_{HBF2} = \underbrace{\left(\frac{1}{1.8}\right)^2}_{Voltage} \cdot \underbrace{\left(\frac{0.09}{0.18}\right)^2}_{Technology} \cdot \underbrace{\left(\frac{15}{24}\right)}_{No.\,of\,bits} \cdot \underbrace{\left(\frac{2000}{96}\right)}_{Frequency} \cdot \underbrace{\left(\frac{9}{5}\right)}_{No.\,of\,taps} \times 5.9 \times \underbrace{1.25}_{Overestimation} = 13.34\,\mu W \quad (15)$$

$$A_{HBF2} = \underbrace{\left(\frac{0.09}{0.18}\right)^2}_{Technology} \cdot \underbrace{\left(\frac{15}{24}\right)}_{No.\,of\,bits} \cdot \underbrace{\left(\frac{9}{5}\right)}_{Hardware} \times 41941 \times \underbrace{1.25}_{Overestimation} = 14,745\mu m^2 \quad (16)$$

Consequently, for the targeted design example, the power consumption in the required decimation filters is approximately 93.3 μW and its area is about 28,514 μm^2.

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