Energy-efficient high-accuracy switching method for SAR ADCs

E. Rahimi and M. Yavari

A new tri-level switching method for successive approximation register (SAR) analogue-to-digital converters (ADCs) is presented. The proposed switching method enhances the efficiency of digital-to-analogue converter switching energy by 93.7% and achieves a 75% reduction in the total capacitor size, compared with the conventional SAR ADC. In addition, the accuracy of the proposed SAR ADC has no dependency on the accuracy of the mid-level reference voltage ($V_{Ref}$) except in the least significant bit, and the common-mode voltage at the input of the comparator will remain approximately unchanged. Analytical calculations and behavioural simulation results are provided to demonstrate the effectiveness of the proposed switching scheme.

**Introduction:** Capacitor switching consumes considerable power in charge-redistribution successive approximation register (SAR) analogue-to-digital converters (ADCs). Recently, several techniques have been proposed to reduce the switching energy and/or the capacitor size [1–5]. Compared with the conventional structure, the set and down phases, in the generation of 2nd-MSB, the bottom plate of the largest capacitor arrays, and the bottom plates of capacitors are connected to the third reference voltage ($V_{Ref}$) except during the generation of the LSB, making the required switching energy and the total capacitor size by 50% compared with the conventional SAR ADC. In addition, the accuracy of the proposed SAR ADC has no dependency on the accuracy of the mid-level reference voltage ($V_{Ref}$) except in the least significant bit, and the common-mode voltage at the input of the comparator will remain approximately unchanged. Analytical calculations and behavioural simulation results are provided to demonstrate the effectiveness of the proposed switching scheme.

The proposed capacitor switching scheme: Fig. 1 shows the proposed DAC switching scheme for a 3-bit SAR ADC which is realised in three phases: most significant bit (MSB), 2nd-MSB to 2nd-LSB and LSB. In the first phase (the MSB phase), after turning on the sampling switches, the differential input signal is sampled on the top plate of both capacitor arrays, and the bottom plates of capacitors are connected to the third reference voltage ($V_{Ref}$) which is equal to half of the reference voltage ($V_{Ref}$). After turning off the sampling switches, the MSB is obtained by the first comparison and no switching energy will be consumed like the one in [3]. In the second phase (2nd-MSB to 2nd-LSB phase), in the generation of 2nd-MSB, the bottom plate of the largest capacitor in the capacitor array which sampled the largest input voltage is connected to $V_{Ref}$, and simultaneously, the same capacitor in the other capacitor array is connected to the ground. Thus, the outputs of both capacitor arrays are changed by $0.25V_{Ref}$ in opposite directions. As a result, the sampled differential input signal is compared with $\pm 0.5V_{Ref}$, and the 2nd-MSB is decided. The conversion cycle of the next bits is similar to the 2nd-MSB except the LSB one, and the conversion cycle of LSb is different from the others. Hence, for an n-bit SAR ADC, this procedure also holds for the next n-3 bits. As shown in Fig. 1, in the LSB phase, the unit capacitor in one capacitor array which has the largest voltage potential is switched to the ground, and in the counterpart array, the unit capacitor remains unchanged. Fig. 2 shows the DAC output waveforms with the proposed switching scheme. As can be seen, the input common-mode voltage of the comparator is approximately constant unlike [2, 4, 5]. In addition, the control logic implementation for this new scheme is simple, and it needs no more complexity compared with the conventional one. Thus, it requires no additional area and power consumption in the control logic, and so, in the overall ADC, unlike [4, 5]. Finally, this new scheme reduces both the switching energy and the total capacitor size by 50% compared with [3] which has the same qualifications such as the fixed comparator input common-mode voltage and no dependency on the accuracy of $V_{Ref}$, and also, the simple control logic.
LSB generation where only one of the capacitor arrays is switched. However, in [4, 5], during each conversion cycle except the MSB, only one capacitor array is switched from $V_{cm}$ to the ground or $V_{Ref}$, and thus, this imprecise transition because of the inaccuracy of $V_{cm}$ remains uncompensated.

Comparison of switching schemes: The behavioural simulations of switching techniques reported in [2, 3] and this new scheme for a fully-differential 10-bit SAR ADC were performed in MATLAB and the results of switching energy against the output codes are illustrated in Fig. 3. The average switching energy for the proposed fully-differential 10-bit SAR ADC is 84.9$CV^2_{Ref}$ which amounts to a reduction of 93.7% in the switching energy compared with the conventional structure. In Table 1, the main features of the proposed scheme and the schemes of [2–5] are compared. As can be seen, the average switching energy of the proposed fully-differential 10-bit SAR ADC is half that of the $V_{cm}$-based SAR ADC [3]. Although, the switching energy of this work is more than that of [4, 5], it needs only a simple digital circuit and the ADC performance has no dependency on the precision of $V_{cm}$ except the LSB and this is an important achievement since the third reference voltage realisation with the overall ADC accuracy would be power hungry. Moreover, in the proposed switching scheme, the common-mode voltage at the comparator input is constant except in the LSB transition, making the comparator’s realisation more relaxed.

![Fig. 3 Switching energy against output digital codes](image)

Table 1: Comparison of several switching schemes for 10-bit ADC

<table>
<thead>
<tr>
<th>Switching scheme</th>
<th>Average switching energy ($CV^2_{Ref}$)</th>
<th>Energy saving</th>
<th>Area reduction</th>
<th>Logic complexity</th>
<th>Dependency on the accuracy of $V_{cm}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Conventional</td>
<td>1363.3 Reference</td>
<td>Reference</td>
<td>Reference</td>
<td>Low</td>
<td>--</td>
</tr>
<tr>
<td>Set and down [2]</td>
<td>255.5</td>
<td>81.2</td>
<td>50%</td>
<td>Low</td>
<td>--</td>
</tr>
<tr>
<td>$V_{cm}$-based [3]</td>
<td>170.2</td>
<td>87.5</td>
<td>50%</td>
<td>Low</td>
<td>No</td>
</tr>
<tr>
<td>Tri-level [4]</td>
<td>42.4</td>
<td>96.89</td>
<td>75%</td>
<td>Medium</td>
<td>Very high (all bits except MSB)</td>
</tr>
<tr>
<td>$V_{cm}$-based monotonic [5]</td>
<td>31.9</td>
<td>97.66</td>
<td>75%</td>
<td>Medium</td>
<td>Very high (all bits except MSB)</td>
</tr>
<tr>
<td>This work</td>
<td>84.9</td>
<td>93.7</td>
<td>75%</td>
<td>Low</td>
<td>Very low (only LSB)</td>
</tr>
</tbody>
</table>

Conclusion: An energy efficient DAC switching scheme for SAR ADCs is proposed resulting in 93.7% less switching energy and a 75% reduction in total capacitor size compared with the conventional SAR ADC. In this scheme, the comparator input common-mode voltage is almost constant and the ADC operation is robust against variations in the third reference voltage ($V_{cm}$) expect in the LSB transition. In addition, it needs only a simple logic circuit to realise a successive operation. Hence, the proposed switching technique can be used in the realisation of low power and small area SAR ADCs.

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