Energy-efficient high-accuracy switching method for SAR ADCs

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A new tri-level switching method for successive approximation register (SAR) analogue-to-digital converters (ADCs) is presented. The proposed switching method enhances the efficiency of digital-to-analogue converter switching energy by 93.7% and achieves a 75% reduction in the total capacitor size, compared with the conventional SAR ADC. In addition, the accuracy of the proposed SAR ADC has no dependency on the accuracy of the mid-level reference voltage (V_{cm}) except in the least significant bit, and the common-mode voltage at the input of the comparator will remain approximately unchanged. Analytical calculations and behavioural simulation results are provided to demonstrate the effectiveness of the proposed switching scheme.

Introduction: Capacitor switching consumes considerable power in charge-redistribution successive approximation register (SAR) analogue-to-digital converters (ADCs). Recently, several techniques have been proposed to reduce the switching energy and/or the capacitor size [1–5]. Compared with the conventional structure, the set and down scheme [2], the V_{cm}-based capacitor switching scheme [3], the tri-level architecture [4] and the V_{cm}-based monotonic scheme [5] reduce the digital-to-analogue converter (DAC) switching energy by 81.2, 87.5, 96.89 and 97.66%, respectively. In [2, 4, 5], a large variation of the common-mode voltage in the fully-differential DAC would cause a negative effect on the operation of the comparator. Although the switching schemes in [4, 5] reduce the DAC switching energy more than the others, the ADC accuracy highly depends on the accuracy of the middle reference voltage (V_{cm}). Moreover, in these techniques, a relatively complex control logic is required resulting in more power consumption in the digital section, and also, the design complexity. In this Letter, a new switching scheme based on the third reference voltage is presented to reduce the DAC switching energy and the total capacitor size more efficiently. The inaccuracy of V_{cm} does not affect the ADC operation except the least significant bit (LSB), and the outputs of the differential DAC have a constant common-mode voltage except during the generation of the LSB, making the required comparator's performance much more relaxed.

Proposed capacitor switching scheme: Fig. 1 shows the proposed DAC switching scheme for a 3-bit SAR ADC which is realised in three phases: most significant bit (MSB), 2nd-MSB to 2nd-LSB and LSB. In the first phase (the MSB phase), after turning on the sampling switches, the differential input signal is sampled on the top plate of both capacitor arrays, and the bottom plates of capacitors are connected to the third reference voltage (V_{cm}) which is equal to half of the reference voltage (V_{Ref}). After turning off the sampling switches, the MSB is obtained by the first comparison and no switching energy will be consumed like the one in [3]. In the second phase (2nd-MSB to 2nd-LSB phase), in the generation of 2nd-MSB, the bottom plate of the largest capacitor in the capacitor array which sampled the lower input voltage is connected to V_{Ref}, and simultaneously, the same capacitor in the other capacitor array is connected to the ground. Thus, the outputs of both capacitor arrays are changed by $0.25V_{Ref}$ but in opposite directions. As a result, the sampled differential input signal is compared with $\pm 0.5V_{Ref}$, and the 2nd-MSB is decided. The conversion cycle of the next bits is similar to the 2nd-MSB except the LSB one, and the conversion cycle of LSB is different from the others. Hence, for an n-bit SAR ADC, this procedure also holds for the next n-3 bits. As shown in Fig. 1, in the LSB phase, the unit capacitor in one capacitor array which has the larger voltage potential is switched to the ground, and in the counterpart array, the unit capacitor remains unchanged. Fig. 2 shows the DAC output waveforms with the proposed switching scheme. As can be seen, the input common-mode voltage of the comparator is approximately constant unlike [2, 4, 5]. In addition, the control logic implementation for this new scheme is simple, and it needs no more complexity compared with the conventional one. Thus, it requires no additional area and power consumption in the control logic, and so, in the overall ADC, unlike [4, 5]. Finally, this new scheme reduces both the switching energy and the total capacitor size by 50% compared with [3] which has the same qualifications such as the fixed comparator input common-mode voltage and no dependency on the accuracy of V_{cm}, and also, the simple control logic.

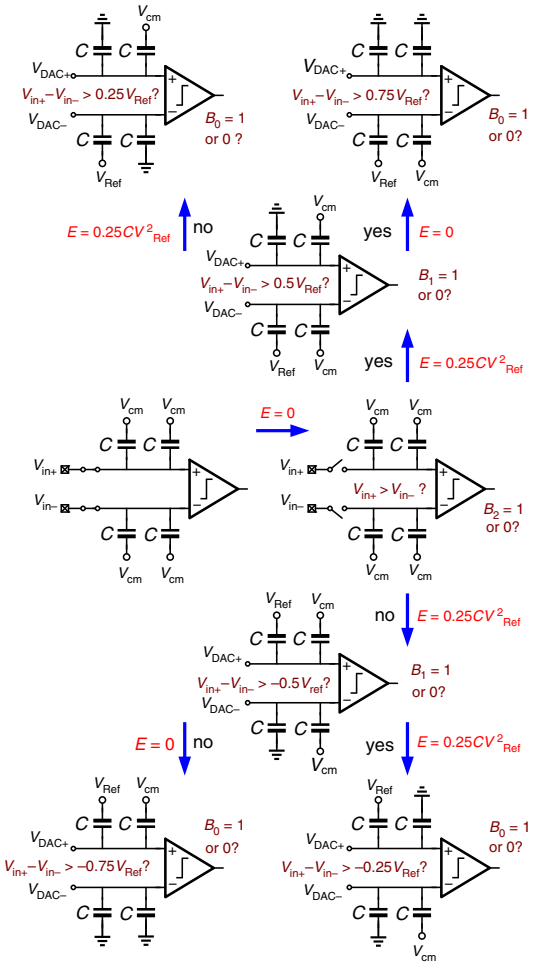

Fig. 1 *Proposed DAC switching scheme of 3-bit ADC*

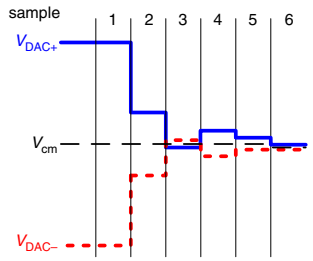

Fig. 2 *Waveform of proposed DAC switching scheme for typical 6-bit SAR ADC*

Analysis of dependency on accuracy of V_{cm}: The bottom plate of a specific capacitor in one capacitor array is switched from V_{cm} to V_{Ref} and in the other capacitor array it is switched from V_{cm} to the ground during each phase except the LSB one. Hence, any variation of V_{cm} has no effect on the ADC operation till the LSB phase. For instance, if this capacitor in the upper and lower capacitor arrays is switched to the ground and V_{Ref}, respectively, and V_{cm} to be $V_{cm}+\Delta V$, then in the extraction of the nth-bit, we have

$$V_{DAC+}(n) = V_{DAC+}(n-1) - 2^{-(n-1)}(V_{cm} + \Delta V) \quad (1)$$

$$V_{DAC-}(n) = V_{DAC-}(n-1) + 2^{-(n-1)}(V_{ref} - V_{cm} - \Delta V) \quad (2)$$

$$V_{DAC}(n) = V_{DAC+}(n) - V_{DAC-}(n) = V_{DAC}(n-1) - 2^{-(n-1)}\,V_{Ref} \quad (3)$$

where the range of 'n' for a fully-differential N-bit SAR ADC is from 2 to $(N-1)$ (2nd-MSB to 2nd-LSB) and V_{DAC} is the differential output of the DAC. As can be seen from the relation (3), any change in V_{cm} does not affect the bit generation. In fact, an inaccurate transition in one capacitor array compensates for the inaccuracy of another path as proved in (3). As a result, the proposed switching scheme has no dependency on the accuracy of V_{cm} except in the

LSB generation where only one of the capacitor arrays is switched. However, in [4, 5], during each conversion cycle except the MSB, only one capacitor array is switched from V_{cm} to the ground or V_{Ref}, and thus, this imprecise transition because of the inaccuracy of V_{cm} remains uncompensated.

Comparison of switching schemes: The behavioural simulations of switching techniques reported in [2, 3] and this new scheme for a fully-differential 10-bit SAR ADC were performed in MATLAB and the results of switching energy against the output codes are illustrated in Fig. 3. The average switching energy for the proposed fully-differential 10-bit SAR ADC is $84.9CV^2_{Ref}$ which amounts to a reduction of 93.7% in the switching energy compared with the conventional structure. In Table 1, the main features of the proposed scheme and the schemes of [2–5] are compared. As can be seen, the average switching energy of the proposed fully-differential 10-bit SAR ADC is half that of the V_{cm}-based SAR ADC [3]. Although, the switching energy of this work is more than that of [4, 5], it needs only a simple digital circuit and the ADC performance has no dependency on the precision of V_{cm} except the LSB and this is an important achievement since the third reference voltage realisation with the overall ADC accuracy would be power hungry. Moreover, in the proposed switching scheme, the common-mode voltage at the comparator input is constant except in the LSB transition, making the comparator's realisation more relaxed.

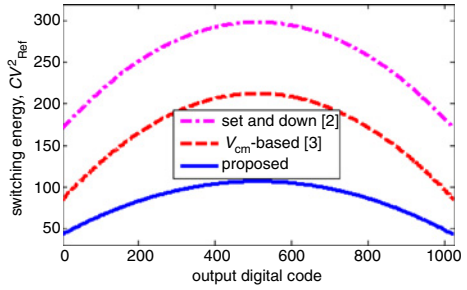

Fig. 3 *Switching energy against output digital codes*

Table 1: Comparison of several switching schemes for 10-bit ADC

Switching scheme	Average switching energy (CV^2_{Ref})	Energy saving	Area reduction	Logic complexity	Dependency on the accuracy of V_{cm}
Conventional	1363.3	Reference	Reference	Low	–
Set and down [2]	255.5	81.2	50%	Low	–
V_{cm}-based [3]	170.2	87.5	50%	Low	No
Tri-level [4]	42.4	96.89	75%	Medium	Very high (all bits except MSB)
V_{cm}-based monotonic [5]	31.9	97.66	75%	Medium	Very high (all bits except MSB)
This work	84.9	93.7	75%	Low	Very low (only LSB)

Conclusion: An energy efficient DAC switching scheme for SAR ADCs is proposed resulting in 93.7% less switching energy and a 75% reduction in total capacitor size compared with the conventional SAR ADC. In this scheme, the comparator input common-mode voltage is almost constant and the ADC operation is robust against variations in the third reference voltage (V_{cm}) expect in the LSB transition. In addition, it needs only a simple logic circuit to realise a successive operation. Hence, the proposed switching technique can be used in the realisation of low power and small area SAR ADCs.

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One or more of the Figures in this Letter are available in colour online.

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