A ΣΔ-FIR-DAC for Multi-Bit ΣΔ Modulators

Hossein Pakniat and Mohammad Yavari, *Member, IEEE*

***Abstract*—In this paper, a new digital-to-analog converter (DAC) is proposed for multi-bit continuous-time sigma-delta modulators (ΣΔMs). This ΣΔ-finite-impulse-response-DAC (ΣΔ-FIR-DAC) digitally converts the multi-bit output of the quantizer to a 1.5-bit signal at a higher rate and then injects it to the modulator loop filter by using a 1.5-bit DAC. An FIR filter is merged into 1.5-bit DAC to improve the clock jitter insensitivity. Furthermore, a new implementation of FIR-DAC is presented to reduce the output rate of ΣΔ-FIR-DAC down to the original rate of the modulator. This reduced rate ΣΔ-FIR-DAC (RR-ΣΔ-FIR-DAC) can be used in both continuous-time and discrete-time ΣΔMs. Theoretical analysis supported by simulation results are provided to evaluate the performance, clock jitter immunity and robustness against DAC elements mismatch in the proposed modulators.**

***Index Terms*—Sigma-delta modulators, multi-bit DAC, FIR-DAC, ΣΔ-FIR-DAC, reduced rate ΣΔ-FIR-DAC.**

I. Introduction

MULTI-BIT sigma-delta modulators (ΣΔMs) have various advantages over single bit ones such as the improved stability and accuracy and reduced sensitivity to the clock jitter. Besides, the multi-bit feedback signal results in reduced swing and slew-rate in integrators, and hence, the multi-bit modulators require relaxed amplifiers to realize the loop filter [1], [2]. However, they are sensitive to the mismatch among the DAC unit elements resulting in a degraded signal-to-noise plus distortion ratio (SNDR). In reality, the modulator's resolution can be limited by the linearity of the outermost feedback multi-bit DAC.

Several solutions have been introduced to alleviate this problem. Two common solutions are the dynamic element matching (DEM) [3]–[5] and the digital calibration [6], [7]. However, the performance of DEM techniques is degraded when the modulator's oversampling ratio (OSR) is decreased [6], [8] and digital background calibration techniques need more digital hardware to realize.

Dual quantization is another solution, where the outer feedback signal is digitally quantized to a 1-bit signal and thereby solves the outer loop's DAC nonlinearity [9]–[12]. Nonetheless, this technique has two main drawbacks. Firstly, in order to cancel the digital quantization error, additional feedback paths [9]–[11] or a very high OSR are required [12]. Secondly, in continuous-time (CT) ΣΔMs, the 1-bit outer feedback DAC is more sensitive to the clock jitter [11]. Although the sensitivity to the clock jitter can be alleviated by using a finite impulse response (FIR) filter [11], but additional error cancellation feedback paths are still required.

Manuscript received July 14, 2012; revised November 06, 2012 and December 16, 2012; accepted December 22, 2012. Date of publication April 11, 2013; date of current version August 26, 2013. This paper was recommended by Associate Editor J. Barreiro da Silva.

The authors are with the Integrated Circuits Design Laboratory, Department of Electrical Engineering, Amirkabir University of Technology, Tehran, Iran (e-mail: myavari@aut.ac.ir.).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TCSI.2013.2244433

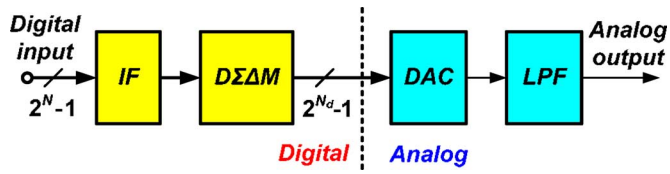

Fig. 1. General block diagram of a ΣΔ-DAC.

As another solution, the multi-bit feedback signal can be transferred to a PWM signal by using a digital block [8], [13], or the whole multi-bit quantizer can be replaced by a PWM-based quantizer [14], [15]. Consequently, the modulator needs a linear single element DAC, while the corresponding two-level (or three-level) PWM signal has a multi-bit nature. However, for an N-bit quantizer, the PWM block requires a time-resolution 2^N times more than that of the modulator. Hence, the maximum admissible clock jitter is strictly limited [8]. Furthermore, the linearity of digital PWM block depends on the matching of its corresponding clock phases [8].

In this paper, a new DAC is proposed to solve the linearity problem in multi-bit modulators while preserving their clock jitter immunity. In the outermost feedback path, a sigma-delta DAC (ΣΔ-DAC) takes the place of multi-bit DAC. This DAC converts the multi-bit signal of the main loop to a higher rate 1.5-bit signal, where the differential implementation of a 1.5-bit DAC is inherently linear [16]. The clock jitter immunity of the modulator is improved by using an FIR filter combined with 1.5 bit DAC which is named as the FIR-DAC [13]. Moreover, a new implementation of FIR-DAC is proposed to reduce the rate of ΣΔ-FIR-DAC down to the original rate of the main modulator. This proposed reduced rate ΣΔ-FIR-DAC (RR-ΣΔ-FIR-DAC) can be used in both CT and discrete-time (DT) ΣΔMs.

The paper is organized as follows. The operation of ΣΔ-DAC is briefly reviewed in Section II. The proposed CT-ΣΔMs with ΣΔ-FIR-DAC is presented in Section III. Section IV introduces the proposed RR-ΣΔ-FIR-DAC. The robustness against DAC elements mismatch and the clock jitter immunity in proposed DACs are examined in Sections V and VI, respectively. The proposed ΣΔMs are compared with conventional multi-bit modulators in Section VII. Finally, Section VIII concludes the paper.

II. Operation of ΣΔ-DAC

ΣΔ-DACs benefit from both the oversampling and noise-shaping techniques to realize a high resolution DAC [1]. It converts a high resolution multi-bit digital signal at the rate of f_s to an analog signal by using a low resolution DAC at the

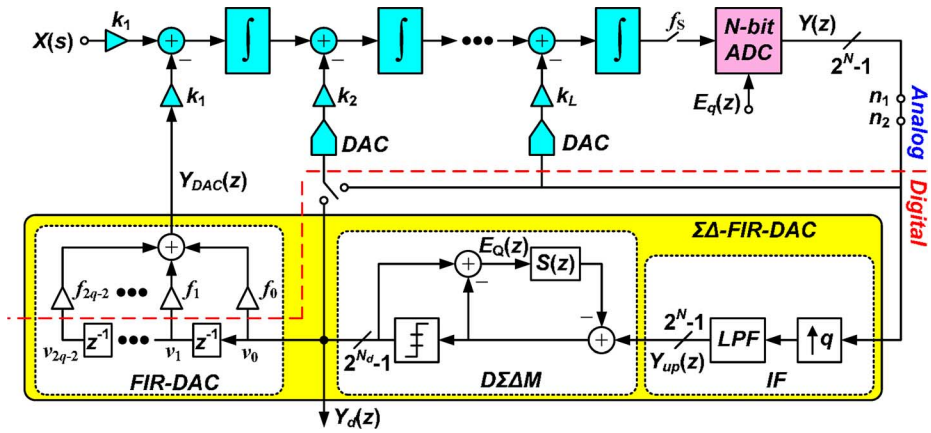

Fig. 2. Proposed CT-ΣΔM with ΣΔ-FIR-DAC.

rate of $q \times f_s$, where q is the OSR of ΣΔ-DAC. As shown in Fig. 1, a ΣΔ-DAC comprises of four main building blocks: an interpolation filter (*IF*), a digital sigma-delta modulator (DΣΔM), a low resolution DAC, and an analog low-pass filter (*LPF*).

The *IF* block, firstly raises the sampling frequency to $q \times f_s$ to allow the subsequent noise shaping, and then suppresses the spectra replicas centered at $f_s, 2f_s, \ldots, (q-1) \times f_s$. The side-band suppression improves the dynamic range of DΣΔM by attenuating the out-of-band signals without affecting the base-band input signal spectrum [1]. High orders of *IF* impose a significant latency, which is not desired when the ΣΔ-DAC is used in the feedback path of ΣΔMs. An up-sampling by a factor of q usually needs inserting $(q-1)$ zeros between two adjacent samples. Here, the up-sampling is done by repeating each sample for q times. This is equivalent to filter the up-sampled data by a sinc filter, $(1-z^{-q})/(1-z^{-1})$, and thus, the spectra replicas centered at $f_s, 2f_s, \ldots, (q-1) \times f_s$ are attenuated. In order to implement the *IF* block, the DΣΔM samples its input signal for q times during the modulator's time period, T_s.

The DΣΔM is used to reduce the word length of its input signal. If the word length is reduced to 1.5-bit, then the subsequent differential DAC would be inherently linear [16]. Finally, the LPF suppresses the out-of-band noise of DΣΔM.

III. Proposed ΣΔ-FIR-DAC

Fig. 2 illustrates a CT-ΣΔM, where the proposed ΣΔ-FIR-DAC is employed in the outermost feedback path and $Y_d(z)$ is selected as the modulator output signal. The up-sampler of ΣΔ-FIR-DAC converts the N-bit output signal of ADC, $y(\cdot)$, to a higher rate multi-bit signal, $y_{\rm up}(\cdot)$, as

$$y_{\rm up}(nq+k) = y(n), \quad (k = 0, 1 \ldots, q-1). \tag{1}$$

A delay free and unity signal transfer function DΣΔM is used in Fig. 2 in which the quantizer passes both the sign and most significant bits and truncates the other bits. Therefore, it adds a negligible delay to the system due to the input adder. The feedback loop of DΣΔM shapes out the quantization noise.

By using a linear model, the modulator output signal is given by

$$\begin{aligned} Y_d(z) &= Y_{\rm up}(z) + (1 - S(z)) \times E_Q(z) \\ &= (STF(z^q) \times X(z^q) + {\rm NTF}(z^q) \times E_q(z^q)) \\ &\quad \times \frac{(1-z^{-q})}{(1-z^{-1})} \\ &\quad + {\rm NTF}_d(z^q) \times E_Q(z)(1 - S(z)) \end{aligned} \tag{2}$$

where $X(z)$, $E_q(z)$ and $E_Q(z)$ are the input signal, ADC's quantization noise, and digital quantization noise, respectively. $STF(z)$, ${\rm NTF}(z)$, and ${\rm NTF}_d(z)(1 - S(z))$ denote (the discrete-time equivalent of) modulator input signal, quantization noise, and digital quantization noise transfer functions, respectively. $E_Q(z)$ and the other errors of DΣΔM (e.g., the finite word length error) are shaped by ${\rm NTF}_d(z)$. Besides, by choosing $S(z) = z^{-1}$ and $S(z) = 2z^{-1} - z^{-2}$, $E_Q(z)$ is shaped by an additional first or second order high-pass filter, respectively. The DAC in the second loop can be driven either by $y(\cdot)$ or $y_d(\cdot)$, and hence, ${\rm NTF}_d(z)$ can be a first or a second order high-pass filter, respectively. The conventional DACs at the other feedback paths are driven by $y(\cdot)$.

Although the differential implementation of a 1.5-bit DAC (driven by $y_d(\cdot)$) is inherently linear [16], but such DAC is much more sensitive to the clock jitter compared to a conventional multi-bit DAC. Thus, $Y_d(z)$ is injected to the first integrator through an FIR filter embedded in the body of FIR-DAC. As a result, the difference between two adjacent DAC output samples is reduced, which improves the clock jitter immunity of the 1.5-bit DAC [11], [13]. The FIR filter, i.e., $F(z)$, is implemented pseudo digitally in the body of the 1.5-bit DAC [17] making an FIR-DAC. The filtering portion of the FIR-DAC is shown in Fig. 2. In this figure, the delay line is implemented by $2q-2$ latches. The analog parts of FIR-DAC (the adder and the coefficients, $f_0, f_1 \ldots, f_{2q-2}$) are implemented in the body of first integrator (e.g., through weighted current cells injected to the amplifier's virtual ground). $F(z)$ is designed to be a low-pass FIR filter with a -3 dB cutoff frequency at $f_s/2$. Also, $F(z)$ should be practically realizable with DAC elements.

As will be explained in Section IV, $F(z)$ is selected as a sinc^2 filter

$$F(z) = \left(\frac{(1-z^{-q})}{q(1-z^{-1})}\right)^2. \tag{3}$$

The OSR of CT-ΣΔM is p and the up-sampler increases it by a factor of q, and hence, related to the signal bandwidth of the main modulator, the ΣΔ-FIR-DAC has an OSR of $p \times q$.

Although the ΣΔ-FIR-DAC operates at a higher rate compared to the main modulator, but according to the simulation results, the amplifiers used in the modulator require the same analog specifications including the gain-bandwidth (GBW), output swing, and slew rate. In fact, the high frequency components of $y_d(\cdot)$ are filtered in the modulator loop filter like any other out-of-band signal, and hence, the integrators do not follow these fast transitions. This is a well-known behavior of CT-ΣΔMs named as inherent anti-aliasing property. The order of this inherent *LPF* is as high as the noise-shaping order of the modulator [1]. Furthermore, in the main loop, the FIR-DAC significantly smoothes the fast variations of $y_d(\cdot)$. However, the limited GBW in the first integrator amplifier may lead to a high-frequency signal-dependent ripple on its virtual ground [18]. This ripple is due to the out-of-band frequency components leaked through the FIR-DAC. Therefore, the output impedance of DAC current cells should be high enough such that their output current would be independent on this ripple.

A. The Effects of ΣΔ-FIR-DAC on CT-ΣΔMs

The up-sampling, the additive-shaped quantization noise of DΣΔM, and the FIR filter affect the performance of proposed modulator with ΣΔ-FIR-DAC. The sampler adjacent to CT-ΣΔM quantizer (Fig. 2) automatically samples down the filtered version of $Y_d(z)$, and hence, the spectra replicas of $|Y(f)|^2$ get back to their original frequency interval exactly matched on power spectral density (PSD) of $|Y(f)|^2$.

The *LPF* of FIR-DAC in series with inherent *LPF* of CT-ΣΔM adequately suppresses the additive noise, which is shaped by $|1 - S(f)|^2$ at frequencies higher than $f_s/2$ prior to the modulator sampling (discussed in Section III-B). Just in modulator bandwidth, the shaped noise of digital quantizer is remained. Additional noise in signal bandwidth, $[0, f_s/2p]$, and modulator bandwidth, defined here as $[0, f_s/2]$, reduces the modulator's SNDR and dynamic range (DR), respectively. As explained in Section III-C, by a suitable design, this noise will be negligible in both signal and modulator bandwidths.

The FIR filter is designed with a -3 dB cutoff frequency at $f_s/2$ to transfer the modulator frequency components. The delay effects of FIR filter will be discussed in Section III-D.

B. Anti-Aliasing Filter of CT-ΣΔM as LPF for ΣΔ-FIR-DAC

The ΣΔ-FIR-DAC has an output signal rate which is q times of modulator sampling rate with an L_d noise shaping order. To reduce the output sampling rate of ΣΔ-FIR-DAC, a q-tap K-th order ($K \geq L_d + 1$) sinc filter is a suitable anti-aliasing filter [19]. Due to the stability consideration in DΣΔM, $L_d \leq 2 \leq L$, and consequently, $K = 3$ is an enough order for the sinc filter. The frequency response of inherent *LPF* of an L-th order CT-ΣΔM is $(\sin(\pi f/f_s)/(\pi f/f_s))^L$ [1], whereas the frequency response of a q-tap L-th order sinc filter is $(\sin(\pi f/f_s)/(q \times \sin(\pi f/qf_s)))^L$. Both filters have the same -3 dB cutoff frequency at $f_s/2$ and the same pass-band characteristic ($q \times \sin(\pi f/qf_s) \approx \pi f/f_s$ for $0 \leq f \leq f_s/2$), while the former has a better out-of-band suppression since $\pi f/f_s > q \times \sin(\pi f/qf_s)$ for $f_s/2 \leq f \leq q \times f_s/2$. Consequently, the inherent *LPF* filter of proposed CT-ΣΔM prepares a suitable L-th order filtering for ΣΔ-FIR-DAC. Furthermore, the FIR filter of Fig. 2 increases this order by two, and hence, the overall order of the anti-aliasing filter is $K = L + 2 \geq 3$. Thus, in the future analysis, it is assumed that the out-of-band frequency components of ΣΔ-FIR-DAC are sufficiently suppressed prior to the sampler of main modulator (adjacent to its quantizer).

C. The Residual Shaped Noise of Digital Quantizer

In this Section the ΣΔ-FIR-DAC is designed such that its shaped digital quantization noise has a negligible effect on the main modulator performance.

According to Fig. 2, the quantization noise transfer function, $\mathrm{NTF}(s)$, is given by

$$\mathrm{NTF}(s) = \frac{s^L}{s^L + k_L\, f_s\, s^{L-1} + \cdots + k_2 f_s^{L-1} s + k_1 f_s^L} \tag{4}$$

where L is the order of modulator. In modulator bandwidth, $[0, f_s/2]$, $\mathrm{NTF}(s)$ is equal to an L-th order high-pass filter, while its discrete-time equivalent is approximately $(1/k_1) \times (1 - z^{-1})^L$, and consequently, $|\mathrm{NTF}(f)|^2 = (2^{2L}/k_1^2)\sin^{2L}(\pi f/f_s)$.

On the other hand, $\mathrm{NTF}_d(s)$ is as follows:

$$\mathrm{NTF}_d(s) = \frac{s^L + k_L\, f_s\, s^{L-1} + \cdots + k_2 f_s^{L-1} s}{s^L + k_L\, f_s\, s^{L-1} + \cdots + k_2 f_s^{L-1} s + k_1 f_s^L}. \tag{5}$$

In modulator bandwidth, $[0, f_s/2]$, $\mathrm{NTF}_d(s)$ is a first order high-pass filter and can be approximated by its discrete-time equivalent as $(k_2/k_1) \times (1 - z^{-1})$ resulting in $|\mathrm{NTF}_d(f)|^2 \approx 2^2 \times (k_2^2/k_1^2) \times \sin^2(\pi f/f_s)$. It should be noted that in relation (5) it is assumed that the DAC of second loop (Fig. 2) is driven by $y(\cdot)$. If this DAC is driven by $y_d(\cdot)$, then $|\mathrm{NTF}_d(f)|^2 \approx 2^4 \times (k_3^2/k_1^2)\sin^4(\pi f/f_s)$.

For a busy (i.e., rapidly and randomly varying) input signal, the quantization error of both quantizers in Fig. 2 can be approximated with a zero-mean white noise [1]. By assuming a flat pass-band frequency response of sinc filter in (2), the one-sided PSD of $Y_d(f)$ in modulator bandwidth is approximately given by

$$\begin{aligned} |Y_d(f)|^2 = {} & |STF(f) \cdot X(f)|^2 \\ & + \left(\frac{1}{k_1}\right)^2 \frac{V_{FS}^2 \times 2^{2L}}{6 f_s\, (2^N)^2} \sin^{2L}\left(\frac{\pi f}{f_s}\right) \\ & + \frac{V_{FS}^2 \cdot 2^{2(L_d+1)}}{6\, q\, f_s (2^{N_d})^2} \sin^{2L_d}\left(\frac{\pi f}{q\, f_s}\right) \\ & \cdot \left(\frac{k_2}{k_1}\right)^2 \sin^2\left(\frac{\pi f}{f_s}\right),\ 0 \leq f \leq f_s/2 \end{aligned} \tag{6}$$

where N is the number of quantization bits and V_{FS} is the full scale voltage in both quantizers. In this equation, the third term represents the PSD of digital quantizer noise shaped by multiplication of $|\mathrm{NTF}_d(f)|^2$ and $|1-S(f)|^2$. To prevent the destructive effect of $\Sigma\Delta$-FIR-DAC on the modulator performance, the integral of the third term in (6) must be negligible compared to the integral of the second term over both signal and modulator bandwidths.

N_d, L_d, and q are the design parameters of $\Sigma\Delta$-FIR-DAC. By considering the linearity of DAC, the maximum value of $N_d(N_d = \log_2(3))$, corresponding to a lower quantization noise, is selected. A minimum value of q can be obtained by assuming the integral of the third term in (6) to be much less than (1/10 or less) that of the second term over the signal bandwidth $[0\ \ f_s/(2p)]$ as

$$q \geq \left(10 \cdot k_2^2 \frac{2L+1}{2(L_d+1)+1} \cdot \frac{2^{2N}}{2^{2N_d}} \left(\frac{p}{\pi}\right)^{2(L-L_d-1)}\right)^{1/(2L_d+1).} \tag{7}$$

Note that in order to obtain the above equation, the approximation of $\sin(x) \approx x$ is used in both second and third terms of (6) for both $f \ll f_s$ and $f/q \ll f_s$.

Similar to (7), another minimum value of q is obtained by assuming the integral of third term in (6) to be much less than (1/10) that of the second term over the $[0\ \ f_s/2]$ frequency interval as

$$q \geq \left(10 \cdot k_2^2 \cdot \frac{2^{2N} \times 2^{2(L_d+1)} C(L_d+1)}{2^{2N_d} \times 2^{2L} \times C(L)}\right)^{1/(2L_d+1)} \tag{8}$$

where $C(L) = \int_o^{\pi/2} \sin^{2L}(x)\,dx = (\sqrt{\pi}\,\Gamma(L+1/2))/(2\,\Gamma(L+1))$ and $\Gamma(\cdot)$ is the gamma function. $C(L)$ is equal to $\pi/2^2, 3\pi/2^4, 10\pi/2^6, 35\pi/2^8$, and $63\pi/2^9$ for $L = 1, 2, 3, 4$, and 5, respectively. Note that in order to obtain the above equation, the approximation of $\sin^{\zeta}(x/q) \approx (1/q^{\zeta}) \times \sin^{\zeta}(x)$ is used in third terms of (6) for $q \geq 2$.

Two values for q are suggested in relations (7) and (8). Their maximum value should be selected in order to satisfy both inequalities. In both suggested values of relations (7) and (8), the OSR of $\Sigma\Delta$-FIR-DAC, q, is proportional to $2^{N/(L_d+0.5)}$.

According to relations (7) and (8), increasing L_d exponentially decreases q, and thus, the clock frequency of digital circuits is decreased. On the other hand, the D$\Sigma\Delta$M of Fig. 2 with $L_d \leq 2$ and output bit length of 1.5 has warranted stability. The stability consideration in D$\Sigma\Delta$M with $L_d > 2$ leads to an infinite-impulse-response (IIR) *NTF* [1]. An IIR *NTF* requires more complex digital circuits compared to its FIR counterpart. Therefore, $L_d = 2$ is selected here.

Besides the quantization noise in D$\Sigma\Delta$M, the effects of its finite word length should be also considered. Fortunately, the errors of D$\Sigma\Delta$M are shaped by NTF_d. So, the word length is designed such that the in-band noise caused by finite precision arithmetic is below the original in-band noise of the modulator [1], resulting in

$$M \geq N + 0.5 \cdot \log_2\left(\delta^2 \frac{2L+1}{(2L'+1)} \cdot \left(\frac{p}{\pi}\right)^{2(L-L')}\right) \tag{9}$$

where M is the required word length in D$\Sigma\Delta$M, L' (=1 or 2) is the noise shaping order of NTF_d, and $\delta = k_2$ or k_3 for $L' = 1$ or 2, respectively. As mentioned before, the order of NTF_d depends on how the signal to be injected into the second loop DAC. $L' = 1$ or 2 when $y(\cdot)$ or $y_d(\cdot)$ is injected into the second loop DAC, respectively. Relation (9) suggests that $M = N + 7$ and $M = N + 3$ for $L' = 1$ and 2, respectively. This means that by injecting $y_d(\cdot)$ into the second loop DAC, a lower word length is required. In this case, a conventional multi-bit DAC is replaced by a 1.5-bit DAC at q-times (2-times) higher sampling rate. Based on analytical results of Section VI-B, the clock jitter noise of this DAC does not affect the modulator's performance. Also according to the simulation results, the required ω_{GBW} of the second amplifier is not considerably increased. However, the noise of digital quantizer permeates into the loop filter more than before resulting in reduced dynamic range. In other words, the aforementioned change increases the required value of q.

D. The Effects of Excess Loop Delay

In modulator shown in Fig. 2, the main sources of excess loop delay are the delay of quantizer, multi-DAC, finite GBW of amplifiers, and finally the delay of FIR-DAC. Like the other CT-$\Sigma\Delta$Ms, the proposed modulator is not robust against excess loop delay (the delay which affects all feedback paths), and hence, it should be compensated for.

The FIR-DAC introduces a time delay in the outer loop of modulator which should be considered. Each element of delay line in FIR-DAC has a delay of T_s/q. Calculating the phase of $F(z)$, introduced in (3), its corresponding delay is $(q-1) \times T_s/q$. Thus, the maximum delay of FIR-DAC is less than T_s. The effect of outer loop delay on modulator stability is widely discussed in [20]. In modulator of Fig. 2, thanks to the other feedback paths, the outer loop delay does not directly lead to an excess loop delay. Based on the simulation results of this modulator, there is no stability problem, while the outer loop has a delay up to $2.3 \times T_s$.

All delays including the FIR-DAC one are compensated in this Sect. The summation of all delays excluding the FIR-DAC is assumed to be one sampling period (T_s), where 60% of this delay is considered for both quantizer and multi-bit DACs and the remained 40% delay assumed to be caused by the limited GBW of amplifiers. To compensate for these delays, a fast DAC loop around the quantizer is utilized [2].

The impulse response of modulator's loop is used to investigate the effect of excess loop delay [21]. For this purpose, the modulator's loop is disconnected in nodes n_1 and n_2 in Fig. 2. A discrete-time impulse signal is exerted to n_2 and the response is observed at n_1. Fig. 3 illustrates the impulse response of modulator's loop in two cases. In the first case, an ideal loop with no delay is considered, while in the second case, all delays including the FIR-DAC are considered and compensated for. In this simulations, the third-order CT-$\Sigma\Delta$M of Fig. 2 with 3-bit quantizer $(N = 3)$ and OSR of $p = 32$ was used. For ideal case, the coefficients are similar to the modulator reported in [20] as $k_1 = 0.3, k_2 = 0.8, k_3 = 1$. In second case, a T_s delay plus the delay of FIR-DAC was considered and compensated for by using a fast DAC around the quantizer [2]. The gain of this DAC is $k^* = 1.45$ and the modified values of other gains

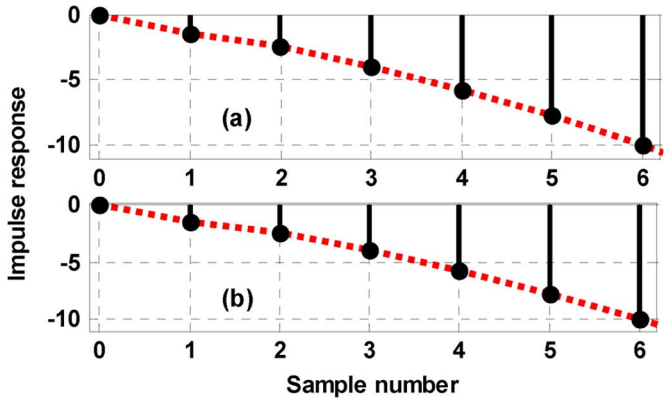

Fig. 3. Impulse response of the proposed modulator: (a) ideal loop (no delay) and (b) real loop by compensating for all possible delays.

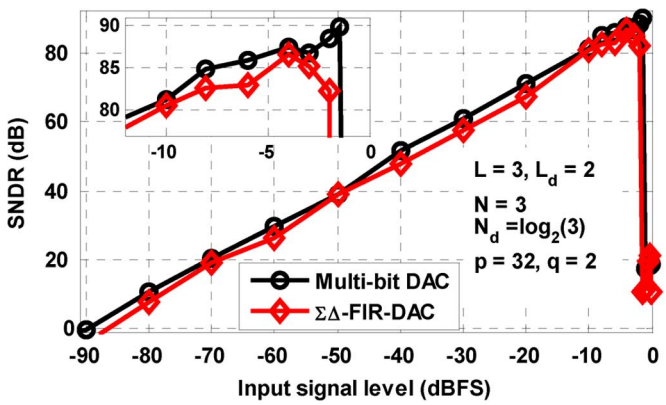

Fig. 4. Simulated SNDR versus the input signal amplitude.

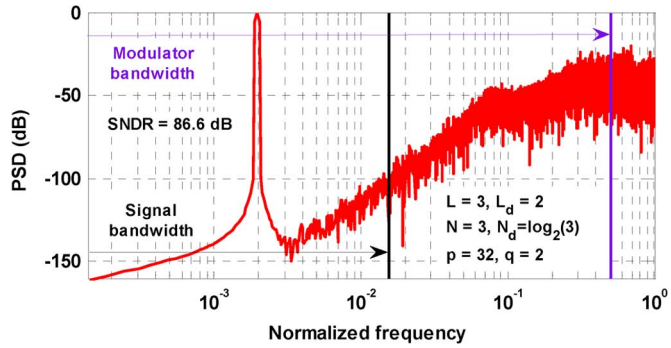

Fig. 5. Simulated power spectral density of the proposed modulator after the compensation for all possible delays.

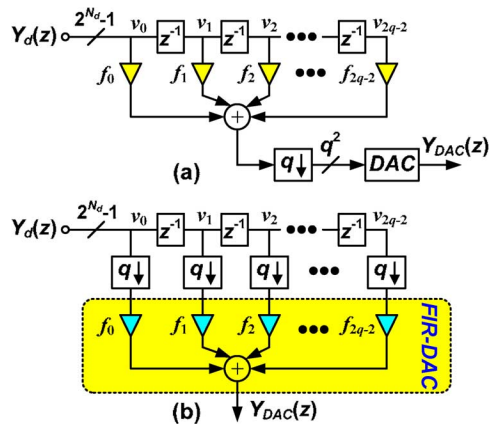

Fig. 6. Two different implementations of the set of FIR filter, down-sampler and DAC: (a) conventional and (b) proposed.

are $k_2 = 1.25$ and $k_3 = 2$, while k_1 remains unchanged. As shown in Fig. 3, both cases have the same impulse response.

E. Simulation Results of Modulator With ΣΔ-FIR-DAC

The modulator introduced in simulation of Fig. 3 is selected for system-level simulations (all delays except FIR-DAC delay and their corresponding compensations are removed). The input signal was a -3 dBFS sinusoidal at the frequency of $f_s/128$. For $N = 3, q = 2.14$ is suggested by both relations (7) and (8). However, the integer value of $q = 2$ was selected. A second-order, $L_d = 2$, DΣΔM$(S(z) = 2z^{-1} - z^{-2})$ with $q = 2$ and output bit length of $N_d = \log_2(3)$ was used for ΣΔ-FIR-DAC. $F(z)$ is a q-tap second-order sinc filter introduced in (3). The presented parameters are also used in all future simulations of this paper, while in all simulations 32768 points FFT with a Hanning window was used for spectral estimation.

Fig. 4 shows the simulated SNDR versus input signal amplitude for the proposed modulator with ΣΔ-FIR-DAC and the conventional multi-bit modulator in ideal conditions. As is seen, in ideal conditions, both modulators have approximately the same performance.

Fig. 5 shows the simulated output PSD of modulator corresponding to the maximum SNDR at the input frequency of $f_s/512$. In this simulation, all delays are considered and compensated for.

IV. Proposed Reduced Rate ΣΔ-FIR-DAC

As illustrated in Fig. 2, the down sampling operation of ΣΔ-FIR-DAC takes place at the sampling point of the main modulator, where the out-of-band noise of DΣΔM is suppressed by both the FIR filter and inherent LPF of CT modulator. However, there is no inherent anti-aliasing filter in DT ΣΔMs and the high rate output signal of ΣΔ-FIR-DAC cannot be directly injected to its integrator. In this section, a technique is proposed to reduce the rate of ΣΔ-FIR-DAC, and hence, the proposed RR-ΣΔ-FIR-DAC can be employed in both DT and CT ΣΔMs.

A. Fundamental of Operation

In proposed ΣΔ-FIR-DAC, a decimation filter can be used to reduce the rate of $Y_d(z)$ prior to its injection to the first integrator. The FIR filter, which is used to reduce the clock jitter sensitivity of 1.5-bit DAC, can be designed properly to play the role of decimation filter as well. According to Fig. 6(a), the decimation filter decreases the rate of $Y_d(z)$ by a factor of q, while the out-of-band noise is adequately suppressed by the FIR filter. However, a multi-bit DAC is required to inject the multi-bit output signal of the FIR filter to the first integrator and so the linearity problem appears again [22].

Implementing the FIR-DAC as proposed in Fig. 6(b) solves this problem. In Fig. 6(b), the down-sampler of Fig. 6(a) is performed before the gain coefficients $(f_0, f_1 \ldots f_{2q-2})$.

This admissible displacement replaces the multi-bit DAC of Fig. 6(a) with an FIR-DAC. Unlike the multi-bit DAC of Fig. 6(a), the DAC elements mismatch in Fig. 6(b), leads to the mismatch in FIR filter coefficients which only modifies its frequency response [13], [17], [23]. The proposed ΣΔM with RR-ΣΔ-FIR-DAC is similar to the modulator of Fig. 2, while its FIR-DAC is replaced with the FIR-DAC of Fig. 6(b).

As mentioned in the previous section, in order to reduce the output signal rate of DΣΔM by a factor of q, a q-tap K-th order sinc filter with $K \geq L_d + 1 = 3$ is a suitable anti-aliasing filter [19]. Therefore, a sinc^3 filter is required as the decimation filter in RR-ΣΔ-FIR-DAC. For FIR implementation, the value of coefficients in a sinc^3 filter distributes in a wide range such that the ratio of the maximum value to the minimum value is in the order of q^2. However, for a sinc^2 filter, this ratio is in the order of q. Therefore, considering the practical limitation of FIR-DAC, $F(z)$ is selected as a sinc^2 filter with a unity gain at DC introduced in (3).

The number of taps in the sinc filter is selected equal to the OSR of DΣΔM. The introduced $F(z)$ is employed as the FIR filter in both ΣΔ-FIR-DAC and RR-ΣΔ-FIR-DAC. Using a sinc^2 filter instead of a sinc^3 filter in the RR-ΣΔ-FIR-DAC ($K = L_d = 2$ instead of $K = L_d + 1 = 3$) causes the out-of-band noise to fold into the modulator's bandwidth. As a result, the third term in (6) is multiplied by q [19]. Hence, the suggested q for ΣΔ-FIR-DAC in relations (7) and (8) are modified for RR-ΣΔ-FIR-DAC. These modified values are obtained by assuming the integral of DΣΔM quantization noise to be $1/(10 \times q)$ of ideal modulator's noise in both signal and modulator bandwidths, respectively, as

$$q \geq \left(10 \cdot k_2^2 \cdot \frac{(2L+1)}{2(L+L_d)+1} \cdot \frac{2^{2N}}{2^{2N_d}} \cdot \left(\frac{\pi}{p}\right)^{2L_d} \right)^{1/(2L_d)} \quad (10)$$

$$q \geq \left(10 \cdot k_2^2 \cdot \frac{2^{2N} \times 2^{2(L_d+1)} C(L_d+1)}{2^{2N_d} \times 2^{2L} \times C(L)} \right)^{1/(2L_d)} \quad (11)$$

where the parameters and the approximations assumed in (10) and (11) are similar to those in (7) and (8), respectively. Relations (10) and (11) suggest two values of q for RR-ΣΔ-FIR-DAC and their maximum value should be selected.

It should be noted that in modulator with RR-ΣΔ-FIR-DAC, the effects of both finite word length and excess loop delay are similar to the modulator with ΣΔ-FIR-DAC.

B. Simulation Results

Similar to Fig. 4, Fig. 7 shows the simulated SNDR versus the input signal amplitude for two modulators in ideal conditions: the multi-bit modulator and the modulator with RR-ΣΔ-FIR-DAC. For $N = 3, q = 2.6$ are suggested by both relations (10) and (11). However, for the sake of simplicity, the integer value of $q = 2$ was selected at the cost of a little SNDR and dynamic range degradation.

Fig. 8 compares the simulated SNDR versus the normalized gain-bandwidth $(\omega_{\mathrm{GBW}}/2\pi f_s)$ of both first and second amplifiers in three architectures: modulators with multi-bit DAC, ΣΔ-FIR-DAC and RR-ΣΔ-FIR-DAC. In all cases, the gain-bandwidth of the third amplifier was considered $5\pi f_s$ rad/sec to prevent the instability of modulators due to the excess loop delay. The ΣΔM of Fig. 2 was simulated using the parameters introduced in Section III-E with a -3 dBFS sinusoidal input signal. As is seen, in all cases, a gain-bandwidth of about $2\pi f_s$ is sufficient. Although the clock rate of the proposed ΣΔ-FIR-DAC is more than that of the main modulator, but the power and speed requirements in the amplifiers are the same as the conventional multi-bit modulators.

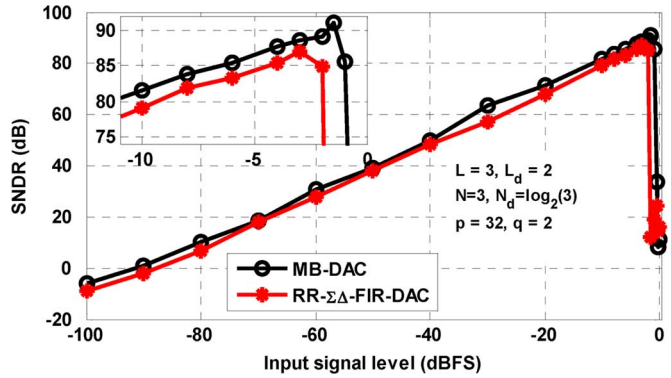

Fig. 7. Simulated SNDR versus the input signal amplitude for multi-bit modulator and the modulator with RR-ΣΔ-FIR-DAC.

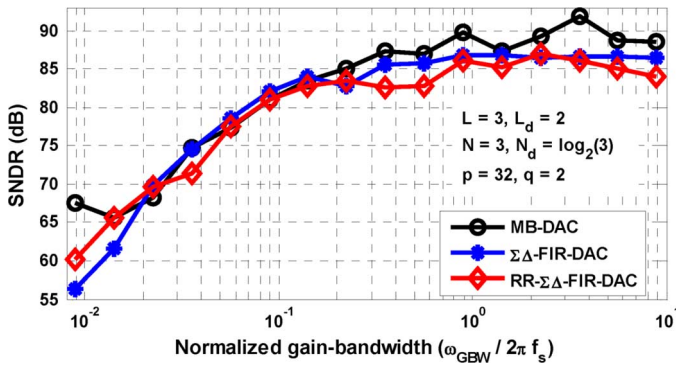

Fig. 8. SNDR versus normalized ω_{GBW} of first and second amplifiers in three modulators.

C. Extension to Feed-Forward Architectures

Both proposed DACs were introduced in the feedback architecture as shown in Fig. 2. In order to extend them for feed-forward architectures, there are two main issues that should be considered: the modulator inherent anti-aliasing filter and the delay of FIR-DAC. Due to the feed-forward branches, the order of modulator anti-aliasing filter is reduced. However, any feed-forward CT-ΣΔM (except unity *STF* architectures) has at least a first order inherent anti-aliasing filter resulting from the first integrator [2].

This anti-aliasing filter in series with the second order *LPF* of FIR-DAC prepare a third order *LPF* which is suitable for a 2nd order DΣΔM. This means that the lower order of inherent anti-aliasing filter in the feed-forward architecture does not limit the usage of both proposed DACs.

The feed-forward modulators have only one feedback path. As a result, the delay of FIR-DAC directly leads to the modulator excess loop delay. As shown in Section III-D, the delay of

both proposed DACs are $(q-1)\times T_s/q < T_s$, while the excess loop delay up to T_s can be compensated for by using a fast DAC loop around the quantizer [2]. However, at high sampling frequencies, there are other sources of excess loop delay which should be compensated. Therefore, the delay of FIR-DAC may be a limitation for maximum achievable sampling frequency in feed-forward architectures. In these cases, a combination of feedback and feed-forward paths can be used. For example, a 3.6 GS/sec modulator employing an FIR-DAC is reported in [23]. In this modulator, the FIR-DAC has a delay of $3.5\times T_s$ (8-tap FIR-DAC working at f_s).

V. Robustness Against DAC Elements Mismatch

In conventional multi-bit ΣΔMs, the output signal of an N-bit quantizer is 2^N-1 thermometer code exciting the DAC unit elements [1]. Any mismatch among the DAC unit elements adds an error which is a nonlinear function of DAC input signal $(y(\cdot))$ [1], [3]. This error causes a linearity problem in multi-bit DACs and it is directly transferred to the modulator output similar to the input signal without any shaping.

Corresponding to Fig. 2, the output signal of proposed ΣΔ-FIR-DAC at the n-th sample of modulator in the presence of elements mismatch can be expressed as

$$\begin{aligned} y_{\mathrm{DAC}}(nq-k) &= \sum_{i=0}^{2q-2} f_i y_d(nq-i-k) \\ &\quad + \sum_{i=0}^{2q-2} f_i\varepsilon_i y_d(nq-i-k) \\ &= y_d(\cdot)*f(\cdot)+y_d(\cdot)*g(\cdot), \\ &\qquad (k=0,\,1,\ldots,q-1) \end{aligned} \tag{12}$$

where * is the convolution operation, f_i is the nominal value of the i-th element in FIR-DAC (introduced in (16)), ε_i is the i-th element normalized error, $f(\cdot)$ is the time domain impulse response of $F(z)$, and $g(\cdot)$ is the time domain impulse response of $G(z)$ (an FIR filter produced by elements mismatch in FIR-DAC). The coefficients of $G(z)$ are $g_i=\varepsilon_i\times f_i$. The first term in (12) is the ideal output of ΣΔ-FIR-DAC and the second term is the error due to the elements mismatch. Unlike the multi-bit DAC error, this error is a linear function of DAC input signal, $y_d(nq-k)$, and just modifies the frequency response of $F(z)$. $G(z)$ deviate the low-pass specification of $F(z)$, and hence, it may pass the out-of-band noise of the DΣΔM. However, these unwanted spectral components are rejected by inherent LPF of CT-ΣΔM prior to the modulator sampling. As a result, the proposed ΣΔ-FIR-DAC has an excellent robustness against DAC elements mismatch.

Corresponding to Fig. 6(b), the output signal of proposed RR-ΣΔ-FIR-DAC can be expressed similar to (12), while $y_{\mathrm{DAC}}(nq-k)$ is down sampled by q times. $F(z)$ is a low-pass filter and prepares an anti-aliasing filter for the down sampling operation as discussed in Section IV. However, $G(z)$ may pass the out-of-band noise of the DΣΔM, and consequently, it is folded into the modulator bandwidth due to the down sampling performed by the decimation filter. This increases the modulator noise floor, and hence, the proposed RR-ΣΔ-FIR-DAC has less robustness against DAC elements mismatch compared to its ΣΔ-FIR-DAC counterpart. However, based on both presented analytical explanations and simulation results, the proposed RR-ΣΔ-FIR-DAC has still much better robustness against DAC elements mismatch compared to the multi-bit DAC.

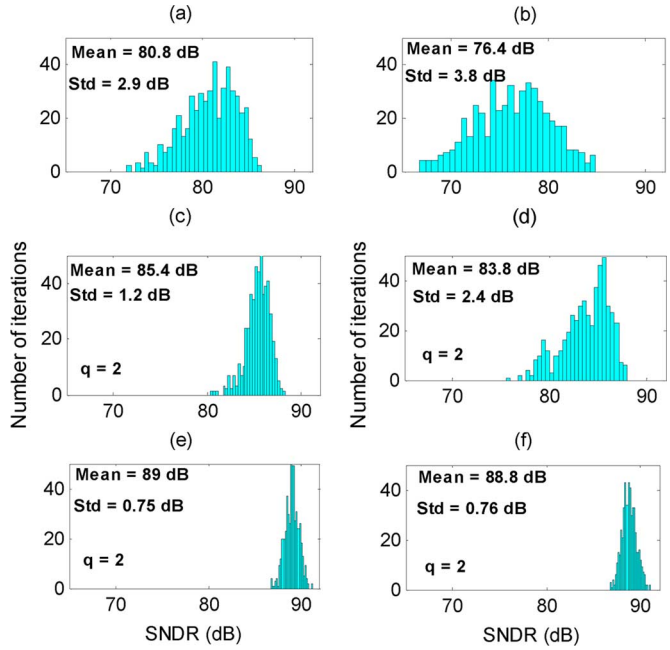

Fig. 9. Comparison of SNDR degradation due to DAC elements mismatch, between conventional multi-bit and proposed modulators with ΣΔ-FIR-DAC and RR-ΣΔ-FIR-DAC ($L=3, L_d=2, N=3, p=32$ and $\mathrm{FFT\ points}=32768$). (a) Multi-bit DAC (0.1%) (no DEM), (b) Multi-bit DAC (0.2%) (no DEM), (c) RR-ΣΔ-FIR-DAC (0.1%), (d) RR-ΣΔ-FIR-DAC (0.2%), (e) ΣΔ-FIR-DAC (0.1%), (f) ΣΔ-FIR-DAC (0.2%).

Several simulations are performed to evaluate the effect of DAC elements mismatch on the modulator performance. The parameters used in these simulations are similar to those mentioned in Section III-E. The clock jitter noise was assumed to be zero. Fig. 9 shows the SNDR histogram of the CT ΣΔM with a multi-bit DAC (no DEM technique was employed) compared to the modulators employing both proposed DACs.

For each case, 500 different simulations were performed. 0.1% and 0.2% intentional mismatch were considered between the DAC elements, while the same amount of mismatch is considered in the FIR-DAC coefficients of both ΣΔ-FIR-DAC and RR-ΣΔ-FIR-DAC. Note that the mentioned amounts of mismatch were considered for each coefficient in FIR-DAC as a percent of its value. The maximum SNDR of ideal modulator is 89 dB. According to Fig. 9, without any DEM technique, the DAC elements mismatch causes significant performance degradation in conventional multi-bit modulator whereas the modulator with RR-ΣΔ-FIR-DAC has less performance degradation and the modulator with ΣΔ-FIR-DAC has negligible performance degradation. The corresponding average and standard deviation of each histogram are also mentioned in the figures.

VI. Clock Jitter Immunity

In conventional CT ΣΔMs, the current of feedback DAC is converted into the voltage by injecting the charge to the inte-

grator feedback capacitor. Any deviation of DAC pulse duration from its nominal value leads to a voltage error added to the input of modulator. This error is directly transferred to the modulator's output, and hence, degrades the modulator's resolution. For a non-return-to-zero (NRZ) DAC, the error sequence can be represented by [24]

$$e(n) = \frac{\beta(n)}{T_s} \cdot [y(n) - y(n-1)] \tag{13}$$

where $y(n)$ is the output of the conventional modulator, $\beta(n)$ is the time deviation of DAC pulse edge at n-th sample time, and T_s is the nominal sampling period of the modulator. $\beta(\cdot)$ is assumed to be a Gaussian white stationary random process independent on $y(\cdot)$ and with a power spectral density of σ_β^2. The model of (13) implies that by decreasing the difference of two adjacent output samples in NRZ DAC, its jitter error can be reduced. On the other hand, the high frequency components of FIR-DAC input signal is filtered by its sinc filter and the difference of its two adjacent output samples is decreased. Therefore, by increasing both the order and number of taps in the sinc filter, the clock jitter immunity of FIR-DAC is improved. However, as mentioned in Section III-A, the number of taps in sinc filter is determined by the modulator bandwidth. Also, as explained in Section IV, the order of sinc filter is determined by the order of *LPF* required to suppress the out-band noise of DΣΔM, while its maximum order is limited by practical considerations. Hence, in this Section, the FIR-DAC with the filtering characteristic of (3) (q-tap sinc^2 filter) is used in the analysis.

A. The Effects of Clock Jitter in Modulator's Outer Loop

Considering (13), in a conventional multi-bit modulator, the variance of output error due to the clock jitter is given by

$$\sigma_{MB}^2 = E\{e^2(n)\} = \frac{\sigma_\beta^2}{T_s^2}\,\sigma_{\Delta y}^2 = \frac{\sigma_\beta^2}{T_s^2} \times \left(\frac{\gamma \times V_{FS}}{2^N}\right)^2 \tag{14}$$

where $E\{\cdot\}$ is the mathematical expectation operator and $\sigma_{\Delta y}$ is the standard deviation of $[y(n) - y(n-1)]$. Without loss of generality, the mathematical expectation of $[y(n) - y(n-1)]$ is assumed to be a coefficient of the quantizer's least-significant-bit (LSB), $\gamma \times V_{FS}/(2^N)$. Considering only the jitter noise, the signal-to-noise ratio (SNR) of the multi-bit modulator for a sinusoidal input signal with amplitude A is given by:

$$\mathrm{SNR}_{MB,\sigma_\beta} = \frac{A^2/2}{\sigma_{MB}^2} \times \mathrm{OSR} = \frac{A^2 2^{2N} T_s^2}{2\sigma_\beta^2 \gamma^2 V_{FS}^2} \times OSR. \tag{15}$$

The effect of clock jitter on proposed ΣΔM with ΣΔ-FIR-DAC can be evaluated as well. According to (3), $F(\mathrm{z})$ is a sinc^2 filter, and hence, its coefficients are given by

$$f_i = \frac{1}{q^2} \times \begin{cases} (i+1) & 0 \le i \le q-1 \\ (2q-1-i) & q \le i \le 2q-2 \end{cases}. \tag{16}$$

The binary signal $Y_d(z)$, which is the input of $F(\mathrm{z})$, is clocked at the rate of $q \times f_s$. The ΣΔ-FIR-DAC works q times faster than the main modulator. Hence, during the modulator's sampling period (T_s), the error due to the clock jitter is produced for q times. During T_s, the overall error in i-th path of FIR filter (Fig. 2) is the summation of these q errors, and therefore, it is given by

$$e_i(n) = \sum_{k=0}^{q-1} f_i \frac{\beta(nq-k)}{T_S} [v_i(nq-k) - v_i(nq-k-1)] \tag{17}$$

where $\beta(nq-k)$ is the time deviation in DAC pulse edge at the $(nq-k)$-th samples of FIR-DAC. The overall error of output voltage is the summation of errors in its $2q-1$ paths. So, we have

$$\begin{aligned} e(n) &= \sum_{i=0}^{2q-2} e_i(n) \\ &= \frac{1}{q^2} \sum_{k=0}^{q-1} \frac{\beta\,(nq-k)}{T_s} \left(\sum_{i=0}^{q-1} (i+1)[v_i(nq-k) \right. \\ &\quad - v_i(nq-k-1)] \\ &\quad \left. + \sum_{i=q}^{2q-2} (2q-1-i)[v_i(nq-k) - v_i(nq-k-1)] \right). \end{aligned} \tag{18}$$

Corresponding to Fig. 2, $v_0(r) = y_d(r)$ and $v_i(r) = v_{i-1}(r-1)$, for $i = 1, 2 \ldots, 2q-2$. Thus, after simplification we have

$$\begin{aligned} e(n) &= \frac{1}{q^2} \sum_{k=0}^{q-1} \frac{\beta(nq-k)}{T_s} \\ &\quad \times \left(\sum_{i=0}^{q-1} y_d(nq-k-i) - \sum_{i=0}^{q-1} y_d(nq-q-k-i) \right). \end{aligned} \tag{19}$$

Therefore, the variance of $e(n)$ is obtained as

$$\sigma_{\Sigma\Delta}^2 = E\{e^2(n)\} = \frac{\sigma_\beta^2}{q^4 T_s^2} \sum_{k=0}^{q-1} E\left\{\Delta y_{dk}^2\right\} = \frac{\sigma_\beta^2}{q^3 T_s^2} \sigma_{\Delta y_d}^2 \tag{20}$$

where $\Delta y_{d\,k} = \sum_{i=0}^{q-1} (y_d(nq-k-i)) - \sum_{i=0}^{q-1} (y_d(nq-k-q-i))$, and $\sigma_{\Delta y_d}^2 = E\{\Delta y_{dk}^2\}$. Assuming $S(\mathrm{z}) = 2z^{-1} - z^{-2}$ in (2), the quantization noise of the DΣΔM is shaped by $(1-z^{-1})^2$. As shown in Appendix A, $\sigma_{\Delta yd}^2$ can be expressed as

$$\sigma_{\Delta y_{\,d}}^2 = q^2 \sigma_{\Delta y}^2 + 4\sigma_Q^2 \tag{21}$$

where σ_Q^2 is the variance (or power) of DΣΔM quantization noise which is equal to $(V_{FS}/2)^2/6$ for evaluating a one-sided spectrum. As noted in (14), $\sigma_{\Delta y}^2 = \gamma^2 \times {V_{FS}}^2/2^{2N}$ and by substituting (21) in (20), we have

$$\begin{aligned} \sigma_{\Sigma\Delta}^2 &= \frac{\sigma_\beta^2}{q^3 T_s^2} \left(q^2 \sigma_{\Delta y}^2 + 4\sigma_Q^2\right) \\ &= \frac{\sigma_\beta^2}{q^3 T_s^2} V_{FS}^2 \left(\left(\frac{\gamma \times q}{2^N} \right)^2 + \frac{1}{6} \right). \end{aligned} \tag{22}$$

The SNR of proposed modulator with ΣΔ-FIR-DAC for a sinusoidal input signal with amplitude A, where only the jitter noise is considered, is equal to

$$\begin{aligned}\mathrm{SNR}_{\Sigma\Delta,\sigma_\beta} &= \frac{A^2/2}{\sigma^2_{\Sigma\Delta}} \times \mathrm{OSR} \\ &= \frac{A^2 q^3\, 2^{2N}\, T_s^2}{2\,\sigma_\beta^2\, V_{FS}^2 \left(\gamma^2 q^2 + \frac{2^{2N}}{6}\right)} \cdot \mathrm{OSR} \\ &= \frac{q^3}{\left(\gamma^2 q^2 + \frac{2^{2N}}{6}\right)} \times \mathrm{SNR}_{MB,\sigma_\beta}. \end{aligned} \tag{23}$$

According to (23), the clock jitter immunity of ΣΔ-FIR-DAC is better than the multi-bit DAC when $q^2 \times (q-1) > 2^N/\sqrt{6}$.

The clock jitter immunity of RR-ΣΔ-FIR-DAC is also estimated. The FIR-DAC of RR-ΣΔ-FIR-DAC shown in Fig. 6(b) includes some down sampling blocks in addition to FIR-DAC of ΣΔ-FIR-DAC shown in Fig. 2. The number of ΣΔ-FIR-DAC pulses during T_s is reduced from $q-1$ to 1 and so the upper boundary summation in (17), (18), and (19) should be modified resulting in

$$\sigma^2_{\Sigma\Delta-RR} = \frac{\sigma_\beta^2}{q^4 T_s^2} E\left\{\Delta y_{dk}^2\right\} = \frac{\sigma_\beta^2}{q^4 T_s^2}\sigma^2_{\Delta y_d}. \tag{24}$$

Therefore, the variance of jitter error and the SNR of modulator with RR-ΣΔ-FIR-DAC (for a sinusoidal input signal with amplitude A and where only the jitter noise is considered) can be expressed as (25) and (26), respectively, as follows:

$$\sigma^2_{\Sigma\Delta-RR} = \frac{\sigma_\beta^2}{q^4 T_s^2} V_{FS}^2 \left(\left(\frac{\gamma \times q}{2^N}\right)^2 + \frac{1}{6}\right) \tag{25}$$

$$\begin{aligned}\mathrm{SNR}_{\Sigma\Delta-RR,\sigma_\beta} &= \frac{(A^2/2) \times \mathrm{OSR}}{\sigma^2_{\Sigma\Delta-RR}} \\ &= \frac{A^2 q^4\, 2^{2N}\, T_s^2 \times \mathrm{OSR}}{2\,\sigma_\beta^2 V_{FS}^2 \left(\gamma^2 q^2 + \frac{2^{2N}}{6}\right)} \\ &= \frac{q^4}{\left(\gamma^2 q^2 + \frac{2^{2N}}{6}\right)} \mathrm{SNR}_{MB,\sigma_\beta} \end{aligned} \tag{26}$$

Several simulations are performed to validate the aforementioned analytical results. The ΣΔM of Fig. 2 was simulated using the parameters introduced in Section III-E. Fig. 10 shows the SNR degradation versus the clock jitter for two cases: $N=3, q=2$ and $N=4, q=3$. Dashed line curves are corresponding to the system level simulations of three modulators where the jitter noise is modeled according to (13). The solid lines are analytical results calculated from (15), (23), and (26) for the multi-bit modulator, proposed modulator with ΣΔ-FIR-DAC, and proposed modulator with RR-ΣΔ-FIR-DAC, respectively, where for a course analytical estimation γ was assumed to be 1.

As illustrated in Fig. 10, there is a good accuracy between analytical and simulation results when the clock jitter is the dominant noise source. The clock jitter immunity of proposed DACs and the multi-bit DAC is approximately the same, while each of proposed DACs contains only half of the unit elements utilized in the multi-bit DAC.

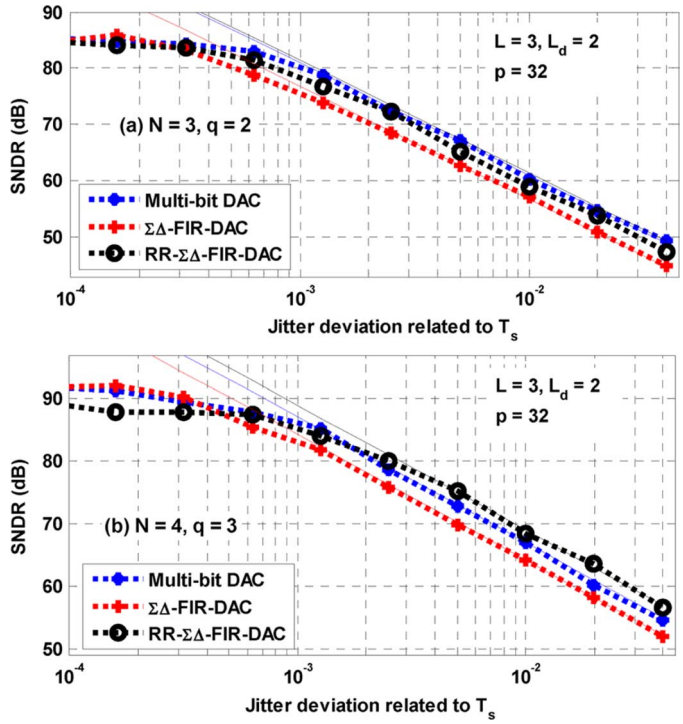

Fig. 10. SNR versus the standard deviation of jitter noise in three different modulators with multi-bit DAC, ΣΔ-FIR-DAC and RR-ΣΔ-FIR-DAC, for (a) $N=3, q=2$, and (b) $N=4, q=3 (\gamma=1)$.

B. The Effects of Clock Jitter in Modulator's Second Loop

In Fig. 2, due to two reasons, the clock jitter noise of inner loops can be negligible compared to the jitter noise of the first loop. Firstly, the inner loops of proposed modulator are driven by multi-bit signal of quantizer, $y(\cdot)$. Secondly, the jitter noise of inner loops is shaped by their prior integrators. However corresponding to Fig. 2, the second loop's DAC can be driven either by $y(\cdot)$ or $y_d(\cdot)$. When the second DAC is driven by the 1.5-bit signal of DΣΔM, $y_d(\cdot)$, its jitter noise becomes significant. Therefore, in this subsection, this case is studied.

Any error in the second loop is shaped by the transfer function of

$$\begin{aligned} D(s) &= \frac{-k_2 f_s^2 s}{(s^3 + k_3 f_s s^2 + k_2 f_s^2 s + k_1 f_s^3)} \\ |D(f)|^2 &\approx \left(\frac{k_2}{k_1}\right)^2 \left(\frac{f}{f_s}\right)^2, \quad \text{if } f \ll f_s. \end{aligned} \tag{27}$$

By using the model of (13), the one-sided PSD of jitter noise at the second loop DAC output is $2 \times (\sigma_\beta^2 \times \sigma^2_{\Delta yd}/T_s^2)/f_s$, where $\sigma^2_{\Delta yd}$ was introduced in (21). The PSD is shaped by $|D(f)|^2$. By integrating the PSD over the signal bandwidth, the in-band noise power due to the clock jitter in the second DAC is given by

$$\sigma^2_{\Sigma\Delta,\,IL} = \frac{\sigma_\beta^2}{T_s^2} V_{FS}^2 \left(\left(\frac{\gamma \times q}{2^N}\right)^2 + \frac{1}{6}\right) \times \frac{k_2^2 \pi^2}{3 k_1^2\, \mathrm{OSR}^3}. \tag{28}$$

Comparing relation (28) with relations (22) and (25), the clock jitter noise of the second loop is less than that of the first loop for both proposed DACs provided that $\mathrm{OSR} = p > \{q^4 \pi^2 k_2^2/(3k_1^2)\}^{1/3}$. For the value of parameters

used in the simulations of this paper, this means that the OSR should be more than 7.2.

VII. Comparision With the Conventional Multi-Bit ΣΔMs

The proposed modulators with ΣΔ-FIR-DAC and RR-ΣΔ -FIR-DAC are mainly different from the conventional one in both DAC architectures and digital circuits. The conventional multi-bit DAC needs 2^N-1 unit elements, while both proposed DACs require only $2q-1$ unequal elements. The value of these elements is introduced in (16) and their summation is equivalent to q^2 unit elements in which $q^2 \approx 2^N/2$.

The proposed modulators are more robust against DAC elements mismatch compared to the multi-bit modulator which uses no DEM technique. Also, the modulators with both proposed DACs have approximately the same clock jitter immunity as the multi-bit modulator.

The modulator output signal with both proposed DACs is a 1.5-bit signal at the rate of $q \times f_s$, while the output signal of the conventional multi-bit ΣΔM is an N-bit signal at the rate of $f_s = 1/T_s$. As noted in Section III, the OSR of digital circuit, q, has a very low value (e.g., 2, 3, and 4 for $N = 3, 4$, and 5, respectively). Also, out of the modulator bandwidth, $[f_s/2,\ q \times f_s/2]$, the noise shaping order is $L_d = 2$, while in modulator bandwidth the noise shaping order is L. Therefore, due to these reasons, i.e., 1.5-bit output signal, low noise shaping order at the out-of-band frequencies, and low value of q, the required decimation filter in proposed modulators are not so complicated compared to that in the conventional N-bit modulator. Besides, the delayed version of $Y_d(z)$ produced by the delay line in the FIR-DAC can also be used in the decimation filter.

Although the ΣΔ-FIR-DAC operates at a higher rate, but according to the simulation results, the modulator amplifiers require approximately the same analog specifications as the conventional multi-bit modulator. In RR-ΣΔ-FIR-DAC, the rate of FIR-DAC is equal to the rate of the multi-bit DAC.

The digital circuit of the proposed modulator consists of two adders, two registers ($S(z) = 2z^{-1} - z^{-2}$) (DΣΔM of Fig. 2) and $2q-2$ latches for the delay line of FIR-DAC [Fig. 2 or Fig. 6(b)]. According to relation (9), the required word length in adders and registers are $N+7$ or $N+3$ depending on $y(\cdot)$ or $y_d(\cdot)$ is applied into the second loop's DAC, respectively.

On the other hand, in conventional multi-bit modulators, a DEM technique must be used to overcome the DAC nonlinearity. Usually by increasing the quantizer resolution, N, the complexity of DEM techniques is increased exponentially, 2^N, while the value of q (and consequently the complexity of proposed DACs) grows approximately linearly with N. Besides, both proposed techniques can be used at low OSRs as well as high OSRs, while the performance of DEM techniques is degraded when the OSR is reduced. As another drawback, the DEM techniques such as the data weighted averaging (DWA) are unsuitable for CT-ΣΔMs with multi-bit NRZ DACs [25]. Only for the sake of comparison, the hardware of DWA as one of the simplest DEM techniques is considered here. The DWA technique requires an N-bit adder, an N-bit register, a randomizer and a logic block to implement the 2^N-1 bit barrel shifter [3].

VIII. Conclusion

A new class of CT ΣΔMs was proposed by using the ΣΔ-DAC to eliminate the mismatch error of multi-bit DAC and an FIR-DAC to improve the DAC clock jitter insensitivity. Furthermore, a reduced rate ΣΔ-FIR-DAC was proposed which can be used in both DT and CT ΣΔMs. The main parts of proposed DACs are implemented in the digital domain, and hence, can be benefited from the scaling advantages of nano-meter CMOS technologies, while the analog requirements of proposed modulators are the same as the conventional multi-bit ones. Analytical calculations and system level simulation results show that the clock jitter immunity in CT ΣΔMs with both proposed DACs and the conventional multi-bit one is approximately the same, while simultaneously their robustness against DAC elements mismatch is significantly improved.

Appendix A

According to (2), $y_d(\cdot)$ has two independent terms. For proposed ΣΔ-FIR-DAC, the value of $\sigma_{\Delta y_d}$ can be obtained as

$$\begin{aligned}\sigma^2_{\Delta y_d} &= E\left\{\left(\sum_{i=0}^{q-1} y_d(m-i) - \sum_{i=0}^{q-1} y_d(m-q-i)\right)^2\right\}\\ &= E\left\{\left(\sum_{i=0}^{q-1} y_{\rm up}(m-i) - \sum_{i=0}^{q-1} y_{\rm up}(m-q-i)\right)^2\right\}\\ &\quad + E\left\{\left(r(m) * \left(\sum_{i=0}^{q-1} e_Q(m-i)\right.\right.\right.\\ &\quad \left.\left.\left. - \sum_{i=0}^{q-1} e_Q(m-q-i)\right)\right)^2\right\} \qquad \text{(A1)}\end{aligned}$$

where $m = nq - k$ and the z-transform of $r(m)$ is $R(z) = 1 - S(z) = (1-z^{-1})^2 = 1 - 2z^{-1} - z^{-2}$. By considering (1), the first term of (A1) is equal to

$$\begin{aligned}&E\left\{\left(\sum_{i=0}^{q-1} y_{\rm up}(m-i) - \sum_{i=0}^{q-1} y_{\rm up}(m-q-i)\right)^2\right\}\\ &\qquad = E\{(q\Delta_y)^2\} = E\left\{q^2 \times \Delta_y^2\right\} = q^2 \times \sigma^2_{\Delta y} \qquad \text{(A2)}\end{aligned}$$

where $\sigma_{\Delta y}$ is introduced in (14).

The second term of (A1) can be expressed as $E\{S^2_{eq}(m)\}$

$$\begin{aligned}S_{eq}(m) &= \left(\sum_{i=0}^{q-1} e_Q(m-i) - 2 \times \sum_{i=0}^{q-1} e_Q(m-i-1)\right.\\ &\quad \left. + \sum_{i=0}^{q-1} e_Q(m-i-2)\right) - \left(\sum_{i=0}^{q-1} e_Q(m-i-q)\right.\\ &\quad - 2 \times \sum_{i=0}^{q-1} e_Q(m-i-1-q)\\ &\quad \left. + \sum_{i=0}^{q-1} e_Q(m-i-2-q)\right). \qquad \text{(A3)}\end{aligned}$$

In (A3), by defining $(m-i-1)=(m-j)$ and $(m-i-2)=(m-l)$, we have

$$\begin{aligned}S_{eq}=&\left(\sum_{i=2}^{q-1}e_Q(m-i)-2\times\sum_{j=2}^{q-1}e_Q(m-j)\right.\\&\left.+\sum_{l=2}^{q-1}e_Q(m-l)\right)-\left(\sum_{i=2}^{q-1}e_Q(m-i-q)\right.\\&\left.-2\times\sum_{j=2}^{q-1}e_Q(m-j-q)+\sum_{l=2}^{q-1}e_Q(m-l-q)\right)\\&+(e_Q(m)+e_Q(m-1)-2e_Q(m-1))\\&-(e_Q(m-q)+e_Q(m-q-1)-2e_Q(m-q-2)).\end{aligned}\tag{A4}$$

Simplifying the relation (A4) results in

$$\begin{aligned}S_{eq}=&(e_Q(m)-e_Q(m-1))\\&-(e_Q(m-q)-e_Q(m-q-1))\end{aligned}\tag{A5}$$

By assuming the digital quantizer noise as white, four terms of (A5) are independent from each other and the variance of S_{eq} is given by

$$E\left\{S_{eq}^2\right\}=4\sigma_Q^2\tag{A6}$$

where σ_Q^2 is the noise variance of the digital quantizer. By substituting (A2) and (A6) in (A1), the relation (21) is proved as:

$$\sigma_{\Delta y_d}^2=q^2\sigma_{\Delta y}^2+4\sigma_Q^2\tag{A7}$$

ACKNOWLEDGMENT

The authors would like to thank the Associate Editor and the anonymous reviewers for their constructive and valuable comments to improve the quality of this paper.

REFERENCES

[1] R. Schreier and G. C. Temes, *Understanding Delta-Sigma Data Converters*. New York: Wiley/IEEE Press, 2005.

[2] M. Ortmanns and F. Gerfers, *Continuous-Time Sigma-Delta A/D Conversion*. New York: Springer, 2005.

[3] R. T. Baird and T. S. Fiez, "Linearity enhancement of multibit ΣΔ A/D and D/A converters using data weighted averaging," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 42, no. 12, pp. 753–762, Dec. 1995.

[4] A. J. Chen and Y. P. Xu, "Multibit delta-sigma modulator with noise-shaping dynamic element matching," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 56, no. 6, pp. 1125–1133, Jun. 2009.

[5] N. Sun and P. Cao, "Low-complexity high-order vector-based mismatch shaping in multibit ΔΣ ADCs," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 58, no. 12, pp. 872–876, Dec. 2011.

[6] J. G. Kauffman, P. Witte, and M. Ortmanns, "An 8.5 mW continuous-time ΣΔ modulator with 25 MHz bandwidth using digital background DAC linearization to achieve 63.5 dB SNDR and 81 dB SFDR," *IEEE J. Solid-State Circuits*, vol. 46, no. 12, pp. 2869–2881, Dec. 2011.

[7] S.-C. Lee and Y. Chiu, "Digital calibration of capacitor mismatch in sigma-delta modulators," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 58, no. 4, pp. 690–698, Apr. 2011.

[8] C.-Y. Lu, M. Onabajo, V. Gadde, Y.-C. Lo, H.-P. Chen, V. Periasamy, and J. Silva-Martinez, "A 25 MHz bandwidth 5th-order continuous-time low-pass sigma-delta modulator with 67.7 dB SNDR using time-domain quantization and feedback," *IEEE J. Solid-State Circuits*, vol. 45, no. 9, pp. 1795–1808, Sep. 2010.

[9] F. Colodro and A. Torralba, "Digital noise-shaping of residues in dual-quantization sigma-delta modulators," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 51, no. 2, pp. 225–232, Feb. 2004.

[10] Q.-Q. Wang, B.-J. Ge, X.-X. Feng, and X.-A. Wang, "Digital noise shaping multibit delta-sigma modulator," *Electron. Lett.*, vol. 46, no. 16, pp. 1110–1111, Aug. 2010.

[11] H. Pakniat and M. Yavari, "Dual quantization continuous time ΣΔ modulators with spectrally shaped feedback," in *Proc. IEEE ICECS*, Dec. 2011, pp. 414–417.

[12] J.-Y. Wu, Z. Zhang, R. Subramoniam, and F. Maloberti, "A 107.4 dB SNR multi-bit sigma delta ADC with 1-PPM THD at 0.12 dB from full scale input," *IEEE J. Solid-State Circuits*, vol. 44, no. 11, pp. 3060–3066, Nov. 2009.

[13] F. Colodro and A. Torralba, "New continuous-time multibit sigma-delta modulators with low sensitivity to clock jitter," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 56, no. 1, pp. 74–83, Jan. 2009.

[14] V. Dhanasekaran, M. Gambhir, M. M. Elsayed, E. Sanchez-Sinencio, J. Silva-Martinez, C. Mishra, L. Chen, and E. J. Pankratz, "A continuous time multi-bit ΣΔ ADC using time domain quantizer and feedback elements," *IEEE J. Solid-State Circuits*, vol. 46, no. 3, pp. 639–650, Mar. 2011.

[15] M. M. Elsayed, V. Dhanasekaran, M. Gambhir, J. Silva-Martinez, and E. Sanchez-Sinencio, "A 0.8 ps DNL time-to-digital converter with 250 MHz event rate in 65 nm CMOS for time-mode-based ΣΔ modulator," *IEEE J. Solid-State Circuits*, vol. 46, no. 9, pp. 2084–2098, Sep. 2011.

[16] K. Nguyen, A. Bandyopadhyay, B. Adams, K. Sweetland, and P. Baginski, "A 108 dB SNR 1.1 mW oversampling audio DAC with a three-level DEM technique," *IEEE J. Solid-State Circuits*, vol. 43, no. 12, pp. 2592–2600, Dec. 2008.

[17] D. K. Su and B. A. Wooley, "A CMOS oversampling D/A converter with a current-mode semi-digital reconstruction filter," *IEEE J. Solid-State Circuits*, vol. 28, no. 12, pp. 1224–1233, Dec. 1993.

[18] M. Kashmiri, K. Makinwa, and L. Breems, "A multi-bit cascaded sigma-delta modulator with an oversampled single-bit DAC," in *Proc. IEEE ICECS*, Dec. 2009, pp. 49–52.

[19] F. Colodro and A. Torralba, "Impact of finite impulse response digital-to analogue converter delay on the stability of continuous-time sigma-delta modulators with pulse-with modulation in the feedback path," *IET Circuits Devices Syst.*, vol. 4, no. 3, pp. 218–226, May 2010.

[20] J. C. Candy, "Decimation for sigma-delta modulation," *IEEE Trans. Commun.*, vol. 34, no. 1, pp. 72–76, Jan. 1986.

[21] S. Yan and E. Sánchez-Sinencio, "A continuous-time ΣΔ modulator with 88-dB dynamic range and 1.1-MHz signal bandwidth," *IEEE J. Solid-State Circuits*, vol. 39, no. 1, pp. 75–86, Jan. 2004.

[22] F. Colodro and A. Torralba, "Multirate single-bit ΣΔ modulators," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 49, no. 9, pp. 629–634, Sep. 2002.

[23] P. Shettigar and S. Pavan, "A 15 mW 3.6 GS/s CT-ΣΔ ADC with 36 MHz bandwidth and 83 dB DR in 90 nm CMOS," in *Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2012, pp. 156–158.

[24] J. A. Cherry and W. M. Snelgrove, "Clock jitter and quantizer metastability in continuous-time delta-sigma modulators," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 46, no. 6, pp. 661–676, Jun, 1999.

[25] L. Risbo, R. Hezar, B. Kelleci, H. Kiper, and M. Fares, "Digital approaches to ISI-Mitigation in high-resolution oversampled multi-level D/A converters," *IEEE J. Solid-State Circuits*, vol. 46, no. 12, pp. 2892–2903, Dec. 2011.

Hossein Pakniat was born in Iran. He received the B.Sc. and M.Sc. degrees in electrical engineering from the University of Shiraz, Shiraz, Iran, and Amirkabir University of Technology, Tehran, in 2007 and 2009, respectively. He is currently working toward the Ph.D. degree at the Amirkabir University of Technology.

His research interests include integrated circuit design and sigma-delta ADCs.

Mohammad Yavari (S'01–M'08) received the B.Sc., M.Sc., and Ph.D. degrees in electrical engineering from the University of Tehran, Tehran, Iran, in 1999, 2001, and 2006, respectively.

He has been an Assistant Professor at the Department of Electrical Engineering, Amirkabir University of Technology (AUT), Tehran, Iran, since September 2006, where he founded the Integrated Circuits Design Laboratory in 2007. He spent several research periods at the Institute of Microelectronics of Seville (IMSE-CNM), Seville, Spain. He was with Niktek from May 2004 to April 2005 and Oct. 2006 to May 2007 as a Principal Design Engineer where he was involved in the design of high-resolution A/D and D/A converters for professional digital audio applications. His research interests include analog and mixed-signal integrated circuits and signal processing, data converters, and CMOS RFIC design for wireless communications. He is the author or co-author of more than 100 peer-reviewed papers in international and national journals and conference proceedings on analog integrated circuits.

Dr. Yavari was a recipient of the Best Student Research Award of the University of Tehran in 2004.