Microelectronics Journal 46 (2015) 1073–1081

Contents lists available at ScienceDirect

Microelectronics Journal

journal homepage: www.elsevier.com/locate/mejo

System level design and optimization of single-loop CT sigma-delta modulators for high resolution wideband applications

Hossein Pakniat, Mohammad Yavari *

Integrated Circuits Design Laboratory, Department of Electrical Engineering, Amirkabir University of Technology (Tehran Polytechnic), Tehran, Iran

ARTICLE INFO

Article history:
Received 5 January 2015
Received in revised form
14 July 2015
Accepted 25 August 2015
Available online 14 September 2015

Keywords:
ΣΔ modulators
Resolution of CT ΣΔ modulators
Power estimation in CT ΣΔ modulators
Continuous-time integrated circuits

ABSTRACT

In this paper, the main resolution limitations in single-stage continuous-time sigma-delta modulators (CT ΣΔMs) are analytically estimated as the function of system level parameters for wideband applications. The analytical results are supported by simulation results. The power consumption of CT ΣΔMs is also analytically estimated as the function of system level parameters, and then, it is validated by the reported power consumption of several state-of-the-art fabricated prototypes. Based on analytical results, for a targeted resolution and bandwidth, an algorithm is proposed to design the system level parameters of CT ΣΔMs for the minimum power consumption. The estimation of power consumption and the designed parameters match well with the design of best state-of-the-art fabricated modulators.

1. Introduction

Continuous-time sigma-delta modulators (CT ΣΔMs) are widely used in power efficient high-resolution and wideband applications [1–9]. On the other hand, CT ΣΔMs like other ADCs are sensitive to the analog circuit non-idealities limiting their maximum resolution especially in MHz bandwidths. The analog circuit non-idealities and the circuit and quantization noise constitute the modulator's noise floor. The reduction of each error or noise has its own power penalty depending on the oversampling ratio (OSR), quantizer bit-length (N_c), and modulator's noise-shaping order (L_c). Consequently, OSR, N_c, L_c and the share of each error in the modulator's noise floor are the most important design parameters to minimize the power consumption for a targeted bandwidth (BW) and resolution (B-bit).

The system level computer aided design (CAD) tools [9–11] and analytic design procedures [12–15] are introduced for CT ΣΔMs which are usually based on the minimization of both quantization noise and power consumption. Also, the extensive system level research on discrete-time (DT) ΣΔMs [16] can be employed for CT ΣΔMs [12], while various DT-to-CT transformations are adapted for this purpose [12]. However, the direct design of CT ΣΔMs is more robust against the circuit non-idealities [9].

Two important aims of the available system level design approaches are the optimum loop filter coefficients and the amplifiers' specifications [9–11]. The loop filter coefficients are usually optimized for the minimum quantization noise, while stability requirements are satisfied. The amplifiers' specifications are optimized for the minimum power consumption [9–11]. But, these useful synthesis tools usually require the main system level parameters (i.e. L_c, N_c and *OSR*) as the input variables [9–15]. These parameters are mainly designed to suppress the quantization noise well below the total noise floor [2,9–15]. There are various combinations of these three parameters which can suppress the quantization noise adequately. The comparison of synthesized results and/or the designer experiences, based on the power estimation, stability requirement, and circuit level non-idealities, lead to select one of the possible combinations [1–9]. However, besides the quantization noise, the CT ΣΔMs have other resolution limitations widely investigated in literature [9,12,17,18,19]. The share of these errors (especially the thermal and jitter noises) in the modulator's noise floor are the other important system level parameters. For example, it is well known that the thermal noise reduction needs the most power budget, and so, it can contain the most part of the noise floor [12,16].

In this paper, the main error sources in single-stage CT ΣΔMs, implemented by active RC integrators, are analyzed and validated by the simulation results where it is necessary. Considering the required power budget to reduce each error source share in the modulator's noise floor, the power consumption of each part of the modulator is analytically estimated and then it is validated by the reported power consumption of the best state-of-the-art fabricated prototypes. The main aim of this paper is the system level design of CT ΣΔMs (L_c, N_c, OSR, and the share of thermal noise floor (α_{th})). For this purpose, for a given resolution and bandwidth, the modulator power consumption is estimated as the function of

* Corresponding author.
E-mail address: myavari@aut.ac.ir (M. Yavari).

http://dx.doi.org/10.1016/j.mejo.2015.08.010
0026-2692/

the system level parameters, and then, a power optimization algorithm for CT ΣΔMs is presented. The proposed algorithm selects the best values of L_c, N_c, OSR, and α_{th}.

The paper is organized as follows. In Section 2, the main errors in single-stage CT ΣΔMs are analytically obtained. Section 3 estimates the power consumption of CT ΣΔMs analytically. The power optimization algorithm is proposed in Section 4. Finally, Section 5 concludes the paper.

2. Resolution limitations in single-stage CT ΣΔMs

The resolution of CT ΣΔMs are mainly affected by the thermal noise, clock jitter noise, limited gain-bandwidth (GBW) and slew rate of amplifiers, quantization noise, resistance–capacitance (RC) product changes due to the process variations, excess loop delay, mismatch among the digital-to-analog converter (DAC) unit elements, and the time mismatch in the rising and falling edges of DAC pulses [12].

Some of these errors are mitigated by system level and/or circuit level techniques such that their effects on the modulator's noise floor can be neglected. The inevitable process variations of resistance–capacitance product are usually overcome by a digitally adjustable capacitor bank up to 40% [2,3,5,7,8]. The limited GBW and slew rate of amplifiers lead to an excess loop delay and data dependent error which can be reduced by suitable circuit and system level design techniques. The excess loop delay is compensated by a fast path around the quantizer [1–8]. The mismatch among the DAC unit elements is mitigated by dynamic element matching [1,16], analog calibration [12], or digital techniques [5,19]. The time mismatch in the rising and falling edges of DAC output is reduced by using the fully-differential architecture [12]. It can be further reduced by a digital calibration [2] or it can be eliminated by utilizing a return to zero (RZ) DAC [12].

The summation of the aforementioned errors, which can be mitigated by system or circuit level techniques, usually constitute a low part of the modulator's noise floor (say 10–20%), while the thermal and clock jitter noise reductions have a significant power penalty, and so, they usually form 70–80% of the noise floor [12]. The quantization noise contains 5–10% of the modulator's noise floor [12–16].

2.1. Thermal noise

The overall in-band thermal noise of a fully-differential CT ΣΔM is given by [12]:

$$IBN_{th} = 1.1 \times 4kTR_t(2BW) \tag{1}$$

where $k = 1.38 \times 10^{-23}$ J/°K is Boltzmann's constant, T is the environment temperature in Kelvin, BW is the signal bandwidth, $R_t = R + R_{DAC} + R_{eq}$ is the equivalent thermal noise resistance referred to the input port. R is the input resistor. R_{DAC} denotes the feedback or its equivalent thermal resistance and R_{eq} is the equivalent input resistance of the amplifier thermal noise. The coefficient 1.1 models the thermal noise of the subsequent integrators as 10% of the first integrator.

For a given B-bit resolution, the modulator's noise floor is given by:

$$NF = \frac{(\lambda V_{FS}/2)^2}{3 \times 2^{2B}} \tag{2}$$

where V_{FS} is the full-scale voltage of the modulator and $\lambda \times V_{FS}$ is the maximum input signal level.By assuming $R_{DAC} = R$, $R_{eq} = 0.1 \times R$ and the total thermal noise is α_{th} (< 1) times of the noise floor, the first integrator resistance in the input signal path is given by:

$$R = \frac{\alpha_{th} NF}{1.1 \times 2.1 \times 4kT(2BW)} \tag{3}$$

2.2. Clock jitter noise

The phase noise is the frequency interpretation of the time jitter. According to Leeson's model, the variance of the phase noise is given by [20]:

$$\sigma_{\Phi N}^2 = S_{n0} F_0 \frac{kT}{2P_s} \times \frac{(2\pi f_s)^2}{Q^2} \tag{4}$$

where F_0 is the noise factor, S_{n0} is the integral of the phase noise power spectral density, f_s is the oscillation (sampling) frequency, P_s is the signal power, and Q denotes the oscillator quality factor. The equivalent jitter noise in second is $\sigma_t = \sqrt{(\sigma_{\Phi N}^2)}\ /2\pi f_s$. A high quality factor and more power are required to reduce σ_t. According to the relation (4), $\sigma_t = \sqrt{(\sigma_{\Phi N}^2 / (2\pi f_s)^2)}$ is frequency independent. But, achieving a constant quality factor versus the frequency is difficult. Hence, σ_t may be increased when a higher sampling frequency is considered.

As shown in [19], the in-band jitter noise power of the modulator with an NRZ DAC is given by:

$$IBN_{j\_NRZ} = \frac{\sigma_t^2 \gamma^2 V_{FS}^2}{2^{2N_c}} (2BW)^2 OSR \tag{5}$$

where T_s is replaced by $1/(2 \times BW \times \mathrm{OSR})$ and $\gamma \times V_{FS}/(2^{Nc})$ is a coefficient of the quantizer's least significant bit (LSB) (It is assumed that the number of quantization levels for an N_c-bit quantizer is 2^{Nc}).

For a sinusoidal input signal of $V_{sig} \times \sin(\omega_{sig} t)$ and by using the model of [18], it can be shown that the in-band jitter noise of the modulator is given by:

$$IBN_{j\_RZ} = 2\sigma_t^2 V_{FS}^2 (2BW)^2 OSR \left(\frac{T_s}{T_c}\right)^2 \times \left(\frac{\lambda^2}{8} + \frac{2^{2(L_c+1)}}{12 a_c^2 \times 2^{2N_c} \times 2\pi} C(L_c)\right) \tag{6}$$

where $C(L_C) = \int_o^{\pi/2} \sin^{2L_c}(x)dx = (\sqrt{\pi}\Gamma(L_c + 1/2))/(2\Gamma(L_c + 1))$ and $\Gamma(.)$ is the Gama function. $C(L_C) = \pi/2^2, 3\pi/2^4, 10\pi/2^6$ and $35\pi/2^8$ for $L_C = 1, 2, 3$ and 4, respectively. a_c is the inverse of the loop gain. Considering the maximum amplitude of the input signal [16] and the excess loop delay in [12], a_c is estimated as:

$$a_c = \frac{(\alpha_{ELD} \times 2)^{L_c+1}}{2 + 2^{N_c}(1 - \lambda)} \tag{7}$$

where α_{ELD} is a constant term depending on the normalized excess loop delay (related to T_s), L_c and N_c. Based on the simulation results for $N_c = 3$, and $L_c = 3$, 4 and 5, we have $\alpha_{ELD} = 0.95$, 1.05 and 1.1, respectively. A typical value of α_{ELD} is 1.

As a rule of thumb (based on extensive simulation results), the RZ DAC is approximately 2^{Nc-1} times more sensitive to the clock jitter noise than the NRZ DAC. The clock jitter restricts the maximum value of OSR in modulators with NRZ and RZ DACs, respectively, as:

$$OSR \le \frac{\alpha_j NF 2^{2N_c}}{\gamma^2 V_{FS}^2 (2BW)^2 \sigma_{t-NRZ}^2} \tag{8}$$

$$OSR \le \frac{4\alpha_j NF}{\gamma^2 V_{FS}^2 (2BW)^2 \sigma_{t-RZ}^2} \tag{9}$$

where the jitter noise is assumed to be α_j (< 1) times of the modulator's noise floor.

2.3. Quantization noise

The noise transfer function of an L_C-th order modulator (without any zero optimization) is $NTF(f)=(f_s/a_c(2\pi f))^{Lc}$. Hence, the in-band quantization noise can be expressed as:

$$IBN_q = \frac{V_{FS}^2 \pi^{2L_c} a_c^2}{12 \times 2^{2N_c}(2L_c+1)(L_c-0.5)^2 OSR^{2L_c+1}} \tag{10}$$

where the term $(L_c-0.5)^2$ is due to the optimization of a pair of NTF zeros when $L_c>2$.

2.4. Limited gain bandwidth of amplifiers

The gain bandwidth (GBW) of an ideal integrator is $\omega_{u\text{-}int\text{-}i}=gf_s$, where g is the integrator gain and f_s is the sampling frequency. The integrator gain for signal path can be expressed in terms of the signal path resistor and integrating capacitor (C_I) [12] as $g\times f_s=1/RC_I$. The limited GBW of the amplifier changes the integrator's transfer function and results in a gain error and delay [21]. Approximating the amplifier by a single-pole (dominant pole) with a DC gain of A_0 and -3 dB bandwidth of ω_p, the amplifier GBW is $\omega_{uc}=A_0\times\omega_p$, and thus, the integrator transfer function is obtained as [22]:

$$H(s) = \frac{A_0 g f_s \omega_{uc}/\beta_f}{A_0 s^2 + s(g f_s A_0/\beta_f + \omega_{uc}(1+A_0)) + g f_s \omega_{uc}/\beta_f} \tag{11}$$

where β_f is a defined metric similar to the feedback factor. Considering Fig. 1, it is defined as the ratio of Thevenin equivalent resistance seen at the virtual ground of the integrator (R_{in}) to the signal path resistor (R), i.e. $\beta_f=R_{in}\ /\ R$. β_f is always equal to or less than unity. Similar to the feedback factor, reducing β_f results in more power in the amplifier. By reducing the input branches of the integrator or by using a current steering DAC, β_f can be increased up to unity.

The relation (11) has a dominant pole and its normalized GBW to the GBW of an ideal integrator is given by:

$$\frac{\omega_{u-\text{ int}}}{\omega_{u-\text{ int}-i}} = \frac{\omega_{u-\text{ int}}}{g f_s} \approx \frac{\omega_{uc}}{\beta_f g f_s + \omega_{uc}} = \frac{\omega_{uc}/f_s}{g/\beta_f + \omega_{uc}/f_s} \tag{12}$$

The GBW of a single-pole amplifier with an effective transconductance of G_{mc} and capacitance load of C_I is $\omega_{uc}=G_{mc}/C_I$. Considering $g\times f_s=1\ /\ RC_I$, ω_{uc} is equal to:

$$\omega_{uc} = G_{mc}/C_I = G_{mc}R\times g f_s \tag{13}$$

Considering the relation (12), in [22], it is stated that for a constant ratio of a real integrator GBW to the ideal one, a lower g is corresponding to the lower amplifier GBW (ω_{uc}). This state is not wrong, but it leads to a misunderstanding. According to (13), ω_{uc} is proportional to g. Hence, for a constant ω_{uc}, reducing g requires a higher G_{mc}, and thus, more power consumption in the amplifier is needed. By substituting the relation (13) into (12), the ratio of the real integrator GBW to the ideal one is obtained as:

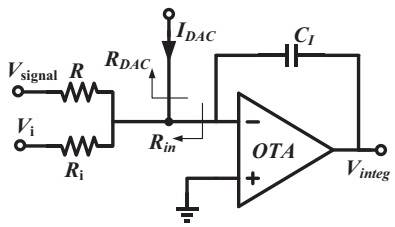

Fig. 1. Circuit level implementation of an active RC integrator.

$$\frac{\omega_{u-\text{ int}}}{\omega_{u-\text{ int}-i}} = \frac{\omega_{u-\text{ int}}}{g f_s} \approx \frac{G_{mc}\beta_f R}{1+G_{mc}\beta_f R} = \frac{G_{mc}R_{in}}{1+G_{mc}R_{in}} \tag{14}$$

Relations (13) and (14) show that $G_{mc}-R_{in}$ product is a determinant parameter for the amplifier and integrator GBW requirements, respectively. By applying additional paths to the input of the integrator or using a resistive DAC, the input equivalent Thevenin resistance of the integrator (R_{in}) is decreased. So, to preserve the $G_{mc}-R_{in}$ product constant, more power is needed to enhance the G_{mc}. Usually a current steering DAC is used in CT $\Sigma\Delta$Ms ($R_{DAC}\gg R$) and additional branches are not injected into the first integrator leading to $R_{in}\approx R$ and $\beta_f\approx 1$. So, for the sake of simplicity, $R_{in}=R$ and $\beta_f=1$ are assumed in this paper.

According to (14), for a gain error less than 1.3 dB, which leads to less than 1.3 dB increment in the in-band quantization noise, $G_{mc}R=\omega_{uc}/(gf_s)=2\pi$ is enough. Besides the gain error, the delay of integrator is also important. The second pole of $H(s)$ in relation (11) is $\omega_{p2}\approx gf_s(1+G_{mc}R)$, and so, the integrator delay in second is approximately equal to:

$$\tau_d = \frac{1}{f_s}\tan^{-1}\left(\frac{1}{g(1+G_{mc}R)}\right) \tag{15}$$

Fig. 2 illustrates the Bode diagram of the integrator transfer function given in relation (11) for $\omega_{uc}=2\pi gf_s$ ($G_{mc}R=2\pi$), $f_s=1$ and two values of integrator gain, $g=1$ and $g=0.125$. Solid lines show the ideal values while the dashed lines depict the simulated real values. For both values of g, the amplitude diagram of the ideal and real transfer functions are well matched at $\omega=f_s=1$. The phase diagram of the real transfer function with $g=1$ has a phase error of $\pi/23$ at $\omega=f_s=1$ (a delay of $0.136T_s$), while for $g=0.125$, the phase error at $\omega=f_s=1$ is $\pi/3.77$ (a delay of $0.83T_s$). The results of Fig. 2 are well matched with the predicted value of relations (14) and (15). As a result of the previous analysis, the delay of an integrator is the most important design parameter. By substituting R from the relation (3) in (15), for a relative delay less than $\alpha_\tau=\tau_d/T_s$, the G_{mc} of the front-end amplifier should be as:

$$G_{mc} \geq 1.4\frac{2.3\times 4kT(2BW)}{\alpha_{th}NF}\left(\frac{1}{g_1\tan(\alpha_\tau)}-1\right) \tag{16}$$

where g_1 is the first integrator gain (Fig. 4) and the coefficient 1.4 accounts for the worst case design while process variations

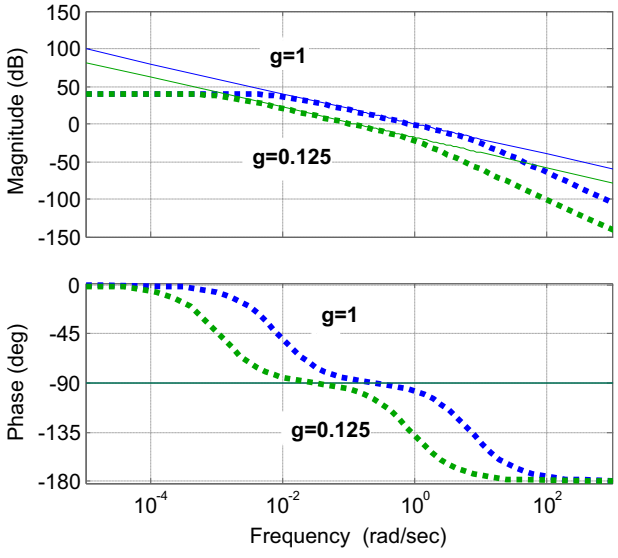

Fig. 2. Bode diagram of integrator transfer function ($H(s)$ in relation (11)) for $f_s=1$ and two values of g.

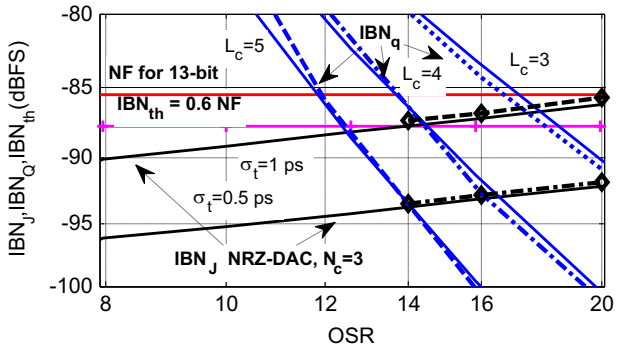

Fig. 3. In-band quantization noise of single-stage CT ΣΔMs, with $B=13$, $N_c=3$, BW=20 MHz, originated from the thermal, jitter and quantization noises.

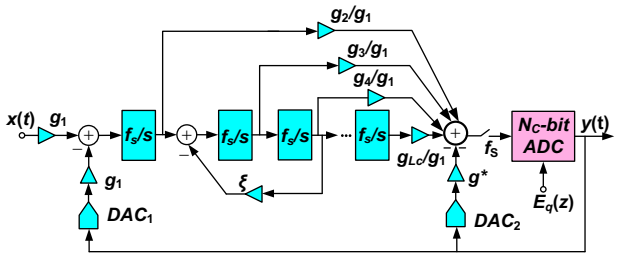

Fig. 4. Single-stage CT ΣΔM with a feedforward architecture used in the system level simulations.

cause an RC product changes up to 40%. As explained before, this RC variation is compensated by a digitally adjustable capacitor bank which may increase the value of C_I up to 40%.

Fig. 3 shows the in-band noise of single-stage CT ΣΔMs originated from three sources in 20 MHz BW with a quantizer bit-length of $N_c=3$. Solid lines show analytical values of thermal noise, noise floor, jitter noise (NRZ-DAC) and quantization noise from relations (1) (with $\alpha_{th}=0.6$)), (2), (5), and (10), respectively. The dashed lines correspond to the simulation results of both quantization and jitter noise in the modulator shown in Fig. 4. The simulation results of jitter noise are presented just in the regions where it is dominant over the quantization noise. The other noises are assumed to be mitigated by the aforementioned circuit or system level techniques such that their summation constitutes 10–20% of the modulator's noise floor.

According to Fig. 3, there is a trade off in the design of OSR. The trend of jitter noise with OSR is incremental while the quantization noise decreases when the OSR is increased.

3. Power estimation

In this section, the power of single-stage CT ΣΔMs is estimated as a function of the system level parameters. For this purpose, the power budget of each part of the modulator is separately estimated. The available power reports of recently fabricated modulators are used to validate the power estimation of each part.

3.1. Power consumption of amplifiers

For a class A amplifier, the static power constitutes approximately the overall power consumption. According to the previous assumption, the amplifiers have an effective transconductance of G_{mc}. The power consumption of each amplifier is $P_{amp}=n_b\times I_B\times V_{dd}=n_b\times(G_{mc}V_{eff}/2)\times V_{dd}$ where n_b is the number of branches, I_B is the bias current of each branch, V_{dd} is the supply voltage, and V_{eff} denotes the effective voltage of MOS transistors providing G_{mc}. Due to the first-order noise-shaping ability of the first integrator, the power consumption of the second amplifier is scaled down compared to the first one. The noise of the second amplifier is shaped by a first-order high-pass filter approximately equal to $s/(g_1\times f_s)$ in the signal bandwidth where g_1 is the gain of the first integrator. In other words, the input-referred noise power of the second amplifier is multiplied by $\int(2\pi f/(g_1\times f_s))^2/(f_s/2)\,df$, for $f=0$ to BW. Hence, its power consumption can be scaled down by $\pi^2/(3g_1^2\times OSR^3)$. According to the assumption of relation (1), the second integrator occupies only 10% of whole modulator's thermal noise, and so, the coefficient scaling should be modified as $\pi^2/(0.3g_1^2\times OSR^3)$. Using the same scaling for the next amplifiers of the loop filter excluding the last integrator and doubling their GBW for better modulator's stability, the final scaling coefficient will be $2(L_c-2)\pi^2/(0.3g_1^2\times OSR^3)$. The only exception is the last integrator which prepares a fast path for the excess loop delay compensation. Its power consumption is comparable with the first integrator [2] or even more than it [3,5]. Using the practical results of [2,3,5], the transconductance scaling of the last CT integrator related to the first one is approximately $2/(0.11OSR-0.02)$. The coefficient 2, in the scaling of the second to the last CT integrators, significantly reduces their gain error (relation (14)). Due to aforementioned explanations, the total static power consumption of a single-stage ΣΔM with L_c CT integrators is obtained as:

$$P_{Amp.s}\approx n_bV_{dd}\left\{\left(\frac{G_{mc}V_{eff}}{2}\right)\left(1+\frac{2(L_c-2)\pi^2}{0.3g_1^2OSR^3}+\frac{2}{0.11OSR-0.02}\right)\right\} \quad (17)$$

where G_{mc} is replaced from relation (16). The first and last terms are corresponding to the power of the first and last amplifiers, respectively, while the middle term estimates the power of L_c-2 remaining amplifiers.

3.2. DAC power consumption

In each modulator's sample, the CT DAC injects a current of $I_{DAC}(t)$ into its corresponding integrator. The total power consumption of each differential CT DAC is $P_{DAC}=2\times\text{mean}\{I_{DAC}^2(t)\}R_{DAC}$ where $R_{DAC}=R$ (introduced in relation (3)) is the equivalent DAC resistance and mean{.} is the averaging function. The DAC output signal is a combination of the input signal and the quantization noise. By assuming that the input signal is sinusoidal with an amplitude of $V_{FS}/2$ and the quantization noise is a random voltage with the standard deviation of $\text{LSB}/\sqrt{12}$, the average power consumption of a differential DAC is $P_{DAC\text{-}CT}=2\times(0.5\times(V_{FS}/2)^2+V_{FS}/(2^{Nc})/\sqrt{12}\ )/R$, where $V_{FS}/(2^{Nc})$ is the quantizer's least significant bit. Similar to the power scaling in amplifiers, the current of next DACs are scaled down compared to the first one owing to the noise-shaping effect. It should be noted that unlike the last amplifier, the current of the last DAC can also be scaled.

The total power consumption of DACs in CT ΣΔMs is approximated by:

$$P_{DACs}\approx\frac{V_{FS}^2}{R}\left(\frac{1}{4}+\frac{1}{\sqrt{3}\times 2^{N_c}}\right)\times\left(1+\frac{\pi^2}{0.3g_1^2OSR^3}\sum_{i=2}^{n_{DAC}}\left(\frac{g_i}{g_1}\right)^2\right) \quad (18)$$

where g_i is the gain of the i-th feedback path and n_{DAC} is the number of CT DACs. For feedforward and feedback architectures with an excess loop delay compensation path, we have $n_{DAC}=2$ and $n_{DAC}=L_c+1$, respectively.

3.3. Power consumption of clock generation

The on-chip or off-chip clock generation has its own power overhead. The clock generation power is directly related to the clock frequency and supply voltage [23]. Also as shown in relation

(4), the clock jitter (or phase noise) is inversely proportional to the admissible variance of the clock jitter. So, the power of clock generation circuit can be estimated as:

$$P_{CLK} \approx K_{CLK}\frac{V_{dd}}{\sigma_t^2}f_s = K_{CLK}\frac{V_{dd}}{\sigma_t^2} \times 2BW \times OSR \tag{19}$$

where K_{CLK} is a constant with a dimension of Ampere multiplied by cubic power of second ($A \times s^3$). A typical value of K_{CLK} can be estimated as 0.17 mW × ps^2/GHz based on the practical results of [2] (P_{CLK}=14.4 mW for V_{dd}=1.2 V, f_s=3.6 GHz and σ_t=0.23 ps).

3.4. Power consumption of quantizer(s)

Fast regenerative latches and high GBW pre-amplifiers are needed in high speed comparators to realize the quantizers. To reduce the regeneration time in latched comparators, the transconductance of transistors should be increased which results in more power consumption. Besides, the GBW of pre-amplifiers in CMOS comparators should be increased to achieve a higher sampling frequency. So, the quantizer power consumption is an exponential function of its bit-length. Also, it is a linear function of the comparison rate [24]. Therefore, the power consumption of a quantizer can be estimated as:

$$P_{quant} \approx K_{quant}V_{dd}2^{N_c}f_s + K_{DEM}V_{dd}2^{N_c}f_s \tag{20}$$

where K_{quant} and K_{DEM} are the constants of quantizer and DEM power terms with an Ampere–second (A s) dimension, respectively. In relation (20), it is assumed that the quantizer bit-length is N_c. Also, the DEM technique is used to overcome the mismatch among the DAC unit elements. Intuitively, the power consumption of a DEM technique is estimated with its own constant, K_{DEM}, similar to the power of quantizer. The reported practical results of [3,5] show 3 mW quantizer power consumption for V_{dd}=1.2 V, f_s=0.5 GHz and N_c=4 (N_d=0) leading to a typical value of K_{quant}=0.3125 mA/GHz. K_{DEM} is a percentage of K_{quant} (say K_{DEM}=0.2 K_{quant}).

3.5. Power consumption of digital circuits

The clock distribution circuits, quantizer and DAC interfaces, calibration circuits, etc, are the main part of digital circuits in ΣΔMs. The decimation filters are the main digital part of ΣΔ ADCs, but usually their power consumption are not reported [1–5], [7,8]. Besides, it may be a feasible assumption that the power overhead of the decimation filters to be the same for different modulators with the similar targeted BW and resolution (B-bit). Hence, the power consumption of the decimation filters is not considered here.

In a specific technology, a standard inverter with a supply voltage of V_{dd} and total parasitic capacitance of C_{inv} has a dynamic power consumption of $P_{inv}=C_{inv} \times {V_{dd}}^2 \times 10^6$ W/MHz. The power of digital circuits in CT ΣΔMs can be estimated as the power of some standard inverters [12] as:

$$P_{digtal} \approx L_c \times n_{G0}P_{inv}f_s \tag{21}$$

where n_{G0} is the number of standard inverters equivalent to the whole digital circuit divided by the number of integrators. A typical value of P_{inv} is 1.44 nW/MHz for C_{inv}=1 fF and V_{dd}=1.2 V. The digital circuit of the fourth-order modulator (L=L_C=4) reported in [3] consumes 165 μW for f_s=500 MHz.

The bias circuits have their own power consumption. A constant power of P_0 is assumed for the bias circuits [3,5].

According to the previous analysis, the total power consumption in single-stage CT ΣΔMs is estimated as the relation (22), where G_{mc} is replaced from the relation (16), ${\sigma_t}^2$ from (8) for an NRZ DAC and from (9) for a RZ DAC, R from (3), and f_s=2BW × OSR. Also the parameters NF and a_c are introduced in relations (2) and (7), respectively. To trade the power of the first integrator with its voltage swing, the integrator's gain can be selected as $g_1=1/\sqrt{a_c}$. The second integrator gain is assumed to be $g_2=1/\sqrt{a_c}$, while the next integrators has a unity gain ($g_3,\ldots, g_{Lc}$=1). The first integrator relative delay $\alpha_\tau=\tau_d/T_s$=0.136 is corresponding to the amplifier GBW of $\omega_u=2\pi f_s$.

$$\begin{aligned} P_{CT} \approx\ & V_{eff}V_{dd}\frac{25.76 \times kT \times BW}{\alpha_{th}NF} \\ & \times \left(\frac{1}{g_1\alpha_\tau} - 1 + 2\sum_{i=2}^{L_c-1}\left(\frac{1}{g_i\alpha_\tau} - 1\right)\frac{\pi^2}{0.3g_1^2OSR^3} \right. \\ & \left. + \frac{2(1/(g_{L_c}\alpha_\tau) - 1)}{0.11OSR - 0.02}\right) + \frac{{V_{FS}}^2}{\alpha_{th}NF}\left(\frac{1}{4} + \frac{1}{\sqrt{3} \times 2^{N_c}}\right) \\ & \left(1 + \frac{\pi^2}{0.3g_1^2OSR^3}\sum_{i=2}^{n_{DAC}}\left(\frac{g_i}{g_1}\right)^2\right)2.3kT(2BW) \\ & + K_{CLK}\frac{{V_{dd}}^2\gamma^2{V_{FS}}^2}{(0.8 - \alpha_{th})NF \times 2^{2N_c}}(2BW)^3OSR^2 + (K_{quant} + K_{DEM}) \\ & V_{dd}2^{N_c}(2BW)OSR + P_{inv}L_cn_{G0}(2BW)OSR + P_0 \end{aligned} \tag{22}$$

The bandwidth of ADC's input signal and also the ADC's sampling rate are well below the technology maximum speed (f_T) [1–9]. Therefore, all of the circuit level models are considered at frequencies well below f_T.

The technology scaling reduces the parameters V_{dd}, K_{CLK}, K_{quant}, K_{DEM}, and P_{inv}. In a scaled CMOS technology, there are less parasitic capacitances, and hence, a higher bandwidth can be achieved with a predetermined transconductance (G_m). However, the scaling of power supply voltage (V_{dd}) reduces the full-scale voltage (V_{FS}) of the input signal, and consequently, for a given dynamic range (DR), a lower noise floor is needed. This is more visible in the migration from a 180 nm technology to a 90 nm one. But, since the voltage supply is almost remained constant around 1 V for CMOS technologies with feature sizes less than 90 nm, it is difficult to judge about the effect of CMOS technology scaling on the power consumption of analog circuits. Just, it can be said that the scaling of CMOS technology cannot reduce the power of analog circuits as well as the power of digital circuits.

3.6. Simulation results

Fig. 5 illustrates the power consumption of CT ΣΔMs versus the required BW for three different values of the modulator's order (L_C) with N_c=3 and OSR=12. The curve has a linear part corresponding to the power of amplifiers, DACs, digital circuits, and quantizer. The third order region of Fig. 5 is due to the power of

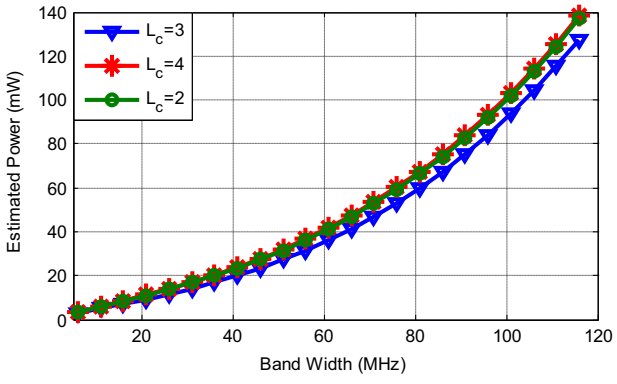

Fig. 5. Estimated power versus the BW for three different orders of loop filter (L_C) in single-stage CT ΣΔMs with B=13, N_C=3, OSR=12, and α_{th}=0.7.

the clock generation circuits. For input signal bandwidths less than 60 MHz, the linear part is dominant, while beyond it, the third order term becomes more important.

Fig. 6 shows the estimated power consumption of CT ΣΔMs for different values of OSR and quantizer bit-length. The power consumption can be minimized for a specific OSR or bit length depending on the other system level parameters especially the targeted bandwidth. Using similar plots extracted from the relation (22), the system level parameters of CT ΣΔMs can be designed for the minimum power consumption.

Table 1 summarizes the reported power and corresponding designed parameters of several best fabricated single-stage CT ΣΔMs, while for each one the estimated power in relation (22) is presented. As it is seen, there is a good matching between the estimated and experimental power consumptions. In this table, the FoM is defined as $P/(2^B \times 2\text{BW})$ where $B=[DR(\text{dB})-1.76]/6.02$. The clock generation power was not reported for references in Table 1, and hence, this part is removed from the estimated power as well. The quantizer bit-length in [1] is 4, while the quantizer power is reduced to a 3-level quantizer by digital techniques, as considered in its power estimation. As explained in Section 2.4, for parameters of [4], $C_I = 1/(R \times g_1 f_s) = 20$ fF which is less than C_{I0}, and so, $C_{I0}=200$ fF and $G_{mc}=C_{I0} \times 2\pi f_s$ are considered in the power estimation of [4].

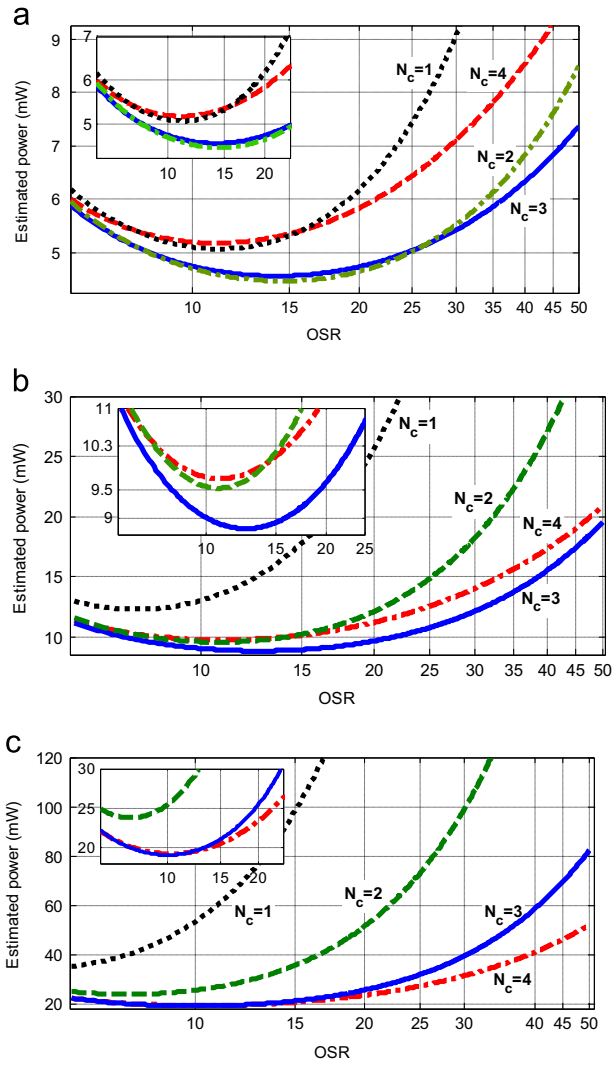

Fig. 6. Estimated power of a single-stage CT ΣΔM versus the OSR and N_c for $B=13$, $L_c=3$ and $\alpha_{th}=0.7$, with (a) BW=10 MHZ, (b) BW=20 MHz, and (c) BW=40 MHz.

3.7. Discussion for special case of $N_c=1$

A single-bit quantizer ($N_c=1$) is often used in the design of sigma-delta modulators [2,12,16]. In this case, the power consumption of the quantizer and its corresponding circuit's complexity are minimized and the feedback DAC does not require any linearization algorithm (K_{DEM} will be zero in relations (20) and (22)). However, a single-bit quantizer has some drawbacks especially in the high resolution wideband applications as follows

1. Due to the large amount of injected quantization noise into the loop filter, the modulator's stability is degraded. This issue is more critical for higher order of noise-shaping (L_C). The out-of-band gain of the modulator's NTF should be reduced enough to handle this large amount of the quantization noise, especially for higher values of L_c where the out-of-band gain of the NTF is large and the stability is more affected by the excess loop delay. The inverse of loop gain, a_c, defined in relation (7), considers the aforementioned stability requirement. By reducing N_c and/or increasing L_c, the parameter a_c is increased such that the out-of-band gain of the NTF remains constant. Besides, α_{ELD} models the sensitivity of higher order modulators to the excess loop delay.
2. The lower number of quantization levels limits the aggressive noise-shaping while simultaneously the quantization noise power is increased. So, a higher OSR with its own power penalty should be used to suppress the quantization noise. This is modeled in relation (10).
3. The output signal of a single-bit DAC has large variations and it consumes more power as shown in relation (18). Besides, the large variations of the DAC output signal enhance the effect of clock jitter which is modeled in relations (5) and (6), for NRZ-DAC and RZ-DAC, respectively. To preserve the modulator's performance, the admissible value of clock jitter (relation (4)) should be reduced which requires more power (relation (19)). In other words, although in relation (22), the power of the quantizer is reduced when $N_c=1$, but the power of the clock generation block and the feedback DACs can significantly be increased.

According to Fig. 3, the value of OSR trades the quantization noise suppression with the jitter noise reduction. A higher OSR is required to suppress the quantization noise, while it increases both the clock jitter noise (relation (4)) and the modulator's

Table 1
Comparison of the estimated power from relation (22) with the reported power of several state-of-the-art wideband CT ΣΔMs.

Reference	*Modulator order L_c*	N_c (bit)	BW (MHz)	OSR	B (bit)	Power (mW)	FoM *fJ*/conv.-step	Estimated power (mW)	V_{dd} (V)
[1]	4	3.2	18	17.8	12.5	3.7	17.74	4	1.2
[2]	4	1	36	50	13.5	15	18	14.8	1.2
[3]	3	4	25	10	12	8.5	51	6.3	1.2
[4]	3	1	60	50	10.5	20	162.7	18.5	1.4
[5]	3	4	25	10	11.5	8	63.4	5.4	1.2
[8]	3	4	20	16	13	20	61	15.5	1.8

sensitivity against the clock jitter (relations (5) and (6) for NRZ-DAC and RZ-DAC, respectively).

Therefore, the conventional single-loop CT ΣΔMs with a single-bit quantizer are not suitable for high resolution wideband applications. This can be inferred from Fig. 6 where $N_c=1$ leads to the highest power consumption. Although the modulator of [2] is designed for high resolution wideband applications by employing a single-bit quantizer, but it uses an on-chip phase locked loop (PLL) to reduce the clock jitter noise and a FIR-DAC to reduce the modulator's sensitivity against the clock jitter. The power consumption of the PLL circuit in [2] is approximately the same as the whole modulator's power and the large delay of the utilized FIR-DAC results in an undesirable peak in the signal transfer function (STF) [2].

4. Power optimization algorithm

For a given targeted BW and resolution (B-bit), the relation (22) can be minimized provided that $\alpha_{th}+\alpha_j+\alpha_q+\alpha_{other}=1$. Respectively, α_{th}, α_j, α_q and α_{other} are the share of thermal noise, clock jitter noise, quantization noise and other errors (mitigated errors like the DAC elements mismatch) in the modulator's noise floor. The selected values of L_C, N_c and OSR should suppress the quantization noise according to the relation (10) well below the modulator's noise floor. As a simplifying assumption, $\alpha_{other}=\alpha_q=0.1$ leads to $\alpha_j=0.8-\alpha_{th}$. Thus, the design parameters of single-stage CT ΣΔMs are L_C, N_c, OSR, and α_{th}.

4.1. Power optimization algorithm

The proposed power minimization algorithm is summarized as:

1. For a given *BW* and resolution (*B*-bit), set the *NF* and the values of α_τ, K_{quant}, K_{DEM}, V_{eff}, K_{CLK}, n_{G0}, and P_0 based on technology, experimental results, and previous experiences. Typically, $\alpha_\tau=0.136$, $K_{quant}=0.3125$ mA/GHz, $K_{DEM}=0.2K_{quant}$, $V_{eff}=0.2$ V, $K_{CLK}=0.17$ mA $\times$ $(ps)^2$/GHz, $P_{inv}=1.44$ nW/MHz, $n_{G0}=76$, and $P_0=0.7$ mW.
2. Choose L_C, N_c and OSR. Compute a_c from the relation (7), and IBN_q from the relation (10).
3. If $IBN_q \le \alpha_q \times NF$ continue, otherwise go back to step 2.
4. For various values of α_{th}, compute the power consumption from the relation (22) and save the minimum power and its corresponding design parameters.
5. Repeat the steps 3 and 4 to cover all possible values of L_C, N_c, and OSR. Recommended ranges are as follows: $0.45 \le \alpha_{th} \le 0.75$, $1 \le N_c \le 5$, $3 \le L_c \le 5$, and $8 \le \text{OSR} \le 50$.
6. Between the saved values of step 5, find the minimum power and its corresponding design parameters.

Using the proposed algorithm with the aforementioned typical values, Table 2 reports the design parameters corresponding to the minimum power of CT ΣΔMs for two different BWs of 10 MHz and 20 MHz and 13-bit resolution provided that $IBN_q=\alpha_q \times NF$. For example, Fig. 6(b) shows that in a 20 MHz bandwidth, the minimum power is corresponding to $L_c=3$, $N_c=3$, and OSR=12. But these values cannot satisfy the relation $IBN_q=\alpha_q \times NF$. Hence, according to Table 2, for this example, the optimum system level design of the modulator is $L_c=3$, $N_c=4$, and OSR=16 which leads to $IBN_q=\alpha_q \times NF$ and it is well matched with the design of [3,5] and [8]. Also, the design of $L_c=4$, $N_c=3$, and OSR=16 for $B=13$, which is suggested in [1], is very close to the optimum design.

Table 2
Design parameters corresponding to the minimum estimated power of a 13-bit single-stage CT ΣΔM for two different bandwidths (clock generation power is not considered).

Design parameters	10 MHz bandwidth	20 MHz bandwidth
OSR	24	16
Quantizer bit-length	$N_c=3$	$N_c=4$
V_{dd}	1.2 V	1.2 V
Modulator order	$L_c=3$	$L_c=3$
α_{th}	0.7	0.7
Estimated power	4.9 mW	10.3 mW
Circuit level simulated power	5.1 mW	11 mW

4.2. Design example

In order to evaluate the power estimation accuracy in Table 1, two conventional CT ΣΔMs have been also simulated at the circuit level using a 90 nm CMOS technology and their corresponding simulated power is also reported in Table 2. As shown in Table 2, the simulated circuit level power is very close to its estimated one. The clock generation power has not been simulated in these reported values.

In these circuit level simulations, the conventional modulator is realized using two-stage OTAs with the feed-forward compensation [2], a conventional flash ADC [24], and resistive DACs [12]. Both simulated modulators are third order with a feedback architecture and 3-bit quantizer. The first modulator bandwidth and OSR are 10 MHz and 24, respectively, while the second

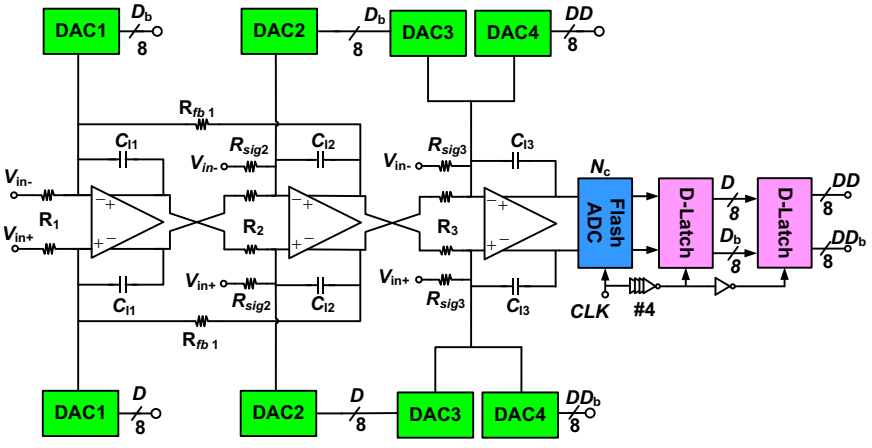

Fig. 7. The circuit level schematic of the simualted single-stage CT ΣΔM for $N_c=3$, $L_c=3$ with the excess loop delay compensation ($T_s/2$).

modulator has a bandwidth of 20 MHz and OSR=16. Fig. 7 shows the circuit level schematic of the simulated modulators and their circuit level and system level parameters are reported in Tables 3 and 4 for BW=10 and 20 MHz, respectively. The system-level parameters are the feedback gains ($g_{1,2,3}$), gain of the excess loop delay compensation path (g^*), and the local feedback gain (k_{f1}). The first D-latch samples the quantizer output by a delayed version of the clock to remove the signal dependent delay of the quantizer [8]. By using the output signal of the first and second D-latches, the feedback signal multiplied by $k^*(1-z^{-1/2})$ is injected into the last integrator through DAC_3 and DAC_4. In this way, an excess loop delay up to $0.5\times T_s$ is compensated for while no amplifier is needed prior to the quantizer [8]. In order to reduce the voltage swing of the last integrator, its gain is reduced by a coefficient of 2/3 in both simulations, while this is compensated for by the quantizer gain of 1.5.

Fig. 8 shows the circuit level realization of the quantizer including the comparator, resistive ladder, and SR latch. The gain of quantizer was increased to 1.5 by the reference voltage scaling (VREFP=1 V and VREFN=0.2 V while V_{DD}=1.2 V). The comparator utilizes a fully-differential pre-amplifier to reduce both the offset and kick-back noise of the regenerative latch. The latch is regenerated at the falling edge of the clock. It is designed to be fast enough in order to reduce the meta-stability errors. SR latches are utilized to save the data during the latch reset phase.

Fig. 9 illustrates the structure of the utilized two-stage feed-forward compensated amplifier in both simulations. A two-stage amplifier is selected to achieve both large DC gain and high output swing. A feed-forward compensation scheme through M_{n5} and

Table 3
Design parameters corresponding to the modulator of Fig. 7 for BW=10 MHz.

Parameter	Value	Parameter	Value
R_1	3 kΩ	R_{fb1}	150 kΩ
C_{I1}	1.4 pF	R_3	14 kΩ
R_{DAC1} (unit)	24 kΩ	C_{I3}	225 fF
R_2	10.2 kΩ	R_{DAC3} (unit)	45 kΩ
C_{I2}	300 fF	R_{sig3}	8.2 kΩ
R_{DAC2} (unit)	60 kΩ	R_{DAC4} (unit)	148 kΩ
R_{sig2}	7.5 kΩ	N_c	3
g_1	0.34	g_2	0.93
g_3	1.7	g^*	0.75
k_{f1}	0.01	f_s	480 MHz

Table 4
Design parameters corresponding to the modulator of Fig. 7 for BW=20 MHz.

Parameter	Value	Parameter	Value
R_1	1.5 kΩ	R_{fb1}	68 kΩ
C_{I1}	1 pF	R_3	15.6 kΩ
R_{DAC1} (unit)	24 kΩ	C_{I3}	150 fF
R_2	17.5 kΩ	R_{DAC3} (unit)	43.2 kΩ
C_{I2}	150 fF	R_{sig3}	7.8 kΩ
R_{DAC2} (unit)	64 kΩ	R_{DAC4} (unit)	140 kΩ
R_{sig2}	8 kΩ	N_c	4
g_1	0.62	g_2	1.3
g_3	2	g^*	0.9
k_{f1}	0.023	f_s	640 MHz

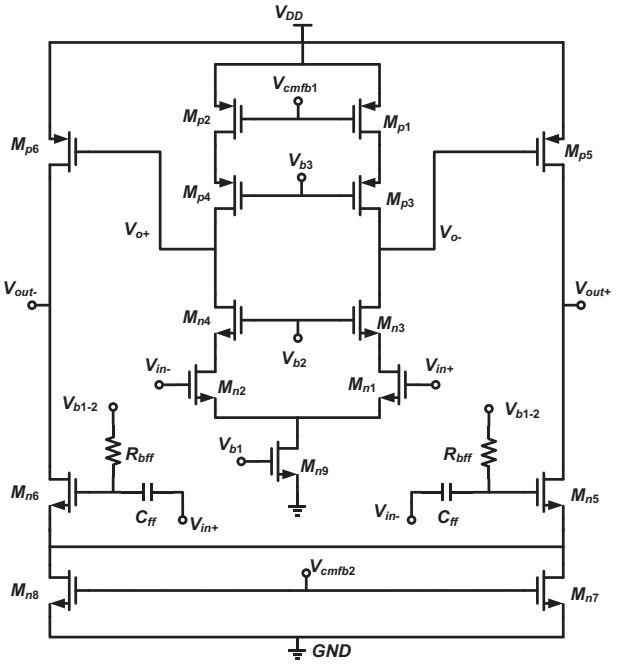

Fig. 9. Feedforward compensated two-stage OTA.

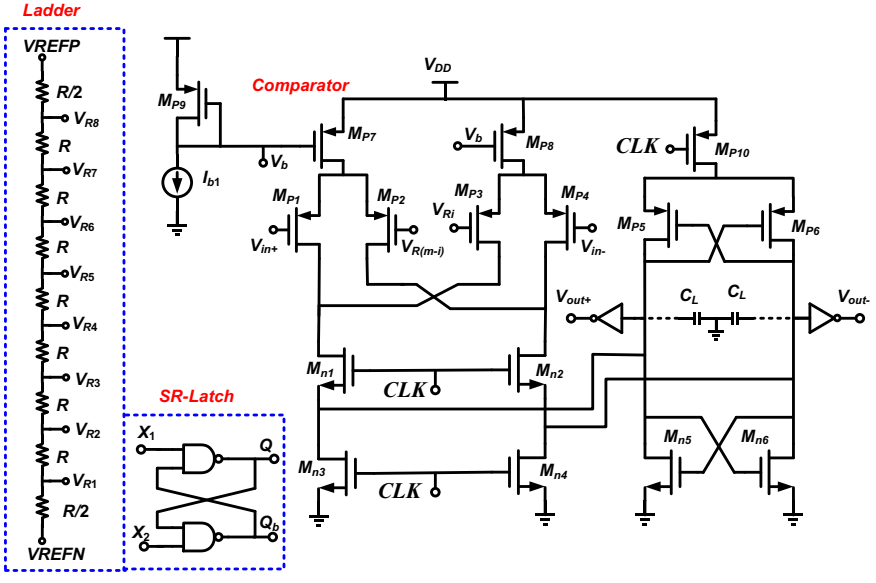

Fig. 8. Building blocks of flash ADC including the comparator, resistive ladder, and SR latch.

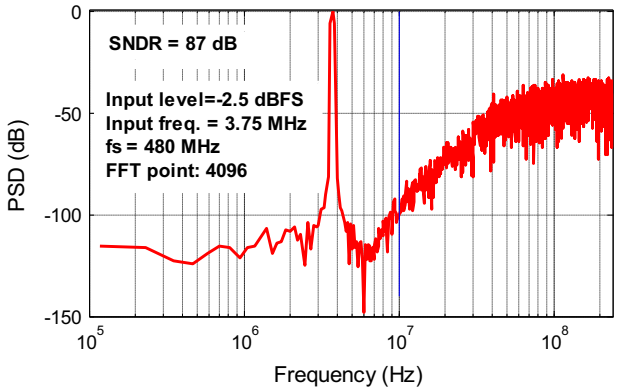

Fig. 10. Simulated circuit level PSD of the CT ΣΔM with BW=10 MHz, N_c=3 and OSR=24 (excluding the circuit thermal and jitter noises).

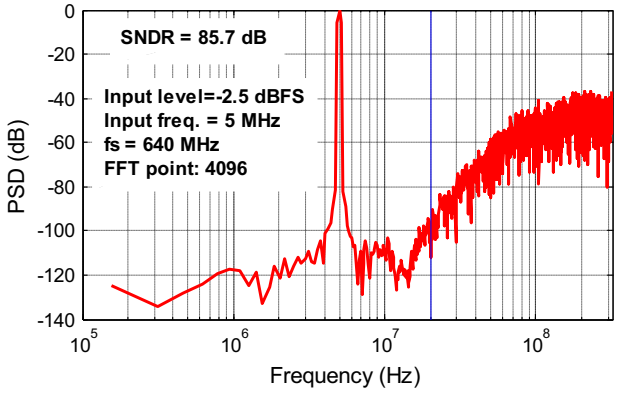

Fig. 11. Simulated circuit level PSD of the CT ΣΔM with BW=20 MHz, N_c=4 and OSR=16 (excluding the circuit thermal and jitter noises).

M_{n6} transistors is utilized to achieve sufficient stability with lower power consumption. Although due to the pole-zero doublet, this amplifier's transient response is not suitable for discrete-time applications, but it is well adapted for CT applications [2]. The common-mode feedback voltages of the first and second stages are controlled separately via nodes of V_{cmfb1} and V_{cmfb2}, respectively.

In the first simulation, the GBW of first, second, and third amplifiers were f_{GBW1}=492 MHz, f_{GBW2}=1000 MHz, f_{GBW2}=1100 MHz, respectively. The GBW of first, second, and third amplifiers in the second simulation were f_{GBW1}=665 MHz, f_{GBW2}=1230 MHz, f_{GBW2}=1230 MHz, respectively. In both simulations, the DC gain of all amplifiers was about 50 dB, while their phase margins were better than 57 degree.

The simulated output power spectral density (PSD) of both modulators is shown in Figs. 9 and 10 for BW=10 MHZ and 20 MHz, respectively. The circuit noise is not considered in the reported SNDR in these figures. By considering the circuit noise, the SNDR of both simulations will be limited to about 82 dB (Fig. 11).

5. Conclusions

In this paper, the main error sources and the power consumption in single-stage CT ΣΔMs are analytically extracted. Based on analytical results, for a targeted BW and resolution, an algorithm is proposed to minimize the power consumption by a suitable design of the system level parameters including OSR, quantizer bit-length, noise-shaping order, and thermal noise level. The analytical power estimations and the designed parameters are well matched with the best state-of-the-art CT ΣΔMs. In other words, by using the proposed analytical results, the power consumption of different possible designs of a CT ΣΔM with an active RC implementation can be compared to choose the best one, while the power estimation of the selected system is also available for the next design steps.

References

[1] Y.-S. Shu, J.-Y. Tsai, P. Chen, T.-Y. Lo, and P.-C. Chiu, A 28 fJ/conv-step CT ΔΣ modulator with 78 dB DR and 18 MHz BW in 28 nm CMOS using a highly digital multibit quantizer, in ISSCC Digest Technical Papers, February 2013, pp. 268–270.
[2] P. Shettigar, S. Pavan, Design techniques for wideband single-bit continuous-time ΣΔ-modulators with FIR feedback DACs, IEEE J. Solid-State Circuits 47 (12) (2012) 2865–2879.
[3] P. Witte, J.G. Kauffman, J. Becker, Y. Manoli, and M. Ortmanns, A 72dB-DR ΔΣ CT modulator using digitally estimated auxiliary DAC linearization achieving 88 fJ/conv in a 25 MHz BW, in ISSCC Digest Technical Papers, February 2012, pp. 154–155.
[4] V. Srinivasan, V. Wang, P. Satarzadeh, B. Haroun, and M. Corsi, A 20 mW 61 dB SNDR (60 MHz BW) 1b 3rd-Order continuous-time delta-sigma modulator clocked at 6 GHz in 45 nm CMOS, in ISSCC Digest Technical Papers, February 2012, pp. 158–160.
[5] J.G. Kauffman, P. Witte, J. Becker, M. Ortmanns, An 8.5 mW continuous-time ΣΔ modulator with 25 MHz bandwidth using digital background DAC linearization to achieve 63.5 dB SNDR and 81 dB SFDR, IEEE J. Solid-State Circuits 46 (12) (2011) 2869–2881.
[6] M. Bolatkale, L.J. Breems, R. Rutten, K.A. Makinwa, A 4 GHz continuous-time ADC with 70 dB DR and 74 dBFS THD in 125 MHz BW, IEEE J. Solid-State Circuits 46 (12) (2011) 2857–2868.
[7] W. Yang, W. Schofield, H. Shibata, S. Korrapati, A. Shaikh, N. Abaskharoun, and D. Ribner, 100 mW 10 MHz-BW CT ΔΣ modulator with 87 dB DR and 91 dBc IMD, in ISSCC Digest Technical Papers, February 2008, pp. 498–450.
[8] G. Mitteregger, C. Ebner, S. Mechnig, T. Blon, C. Holuigue, E. Romani, A 20-mW 640-MHz CMOS continuous-time ΣΔ ADC with 20-MHz signal bandwidth, 80-dB dynamic range and 12-bit ENOB, IEEE J. Solid-State Circuits 41 (12) (2006) 2641–2649.
[9] S. Patón, A.D. Giandomenico, L. Hernández, A. Wiesbauer, T. Pötscher, M. Clara, A 70-mW 300-MHz CMOS continuous-time ΣΔ ADC with 15-MHz bandwidth and 11 Bits of resolution, IEEE J. Solid-State Circuits 39 (7) (2004) 1056–1063.
[10] J. Ruiz-Amaya, J.M. de la Rosa, F.V. Hernández, F. Medeiro, R. del Río, B. Pérez-Verdú, A. Rodríguez-Vázquez, High-level synthesis of switched-capacitor, switched-current and continuous-time ΣΔ modulators using SIMULINK-based time-domain behavioral models, IEEE Trans. Circuits Syst. I: Regul. Pap. 52 (9) (2005) 1795–1810.
[11] T. Brückner, C. Zorn, J. Anders, J. Becker, W. Mathis, M. Ortmanns, A GPU-accelerated web-based synthesis tool for CT sigma-delta modulators, IEEE Trans. Circuits Syst. I: Regul. Pap. 61 (5) (2014) 1429–1441.
[12] M. Ortmanns, F. Gerfers, Continuous-Time Sigma-Delta A/D Conversion, Springer, 2005.
[13] R. Schoofs, M.S.J. Steyaert, W.M.C. Sansen, A Design-optimized continuous-time delta–sigma ADC for WLAN applications, IEEE Trans. Circuits Syst. I: Regul. Pap. 54 (1) (2007) 209–217.
[14] S. Pavan, N. Krishnapura, R. Pandarinathan, P. Sankar, A power optimized continuous-time ΣΔ ADC for audio applications, IEEE Trans. Circuits Syst. I: Regul. Pap. 43 (2) (2008) 351–360.
[15] M. Safi-Harb, G.W. Roberts, Low power delta–sigma modulator for ADSL applications in a low-voltage CMOS technology, IEEE Trans. Circuits Syst. I: Regul. Pap. 52 (10) (2005) 2075–2089.
[16] R. Schreier, G.C. Temes, Understanding Delta-Sigma Data Converters, Wiley/IEEE Press, 2005.
[17] J.A. Cherry, W.M. Snelgrove, Continuous-time Delta-Sigma Modulators for high-speed A/D Conversion, Kluwer Academic Publisher, Dordrecht, 1999.
[18] X. Chen, A Wideband Low-power Continuous-time Delta-sigma Modulator for Next Generation Wireless Applications (Ph.D. dissertation thesis), Oregon State University, Corvallis, OR, 2007.
[19] H. Pakniat, M. Yavari, A ΣΔ-FIR-DAC for multi-bit ΣΔMs, IEEE Trans. Circuits Syst. I: Regul. Pap. 60 (9) (2013) 2321–2332.
[20] D.B. Leeson, A simple model of feedback oscillator noise spectrum, Proc. IEEE (1966) 329–330.
[21] J.G. Kauffman, T. Bruckner, M. Ortmanns, A comprehensive analysis of the effect of finite amplifier bandwidth and excess loop delay in continuous-time sigma-delta modulators, Microelectron. J. 40 (2009) 1736–1745.
[22] S.D. Kulchycki, R. Trofin, K. Vleugels, B.A. Wooley, A 77-dB dynamic range, 7.5-MHz hybrid continuous-time/discrete-time cascaded ΣΔ modulator, IEEE J. Solid-State Circuits 43 (4) (2008) 796–804.
[23] S. Docking, M. Sachdev, An analytical equation for the oscillation frequency of high-frequency ring oscillators, IEEE J. Solid-State Circuits 39 (3) (2004) 533–537.
[24] F. Maloberti, Data Converters, Springer, The Netherlands, 2007.