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A push-pull FVF based LDO voltage regulator with slew rate enhancement at the gate of power transistor

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ABSTRACT

A low-dropout (LDO) voltage regulator based on a push-pull flipped voltage follower cell with slew rate improvement at the gate of power transistor is presented. The proposed three-stage regulator exploits two separate signal paths by cross-coupled common-gate cells to improve the transient response and loop stability with low power consumption. Moreover, a slew rate enhancement technique is employed at the gate of power transistor by adding a new current signal path which also improves the small-signal behavior. It is simulated in Cadence with a 90 nm CMOS process, 2.1 μW minimum power dissipation, and 150 mV dropout voltage for 0.9–1.2 V input voltage. It is stable over a range of 40 μA–100 mA load currents and 100 pF load capacitor. The achieved settling time is about 1.2 μs when the load current changes from 40 μA to 100 mA with 200 ns rise time. The obtained line and load regulations are 0.4 mV/V and 6 μV/mA, respectively.

1. Introduction

Power management systems are extensively used in many low voltage portable applications such as system-on-chip (SoC), energy-efficient internet-of-things (IoT) sensor networks and implantable biomedical systems to provide ripple-free and clean power supplies in order to increase the battery life [1–3]. Thus, the power management is one of the most essential and challenging sections in the design of low voltage applications. Since, low-dropout (LDO) regulators are the vital components in power management systems, they play a great role in the efficiency of power management in terms of their output noise and power supply rejection (PSR) characteristics, good output regulation, and relatively simple structure due to their fast transient response, clean output, and ease of integration [4,5]. In low voltage applications, voltage regulators should maintain clean and ripple free output voltage; consume as small quiescent current as possible and low dropout voltage to prolong the battery life, occupy small chip area, and achieve stable operation over large load currents [6,7]. Nevertheless, keeping low dropout voltage and lowering quiescent current for a LDO regulator are the most demanding keys along with meeting highly enough loop stability and fast transient response behavior.

Several structures of LDO voltage regulators have been reported in Refs. [8–13]. In Ref. [8], the proposed regulator comprises of two flipped voltage follower (FVF) structures with a subsequent push–pull output stage forming the error amplifier for boosting the transient response with only 1.2 μA no-load current. Nonetheless, having a small DC open-loop gain causes the regulator to suffer from poor line and load regulations (LNR and LDR) and degrades the transient response of the regulator. In Ref. [9], an additional stage in the error amplifier is employed in the FVF based regulator in Ref. [8] in order to extend the DC open-loop gain and improve both LNR, LDR, and power supply rejection ratio (PSRR). Nevertheless, the minimum load current is limited to 3 mA for maintaining the stability of this regulator under applying a 50 pF output load capacitor and it consumes 8 μA quiescent current. The minimum load current operation restricts the regulator flexibility in low voltage applications in which low load currents are required.

Another fast transient FVF regulator using a dual dynamic load composite gain stage has been demonstrated in Ref. [10]. Not only is limited the maximum load current of this regulator to only 10 mA, but also very large on-chip capacitors (totally 16 pF) have been used to stabilize the regulator under a small range of the load current. Furthermore, a higher value 50 μA quiescent current in no-load condition has dedicated to this structure. In Ref. [11], unlike the output stage structure as stated for the regulator in Ref. [8], a disparate telescopic-cascode architecture is deployed as the output stage of the

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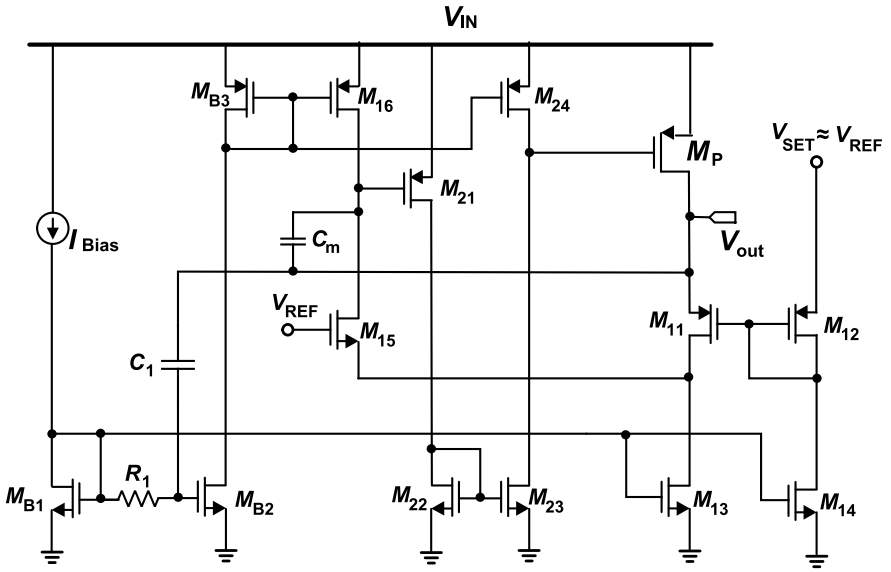

Fig. 1. Structure of LDO regulator in Ref. [9].

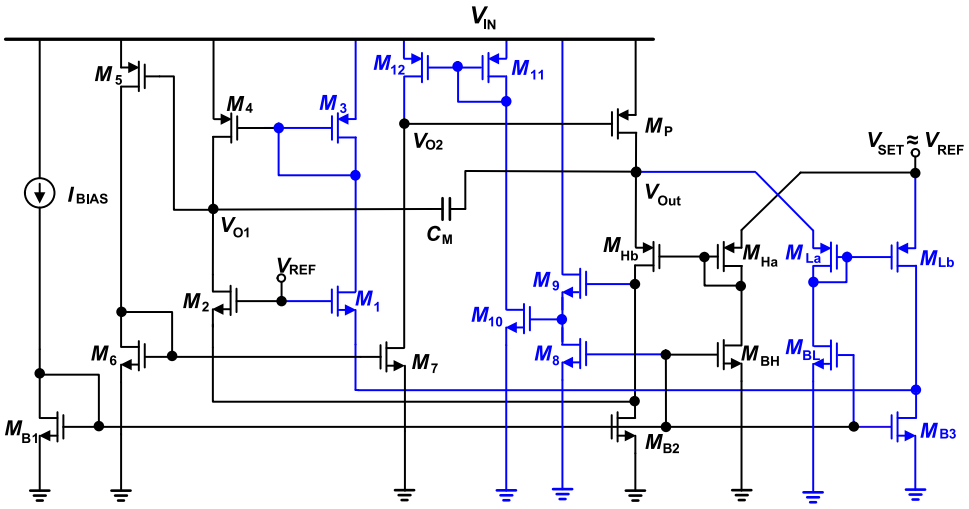

Fig. 2. Proposed push-pull FVF based LDO voltage regulator.

regulator with the aim of causing more increasing in the loop gain compared to the structure presented in Ref. [8]. Moreover, a dual-path active-feedback frequency compensation technique is also implemented to provide stability for the regulator within the required gain bandwidth (GBW). However, quite large on-chip compensation capacitors are demanded to maintain sufficient stability for the regulator. On the other hand, the development over LNR and LDR parameters have not been significantly obtained despite of consuming a rather high quiescent current of 14 μA.

The LDO regulator in Ref. [12] results in a lower dropout voltage of 50 mV in order to enhance the power efficiency. Whereas, reducing dropout voltage causes the LDO regulator to suffer from several issues such as low DC loop gain, poor PSR, and large chip area due to requiring larger power transistor size. Accordingly, by using a self-supplied gain boost stage, the open-loop gain of the FVF-based LDO has been increased. In addition, by exploiting a coupled transient enhancement unit, the LDO regulator is fully recovered within only 220 ns for a 0–20 mA load transient with 100 ps rise time. Regardless, a load capacitor up to 30 pF is used for the LDO regulator with 33 μA quiescent current that it is only suitable for working on regulators in a digital system. Comprehensively, designing an output capacitorless LDO regulator with ultra-low power and fast transient response as well as good stability and optimized DC regulation will be much more challenging.

In [13], a high-gain and low-power FVF based LDO voltage regulator has been developed. For improving the open-loop gain in order to achieve high LNR, LDR and PSRR, a three-stage error simplifier has been utilized. Therefore, a substantial compensation network including three different compensation schemes have employed to meet the required stability for the regulator. Since the quiescent current is only 1.83 μA, an adaptive biasing network has been also employed to provide sufficient GBW at large load currents and enhance slew rate at the gate of power transistor. Nevertheless, the complexity of compensation network and the LDO restriction on its operation at large load currents can be even improved.

This paper presents a novel LDO voltage regulator structure proceeded from the LDO regulator reported in Ref. [9]. The most restrictive parameters for a LDO regulator by focusing in low voltage applications are chip area and power consumption, the desirable LDO regulator shall meet these requirements. As previously described, the LDO reported in Ref. [9], which is shown in Fig. 1, cannot be stable under load currents

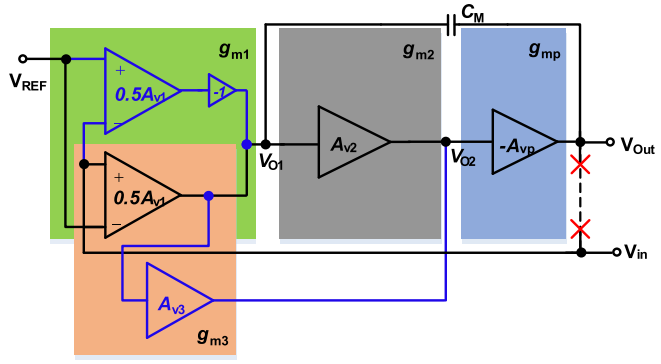

Fig. 3. Conceptual block diagram of the proposed LDO regulator.

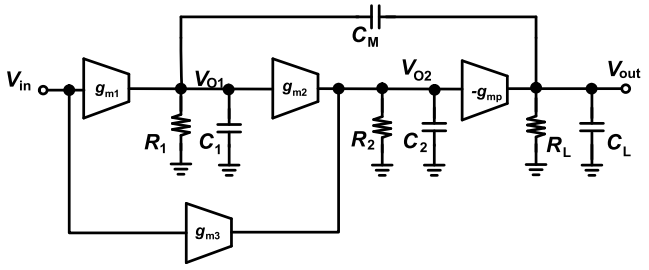

Fig. 4. Equivalent open-loop circuit of the proposed three-stage LDO voltage regulator.

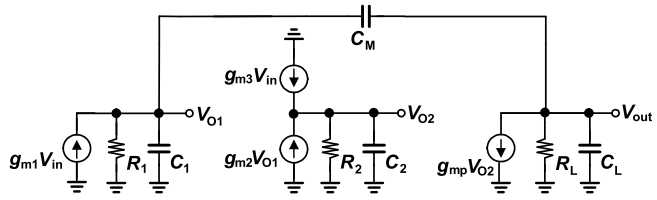

Fig. 5. Small-signal model of the proposed LDO voltage regulator.

smaller than 3 mA and it uses 7 pF on-chip capacitor for maintaining the stability over load currents from 3 mA to 100 mA. Based on this demonstration, in this paper, a push-pull FVF based regulator with slew rate enhancement at the gate of the power transistor is proposed without needing a voltage spike detection circuit. The proposed LDO regulator is compensated by a simple small Miller compensation capacitor to provide enough stability for even load currents down to 40 μA. On the other hand, transient responses of the proposed regulator under ultra-low quiescent current are also improved significantly.

In this paper, the architecture of the proposed LDO voltage regulator and its stability analysis are described in Section 2, Subsequently, load transient response evaluation and the circuit level implementation of the proposed LDO regulator are addressed in this section too. The post-layout simulation results and discussions are presented in Section 3. Finally, Section 4 concludes the paper.

2. Proposed LDO voltage regulator

A description of the proposed three-stage LDO voltage regulator architecture is explained and then its analysis and circuit level implementation are introduced.

2.1. Architecture of the proposed LDO voltage regulator

Fig. 2 illustrates the full schematic of the proposed push-pull FVF LDO voltage regulator with high loop gain and slew rate enhancement circuit. By combining another differential common-gate transconductance cell (G_{mL}) including M_{La}, M_{Lb} and M_{BL} transistors compared to the structure in Ref. [9], these two-differential common-gate transconductance cells (G_{mH}, G_{mL}) with $M_{1\text{-}4}$ transistors form a push-pull FVF amplifier as the first gain stage. Transistors $M_{5\text{-}7}$ constitutes the second gain stage so that it builds a non-inverting amplifier. Furthermore, another additional branch of current signal by transistors $M_{8\text{-}12}$ is added compared with the structure of power transistor reported in Ref. [9] to increase the open-loop gain and enhance the slew rate at the gate of the M_P power transistor. Conceptual architecture of the proposed three-stage push-pull FVF regulator is shown in Fig. 3 where V_{O1}, V_{O2} and V_{Out} are the output voltages of each stage in the proposed regulator. C_M is the Miller compensation capacitor and the A_{v3} stage is the additional branch including transistors $M_{8\text{-}12}$ to both charge/discharge more currents to the gate of the power transistor when the output voltage suddenly changes in the transient state and boost the DC gain in the small-signal behavior.

2.2. Stability analysis

First step of analyzing the LDO regulator stability is to be broken the feedback path from the output node of regulator to the inverting input of error amplifier as illustrated in Fig. 3. For the sake of simplicity, the loading effects of input node (impedances of G_m cells) at the output side of the regulator are overlooked. However, a resistance impact by the input side of feedback equivalent to $\left(\frac{1}{g_{m,La}}\middle\|\frac{1}{g_{m,Hb}}\right)=\frac{1}{g_{m,La}+g_{m,Hb}}$ is being observed in parallel with the resistance load affected by feedback loop splitting. Since the load resistor changes are from 7 Ω to 20 kΩ depending on the load current spanning from 40 μA to 100 mA, the equivalent resistance of the G_m cells loaded at the output becomes about 120 kΩ which is adequately larger than the load resistor and it can be neglected as well. So, the corresponding simplified open-loop three-stage circuit of the proposed regulator is depicted in Fig. 4 where V_{out} is the small-signal output voltage of the LDO regulator and V_{in} is the small-signal input voltage used for AC analysis which has been opened at the output voltage (V_{out}) as shown in Fig. 3. In this case, g_{m1} is the transconductance of the first-stage including G_{mL} (M_{La}, M_{Lb}, M_{BL}) and G_{mH} (M_{Ha}, M_{Hb}, M_{BH}) cells and $M_{1\text{-}4}$ transistors. g_{m2} and g_{m3} are realized as the transconductance of the second-stage made up of $M_{5\text{-}7}$ transistors and additional stage including $M_{8\text{-}12}$ transistors to enhance the slew rate of the M_P, respectively. g_{mp} is the transconductance of the third-stage as the representative of the power transistor. R_1, R_2, and R_L model the output resistances of the first, second, and output stages, respectively. Besides, C_1, C_2, and C_L represent the parasitic capacitances of the first and second stages and the load capacitance of the regulator, respectively.

As long as the multi-stage proposed regulator is mostly suspected of closed-loop instability, the small-signal analysis of the LDO regulator is highly necessitated to be examined. The small-signal sketch of the open-loop structure in Fig. 4 is demonstrated in Fig. 5. The capacitor C_2 is the total parasitic capacitances at the gate of the huge power transistor including the C_{GS} of M_P in addition to the Miller effect of C_{GD} of the power transistor which is ignorable compared to the C_1. Therefore, a Miller compensation capacitor (C_M) far larger than C_{GD} of M_P is located between V_{out} and the output of first stage in order to make the dominant pole at the output node of the first stage. Ultimately, with sufficient gain in the second and third stages and reasonable value for C_M, the poles are split from each other and the dominant pole is located at lower frequency than the poles existed at the output of second stage and the output of the regulator [14–16].

Conclusively, the transfer function is deduced by analyzing the small-signal pattern described in Fig. 5. Indeed, it is attained with assumptions that $C_L \gg C_M$, $C_2 \gg C_1$ and $g_{m1}R_1$, $g_{m2}R_2$, $g_{mp}R_L \gg 1$ [17,18]. Therefore, we have:

$$A_v(s) = A_{dc}\frac{1 + C_M\left(\frac{g_{m3}}{g_{m1}g_{m2}} - \frac{1}{g_{mp}g_{m2}R_2}\right)s - \frac{g_{m3}C_2C_M}{g_{m1}g_{m2}g_{mp}}s^2}{1 + g_{m2}g_{mp}R_1R_2R_LC_Ms + R_2C_2(R_LC_L + R_1C_M)s^2 + R_1R_2R_LC_MC_2C_Ls^3} \tag{1}$$

where A_{dc} is the DC gain of the proposed LDO regulator. The dominant pole ω_{p1} is identifiable easily from equation (1). Hence, the A_{dc} and GBW are given by:

$$\begin{cases} A_{dc} = (g_{m3} + g_{m1}g_{m2}R_1)g_{mp}R_2R_L \\ \omega_{p1} = \dfrac{1}{g_{m2}g_{mp}R_1R_2R_LC_M} \end{cases} \Rightarrow \quad \omega_{GBW} = A_{dc} \times \omega_{p1} = \frac{g_{m1}}{C_M} \tag{2}$$

To obtain the approximate location of the zeros and poles, it should be noted that the location of the poles and zeros change with the output current of the voltage regulator. For more details, from overall transfer function in equation (1), the effect of the load current (g_{mp} and R_L) on the location of poles and zeros can be seen. Thus, stability validation of the regulator is theoretically carried out in two cases of low and high load currents.

2.2.1. Stability over low load currents

Under low load current circumstances, g_{mp} is being small due to operating the power transistor in the weak inversion region. However, it is still larger than g_{m1} and g_{m2} (because of the large size of M_P). Along with, the pole generated at the output of the regulator ($1/C_LR_L$) is moved toward lower frequency owing to the large load resistor. As a consequence, a pair of complex poles is constituted by the pole at the regulator output and the pole at second stage output (gate of power transistor) at the frequency response of the regulator. Intending to approximate the pole-zero places over low load current conditions, the transfer function is given in (3):

$$A_v(s) \approx A_{dc}\frac{\left(1 + \frac{s}{\omega_{z1}}\right)\left(1 + \frac{s}{\omega_{z2}}\right)}{\left(1 + \frac{s}{\omega_{p1}}\right)\left(1 + \frac{s}{Q\omega_0} + \frac{s^2}{{\omega_0}^2}\right)} \tag{3}$$

So that the location of each pole and zero, the resonant frequency, ω_0, and the quality factor, Q, in the small-signal analysis for the proposed LDO regulator can be calculated as follows:

$$\omega_{z1} = +\frac{1}{C_M\left(\frac{g_{m3}}{g_{m1}g_{m2}} - \frac{1}{g_{mp}g_{m2}R_2}\right)}, \quad \omega_{z2} = -\frac{g_{mp}}{C_2}$$

$$Q = (R_LC_L + R_1C_M)\sqrt{\frac{g_{m2}g_{mp}}{C_2C_L}}, \quad \omega_0 = \sqrt{\frac{g_{m2}g_{mp}}{C_2C_L}}$$

$$\omega_{p2,3} = -\frac{\omega_0}{2Q}\left(1 \pm \sqrt{1 - 4Q^2}\right) = \frac{-1}{2(R_LC_L + R_1C_M)}\left(1 \pm \sqrt{1 - 4Q^2}\right) \tag{4}$$

where the right half-plane zero ω_{z2} created by gate-drain capacitor of the power transistor, is always placed at a higher frequency. Another zero ω_{z1} caused by the effect of the Miller capacitor (C_M) that should have placed basically at the right half-plane without g_{m3} existence, can be located at the left half-plane by choosing an appropriate value of g_{m3} $\left(g_{m3} > \frac{g_{m1}}{g_{mp}R_2}\right)$ in order to enhance the phase margin, and hence, to achieve stability at low load currents. Furthermore, two requirements must be met in order to maintain stability at low currents, according to the $\omega_{p2,3}$ formula in (4). One is $Q < 0.5$, which ensures that no imaginary part is created for non-dominant poles, thereby improving the phase margin [19].

$$\frac{4g_{m2}g_{mp}}{C_2C_L}(R_LC_L + R_1C_M)^2 < 1 \quad \Rightarrow \frac{1}{2(R_LC_L + R_1C_M)} > \sqrt{\frac{g_{m2}g_{mp}}{C_2C_L}} = \omega_0 \tag{5}$$

Conclusively, the common part of $\omega_{p2,3}$ poles, $\frac{1}{2(R_LC_L+R_1C_M)}$, is strongly affected by amount of ω_0 with respect to equation (5). Therefore, the other condition for transferring the $\omega_{p2,3}$ poles far enough from GBW and following proper stability is to keep the ω_0 as high as possible above the unity gain-bandwidth frequency. This effectively aims to guarantee that none of $\omega_{p2,3}$ poles can significantly decrease the phase margin (<45°) at low load currents which gives an assumption of at least five times larger than the GBW, i.e.:

$$\omega_0 = \sqrt{\frac{g_{m2}g_{mp}}{C_2C_L}} > 5\frac{g_{m1}}{C_M} \Rightarrow g_{mp} > \frac{25g_{m1}^2}{g_{m2}C_M^2}C_2C_L \tag{6}$$

Then by noticing that the power transistor, M_p, is operating in weak version region due to low load currents, the current flowing through the power transistor is given by $I_{Load} \approx I_{D0}\frac{W}{L}e^{V_{gs}/nV_t}$ which leading to $g_{mp} = \frac{\delta I_{Load}}{\delta V_{gs}} = \frac{I_{Load}}{nV_t}$. On the other hand, the gate capacitance, C_2, of the power transistor can also be estimated by $C_2 \approx C_{Gate.M_p} \approx C_{ox}.W_{M_p}.L_{M_p}$. Inevitably, it is realized that there is still a low limit on load current for maintaining the stability with respect to equation (6) at which the regarded regulator can continue operating, as seen below:

$$I_{Load} > \frac{25nV_tC_{ox}g_{m1}^2}{g_{m2}C_M^2}C_L\left(W_{M_p}.L_{M_p}\right) \tag{7}$$

In general, LDO regulators are suspended often at the edge of instability at very small load currents as calculated precisely in this paper, the minimum possible load current for the desired stability with respect to equation (7). Afterward, the LDO regulator's stability can be maintained for ultra-low currents dominantly by lowering the load capacitance (C_L), which limits its use in some applications, or raising the Miller compensation capacitor (C_M), which leads to a reduced unity gain-bandwidth and larger chip area, or decreasing the size of power transistor, which also reduces the maximum load current leading to lower efficiency.

2.2.2. Stability over high load currents

The power transistor is operated in strong inversion region owing to large amount of the load currents. Therefore, g_{mp} becomes much larger than g_{m1} and g_{m2}. Besides, at this condition, the load resistance is become very small in case with the assumption $R_LC_L \ll R_1C_M$. Therefore, the intended transfer function at high load currents can be simplified as:

$$A_v(s) = A_{dc}\frac{1 + \frac{g_{m3}C_M}{g_{m1}g_{m2}}s - \frac{g_{m3}C_2C_M}{g_{m1}g_{m2}g_{mp}}s^2}{\left(1 + g_{m2}g_{mp}R_1R_2R_LC_Ms\right)\left(1 + \frac{C_2}{g_{m2}g_{mp}R_L}s + \frac{C_2C_L}{g_{m2}g_{mp}}s^2\right)} \tag{8}$$

So that, the location of poles and zeros can be also estimated by the assumption that poles and zeros are split far enough from each other as below:

$$\omega_{z1} = +\frac{g_{m1}g_{m2}}{g_{m3}C_M}, \quad \omega_{z2} = -\frac{g_{mp}}{C_2}$$

$$\omega_{p2} = +\frac{g_{m2}g_{mp}R_L}{C_2}, \quad \omega_{p3} = +\frac{1}{R_LC_L} \tag{9}$$

Such that the $\omega_{p2,3}$ and ω_{z2} are always situated at higher frequencies due to large g_{mp} and small R_L. The only concern for maintaining the stability at higher load currents is to be sure that ω_{z1} is being sufficiently larger than the GBW, which leads to below condition:

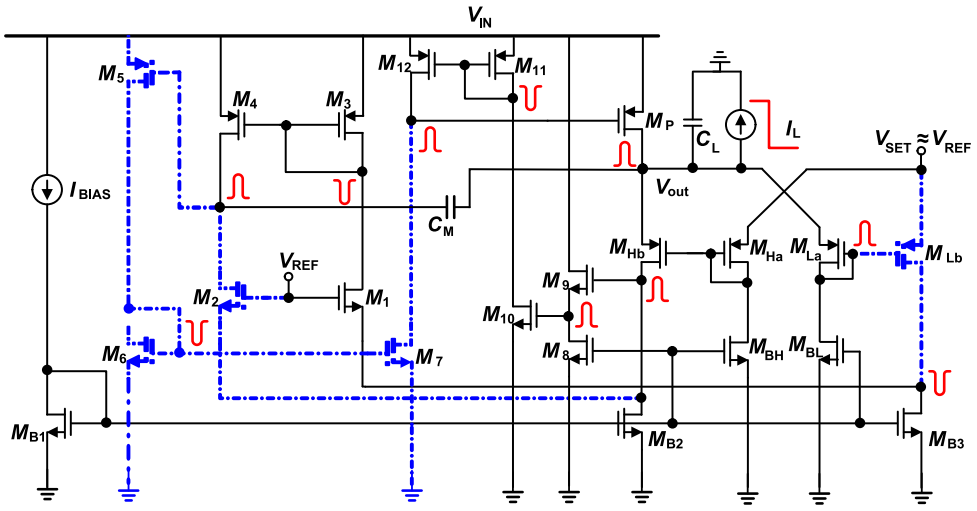

Fig. 6. The large signal behavior of the regulator under falling load current suddenly from high to low.

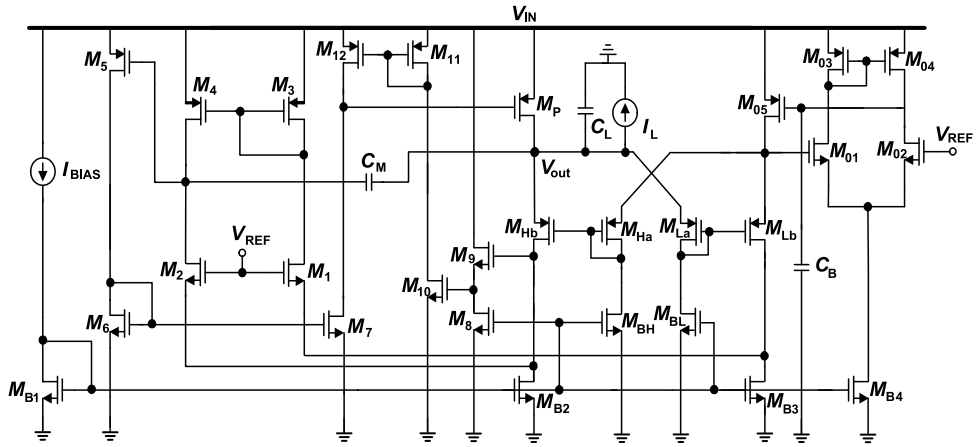

Fig. 7. Overall circuit of the proposed LDO voltage regulator.

$$\omega_{z1} > 2 \times GBW \quad \Rightarrow \quad \frac{g_{m1}g_{m2}}{g_{m3}C_M} > 2\frac{g_{m1}}{C_M} \quad \Rightarrow \quad g_{m3} < \frac{g_{m2}}{2} \tag{10}$$

2.3. Improvement of load transient response

In [9] to reduce the overshoot of the regulator, a voltage spike detection circuit has been employed by using a large on-chip capacitor resulting in large chip area. In this paper, to fasten the load transient response, a new path including $M_{8\text{-}12}$ transistors for passing another current signal to the gate of the power transistor for slew rate enhancement is proposed as shown previously in Fig. 2 and its operation is more described here. Fig. 6 shows the behavior of transistors in the proposed regulator when the load current suddenly changes from high to low with a fall time of 200 ns. During this time, the output voltage will increase rapidly and there will be an overshoot at the output voltage. Since the gate voltage of the M_{Hb} is constant, this overshoot at the output voltage is directly transferred to the source of M_2 and causes all transistors along the dashed blue paths in Fig. 6 from M_2 to the gate of M_P in cut-off region. Consequently, an overshoot also at the gate of M_P is occurred with the purpose of responding to the sudden change at the output voltage in a rapid manner. On the other hand, this sudden overshoot at the output voltage is transferred even faster to the gate of M_P through the current signal line including $M_{8\text{-}12}$ transistors called the slew rate enhancement circuit. While, an overshoot happens at the output voltage, this event is conducted to the gate of M_9 too so that it also is transferred to the gate of M_{10} and eventually leads to a large current in current mirror M_{11} and M_{12} transistors. Afterward, large currents are provided from two paths for charging the gate capacitance of M_P abruptly. Contrarily, when an undershoot at the output voltage is created because of instantaneous change in load current from low to high, the current signal in the paths including $M_{8\text{-}12}$ and $M_{1,3,4}$ transistors is not flowed. Therefore, discharging the parasitic capacitance at the gate of M_P and responding to the rapid overshoot at the output voltage is barely carried out by the path of $M_{2,5\text{-}7}$ transistors. As a conclusion, a reduction in the output overshoot is happened due to exploiting the new path including $M_{8\text{-}12}$ transistors and the slew rate at the gate of M_P is enhanced.

2.4. Circuit level implementation

Fig. 7 demonstrates the complete transistor-level view of the proposed LDO regulator by considering the voltage buffer for driving V_{REF}. It comprises of two common-gate differential input pairs (G_m Cells), a push-pull FVF cell consisting of M_1 to M_4 transistors and a non-inverting gain stage of $M_{5\text{-}7}$ transistors along with slew rate enhancement network including $M_{8\text{-}12}$ transistors to constitute the error amplifier in order to boost the overall loop gain amplifier and develop the transient response of the regulator. The transconductance of the first- and second-stage are

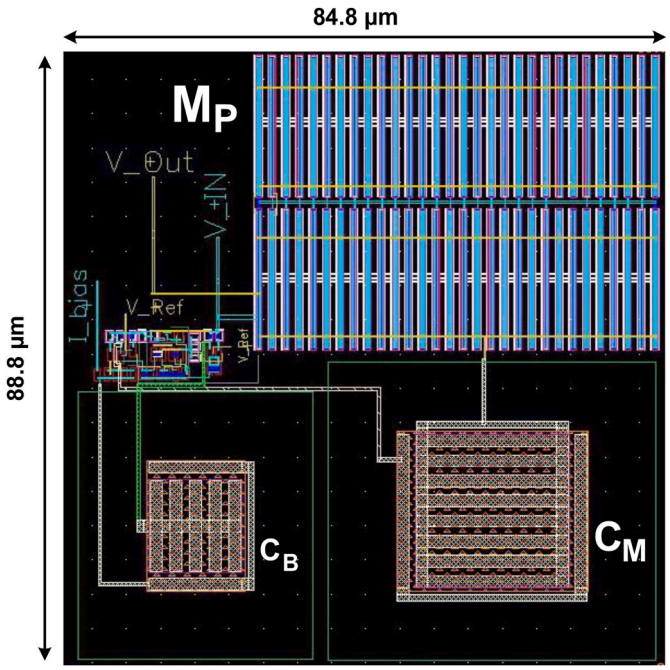

Fig. 8. Layout realization for the proposed LDO regulator.

Table 1
Simulated device parameters.

Parameter	Value	Parameter	Value
$(W/L)_{1,2,6}$	0.15 µm/0.72 µm	$(W/L)_P$	60 × 20 µm/0.1 µm
$(W/L)_{5,11,12}$	0.5 µm/0.72 µm	$(W/L)_{8,9}$	0.15 µm/0.72 µm
$(W/L)_7$	4 × 0.15 µm/0.72 µm	$(W/L)_{10}$	0.3 µm/0.72 µm
$(W/L)_{Ha,La\ Hb,\ Lb}$	0.13 µm/0.9 µm	$(W/L)_{01,02}$	0.13 µm/0.72 µm
$(W/L)_{BH,BL,\ B1}$	0.15 µm/0.72 µm	$(W/L)_{03,04}$	0.5 µm/0.72 µm
$(W/L)_{B2,B3,\ B4}$	2 × 0.15 µm/0.72 µm	C_M, C_B, I_{BIAS}	800 fF, 300 fF, 100 nA

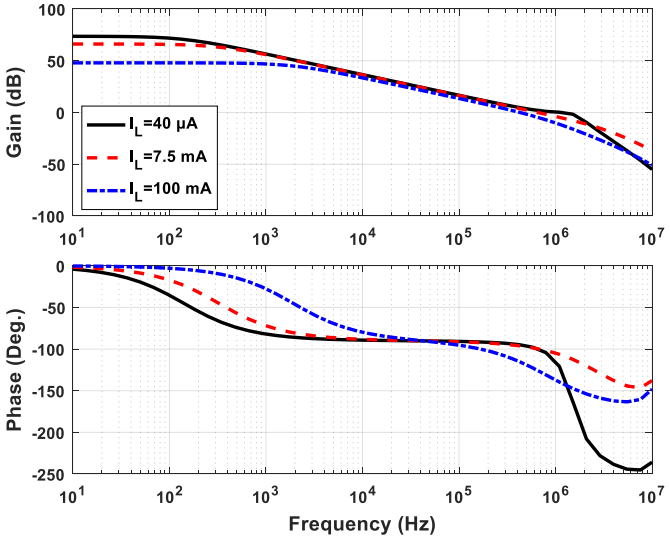

Fig. 9. AC frequency response of the LDO voltage regulator for different load currents at C_L = 100 pF.

determined by $M_{1,2}$ and $M_{5\text{-}7}$ transistors, respectively. In addition, transistors $M_{8\text{-}12}$, which have been utilized to enhance the slew rate at the gate of the power transistor during high to low transition of the load current, form another stage adding some small-signal gain to the LDO

Table 2
Simulated AC frequency characteristics of the LDO voltage regulator at 40 µA load current under process corners and temperature variations.

	FF @-40 °C	TT @27 °C	SS @85 °C
DC Gain (dB)	72.2	74	76
ω_{GBW} (kHz)	820	880	970
Phase Margin (deg.)	52	48	43

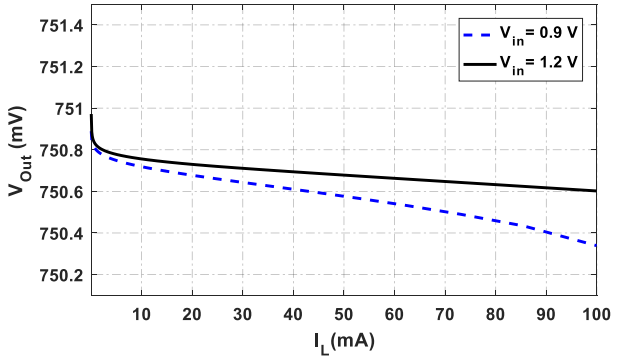

Fig. 10. Simulated load regulation in two different supply voltages from I_{Load} = 40 µA to I_{Load} = 100 mA.

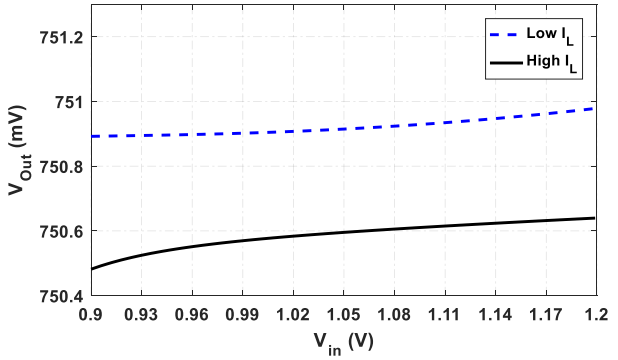

Fig. 11. Line regulation simulation for I_{Load} = 40 µA and I_{Load} = 100 mA.

regulator by the transconductance of g_{m3}. In fact, $M_{8,9}$ transistors have been added to decrease DC gate voltage of M_{10} from $V_{out} - V_{SD,Hb}$ to $V_{out} - V_{SD,Hb} - V_{GS8}$ with the purpose of reducing the power consumption of the regulator. Finally, the $M_{10,11,12}$ transistors mirror the signal of this stage to gate of the power transistor. The power MOS transistor, M_P, with the aspect ratio of W/L = 1200 µm/0.1 µm has been used as the third-stage to provide maximum 100 mA load current.

Transistors $M_{01\text{-}04}$ realize the reference voltage buffer to generate control voltage and create a fixed gate voltage under small load resistance of $M_{Ha,Lb}$ ($1/g_{mHa,Lb}$). The capacitor C_B has considered for assuring the stability of the reference voltage buffer circuit. $M_{B1\text{-}4,BH,BL}$ transistors provide current sources for the LDO regulator through I_{BIAS}. C_M is the Miller compensation capacitor. C_L and I_L model the lumped parasitic capacitances at the output node and load current of the regulator, respectively. To take advantage of operating the regulator at very no-load current and progressively ensuring fast transient response and high gain characteristics for the error amplifier, the channel length of all transistors except M_P are tailored to be at least five times as much as the minimum channel feature size of the 90 nm technology.

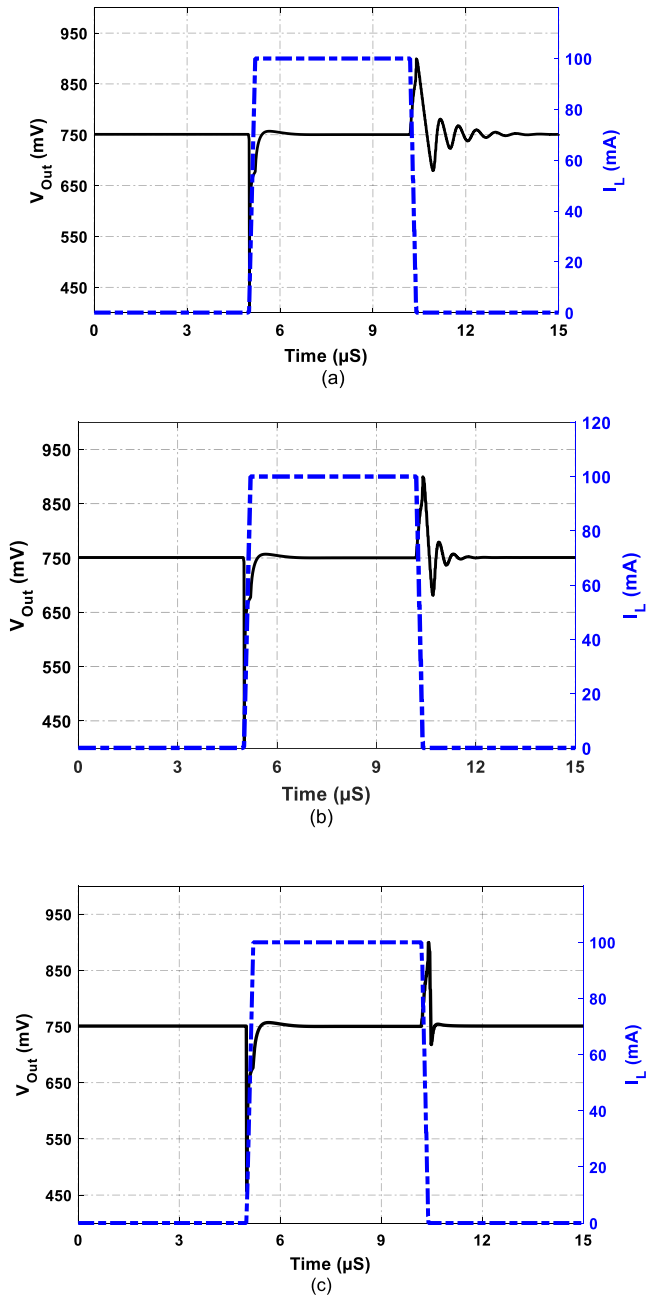

Fig. 12. Load transient response simulation result at $V_{out} = 0.75$ V and $V_{in} = 0.9$ V for three different load capacitance (a) $C_L = 100$ pF, (b) $C_L = 40$ pF and (c) $C_L = 1$ pF.

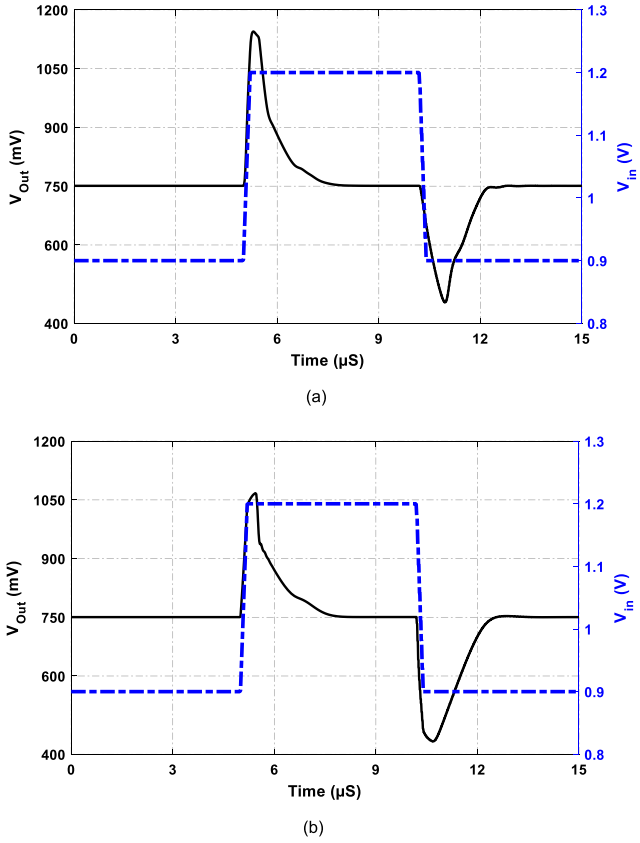

Fig. 13. Line transient response simulation result at $V_{out} = 0.75$ V, $C_L = 100$ pF and: (a) $I_{Load} = 40$ μA, (b) $I_{Load} = 100$ mA.

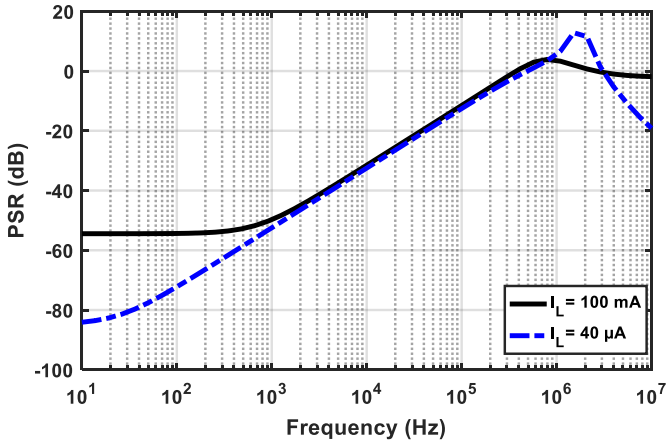

Fig. 14. PSR simulation result of the proposed LDO regulator at $C_L = 100$ pF.

3. Post-layout simulation results

Validation of the proposed LDO voltage regulator is realized by simulation-based analysis in TSMC 90 nm CMOS technology. Correspondingly, its layout drawing is demonstrated in Fig. 8 where the whole chip area is 84.8 × 88.8 μm^2 including compensation capacitors C_M and C_B totally 1.1 pF. The LDO regulator output is 750 mV over an input voltage range from 0.9 V to 1.2 V under achieving maximum 100 mA load current. It consumes 1.74 μA quiescent current at minimum load current possibility of 40 μA. For modeling the load capacitor C_L in the simulations, an on-chip capacitor of 100 pF is presumed at the output of the LDO regulator. Table 1 indicates the exact size of each transistor and capacitor used in the proposed LDO regulator. As observed, aiming to grasp as lower quiescent current as possible, the channel length of all transistors has been regarded to be larger than the power transistor.

AC response of the proposed LDO regulator is exhibited in Fig. 9 by opening the output node as stated in Fig. 3 under different load currents with C_L = 100 pF. The regulator stability is maintained by Miller compensation technique. The desired phase margin of 48° and DC gain of 74 dB are obtained in 40 μA lowest load current. By increasing the load current to 100 mA, a loop gain of 50 dB with a phase margin of 75° is achieved. For an accurate AC response analysis, loop gain and phase margin characteristics over process and temperature variations are listed in Table 2 at 40 μA lowest load current. As shown in Table 2, the proposed LDO regulator has less sensitivity to the process, voltage and

Table 3
Performance summary of the proposed LDO voltage regulator and comparison with several state-of-art LDO regulators.

Parameter	JSSC′10 [9]	TCAS-II′20 [12]	CSSP′21 [13] [a]	MEJ′20 [23]	AICSP′18 [25]	TVLSI′20 [27]	TCAS-I′18 [28]	AICSP′19 [30] [a]	TPEL′19 [31]	MEJ′21 [32] [a]	This work[a]
Tech. (nm)	90	65	90	180	180	40	65	180	65	130	**90**
$I_{L,Max}$ (mA)	100	10	40	50	50	100	25	100	50	50	**100**
V_{DO} (mV)	200	250	150	200	200	200	200	200	200	200	**150**
I_Q (μA)	8	49.4	1.83	95	1.8	23.7	1.6	43	50	95	**1.74**
$C_{on\text{-}Chip}$ (pF)	7	16	0.49	0.3	0	1.56	0.6	5	0.5	NA	**1.1**
C_L range (F)	0–50p	10n–470p	0–100p	0–100p	0–100p	0–100p	0–25p	0–100p	0-2n	0-2n	**0–100p**
LNR (mV/V)	3.78	4	1	11	8.5	5.6	0.7	0.24	1	5	**0.4**
LDR (μV/mA)	100	140	36	508	550	12.5	280.5	1.76	40	9	**6**
PSR (dB) @1 kHz	−44	−37	−43	−31	−51	−48	−49	−58.8	−45	−43	**−51**
ΔV_{Out} (mV)	114	41.6	320	133	35.7	23.7	37	130	80	390	**350**
T_R (μs)	>2.2	0.38	0.85	2.41	0.75	0.414	3.6	0.77	~1	0.2	**1.2**
Edge Time (μs)	0.1	0.0002	0.2	0.05	0.3	0.2	0.1	0.3	0.002	0.0001	**0.2**
Edge Time Ratio (K)	1000	2	2000	500	3000	2000	1000	3000	20	1	**2000**
FoM_1 (mV)	9	0.42	15.2	126.4	9.2	11.2	2.4	166	1.6	0.74	**12.2**
FoM_2 (ps)	176	1880	38.9	4579	27	98	230	331	1000	38	**20.9**

[a] Simulation results, LNR: Line regulation, LDR: Load regulation.

temperature (PVT) variations.

Fig. 10 depicts the simulated load regulation when the load current is switched from 40 μA to 100 mA with 200 ns rise-/fall time. The load regulation values for two input voltages $V_{IN} = 0.9$ V and 1.2 V are 6 μV/mA and 4 μV/mA, respectively. The line regulation is demonstrated in Fig. 11 when V_{IN} is changed from 0.9 V to 1.2 V for two modes of low and high load currents. The determined line regulation values over applying two different load currents, $I_L = 40$ μA and $I_L = 100$ mA, are 0.33 mV/V and 0.4 mV/V, respectively.

Evaluation of transient performance of the proposed LDO voltage regulator is verified by simulation at large-signal model through load-/line transient response. For output transient response characterization, the load current steps from 40 μA to 100 mA with 200 ns rise and fall times. The load transient response under different capacitive loads of 100 pF, 40 pF and 1 pF regarding to the output voltage of 750 mV is shown in Fig. 12. As can be seen in Fig. 12(a), the regulator is pushed quickly into the instability boundary by rapidly decreasing the load current to the lowest load current (40 μA minimum acceptable load current for our design in CL = 100 pF to maintain the stability), potentially cause some ringing during transient simulation of the regulator. Furthermore, according to the explanations presented in section 2.2.1 and equation (8), transient simulation results in Fig. 12(b and c) have already demonstrated that by dropping the load capacitance from 100 pF to 40 pF and even 1 pF, the lowest permitted load current is moved to lower values, and therefore, 40 μA load current is no longer on the border of instability, conclusively causing significant stability. Moreover, by reducing the load capacitor and going the output pole to higher frequencies, the slew rate enhancement circuit also reacts more rapidly to the extreme change at the output voltage. In this simulation, the undershoot and overshoot over the output voltage are obtained 320 mV and 150 mV, respectively, with input voltage of 0.9 V and $C_L = 100$ pF. Correspondingly, a 0.5 μs recovery time is reached under these circumstances.

The simulation results of line transient response have been presented in Fig. 13 with an input voltage switching between 0.9 V and 1.2 V and 200 ns rise-/fall time. The result proves that the maximum output voltage overshoot is less than 350 mV. Power supply rejection simulation results for the LDO regulator are specified in Fig. 14 at the presence of 100 pF load capacitance and two load currents of 40 μA and 100 mA. According to Fig. 14, the resulting PSR is −53 dB and −13.4 dB for a 40 μA load current at 1 kHz and 100 kHz, respectively. With 100 mA load current, the simulated PSR of the proposed regulator is −51 dB and −12.3 dB at 1 kHz and 100 kHz, respectively.

In Table 3, a comparison between the performance of this work and some previously published LDO voltage regulators is summarized. The following popular figure-of-merits (FoMs) given in Refs. [9,20–22,24,26,29] are employed to compare the proposed LDO regulator with other LDO regulator structures.

$$FOM_1 = K\frac{\Delta V_{out} I_Q}{\Delta I_{Load}} \tag{11}$$

$$FOM_2 = \frac{T_R I_Q}{I_{L,Max}} \tag{12}$$

where respectively K is the edge time which is defined by $K = \frac{\Delta t \text{ used in the measurment}}{The \text{ smallest } \Delta t \text{ among comparison designs}}$ and the transient response time T_R is an average settling time of the LDO regulator responded to the overshoot and undershoot of output voltage under load-/line transient responses. A lower value of this FoMs represents a better transient performance in which it can work with a small quiescent current. As shown in Table 3, the proposed LDO regulator has a remarkable FoM by providing the best transient response and regulation. It is noteworthy that the proposed regulator consumes only 1.74 μA quiescent current. Its power consumption is only 2.1 μW making it suitable for low-power low voltage applications.

4. Conclusions

A low-power LDO voltage regulator based on a push-pull FVF cell with slew rate enhancement at the gate of the power transistor is reported in this paper. The open-loop gain of the regulator is increased by using a three-stage structure including two symmetric paths of current signal to the gate of power transistor unlike other previously reported architectures based on FVF concept aiming to improve the PSR and line and load regulations. The load transient characteristic of the regulator is also developed by employing a push-pull FVF concept and adding another new path between the output of the regulator and the gate of power transistor to enhance slew rate at the gate of power transistor beneficially. Stability requirements for the proposed LDO regulator is fulfilled over a wide load current range from 40 μA to 100 mA at the presence of 100 pF load capacitance. Furthermore, a quiescent current of 1.74 μA is introduced with a dropout voltage of 150 mV for 0.9–1.2 V input voltage. Verification of the proposed LDO regulator is further manifested by post-layout simulations in a 90 nm CMOS process. Afterward, due to ultra-low power consumption and high efficiency of the regulator, it can be well suited in low voltage applications.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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