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A Low-Power High-Gain Low-Dropout Regulator for Implantable Biomedical Applications

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Abstract

This paper presents an ultra-low-power and high-gain low-dropout (LDO) regulator. It is based on the flipped voltage follower cell with an adaptive biasing technique that is suitable for implantable biomedical applications. The error amplifier for the proposed regulator consists of two cross-coupled common-gate cells and a pseudo-folded-cascode structure to increase the regulator's loop gain. In addition, three different compensation techniques including Miller, cascode, and Q-reduction are simultaneously utilized at the LDO regulator to achieve high stability despite having the minimum load current and ultra-low power consumption. The proposed LDO regulator has been simulated in TSMC 90-nm CMOS technology with minimum power consumption of 2.8 μW at no load. Post-layout simulation results show that the proposed LDO regulator is stable over load currents from 30 μA to 40 mA with a maximum on-chip C_L of 100 pF. Moreover, the voltage regulator settles in less than 850 ns at 0.75 V output voltage that is achieved in response to a load transient step of 40 mA with a rise time of 200 ns. Besides, the obtained line and load regulations are significantly improved to 1 mV/V and 36 μV/mA, respectively.

Keywords Low-dropout (LDO) regulator · Adaptive biasing · Pseudo-folded-cascode structure · Transient response · Power consumption · Implantable biomedical devices

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1 Introduction

Low-dropout (LDO) regulators are one of the important parts of power management systems in radio frequency identification tags and implantable biomedical devices [22, 25, 26], where the supplied energy to these systems should be severely restricted. In addition, the active silicon area of the LDO regulators comprising the transistors and compensation capacitors must be as small as possible. In implantable biomedical applications, voltage regulators should consume ultra-low quiescent current to have longer LDO regulator battery lifetime, low dropout voltage, small chip area, high power supply rejection (PSR), and stable operation at low load currents [18, 19, 24]. Moreover, fast line and load transient responses at the output of the voltage regulator are also extremely important.

As yet, several LDO regulators have been reported in [4, 9, 10, 13, 14, 20, 16, 17]. In [9], the regulator combines the single-stage load regulation with replica biasing. It achieves optimum load regulation and a very fast time response with a high quiescent current of 6 mA, which is not suitable for low-power applications. The LDO regulator in [20], by using two flipped voltage follower (FVF) structures and a push–pull output stage at the error amplifier, improves the transient response by a very low quiescent current of 1.2 µA. This regulator also suffers from a poor loop stability at low load currents and small loop gain. In [4], the error amplifier of the regulator is based on the structure in [20]. However, the settling time of the regulator output voltage is about 6 µs which is too long when the load current changes from 1 to 100 mA although the fall and rise times for line and load transient responses have been considered a large amount of 1 µs.

In [14], a telescopic-cascode output structure is utilized at the output stage of the regulator instead of the push–pull amplifier to improve the loop gain of the architecture presented in [20]. In addition, a dual-path active-feedback frequency compensation scheme is exploited to enhance both the stability and gain bandwidth (GBW) of the LDO regulator. Consequently, there is no restriction in the load current requirement in the operation of the LDO regulator at very low load currents and the transient response is simultaneously improved. However, rather large on-chip capacitors (totally 6 pF) are used for frequency compensation as well as consuming a relatively large quiescent current of 14 µA. On the other hand, the obtained line and load regulations have not been improved significantly. In the regulator presented in [10], the bias current of the regulator increases rapidly by a dynamic bias boosting technique when the output voltage changes suddenly. As a result, it exhibits a faster settling time and an extremely lower quiescent current. Higher undershoot and lower loop gain are the main disadvantages of this structure. A fast transient regulator has been demonstrated in [13]. It is based on a dual dynamic-load composite gain stage for FVF topology to have a reasonable high gain and improved line and load regulations. It also consumes a quiescent current about 50 µA in no-load condition. Therefore, it is very challenging to design an ultra-low-power and fast transient response output capacitor-less low-dropout (OCL-LDO) regulator with high loop gain.

To overcome the challenges of previous methods, an ultra-low-quiescent-current three-stage LDO regulator with a fast transient response is proposed in this

paper by using the concept of FVF structure. However, by adding an extra stage to the error amplifier, the regulator benefits from high gain, improved line and load regulations, and enhanced PSR. In order to achieve the stability of the LDO regulator, a compensation network including three different compensation techniques is proposed despite consuming almost the same quiescent current as the one in [20]. In addition, for gain bandwidth improvement, an adaptive biasing technique is utilized.

The rest of the paper is organized as follows. In Sect. 2, the structure of the proposed LDO regulator and its analysis are presented. Section 3 describes the circuit level implementation of the proposed LDO regulator. The simulation results, discussions, and performance comparison with several other recent LDO regulators are provided in Sect. 4. Finally, the conclusions are given in Sect. 5.

2 Proposed LDO Regulator

In this section, the structure and analysis of the proposed three-stage LDO regulator are presented.

2.1 Proposed LDO Regulator Architecture

Figure 1 shows the conceptual architecture of the proposed three-stage LDO regulator without the compensation network which is originated from the LDO regulator structure presented in [20]. It consists of two differential common-gate transconductance cells (G_{mH}, G_{mL}), an additional gain stage (A_{ex}), a current summation circuit to add currents of two parallel paths, a power transistor M_P, and the load capacitor C_L. V_{out}, V_{IN}, and V_{REF} are the output, input, and reference voltages, respectively. Since most of the voltage references do not have the output current-driving capability, the buffer stage is added after the reference voltage. In comparison with the structure in [20], an additional gain of A_{ex} is added to the error amplifier to boost

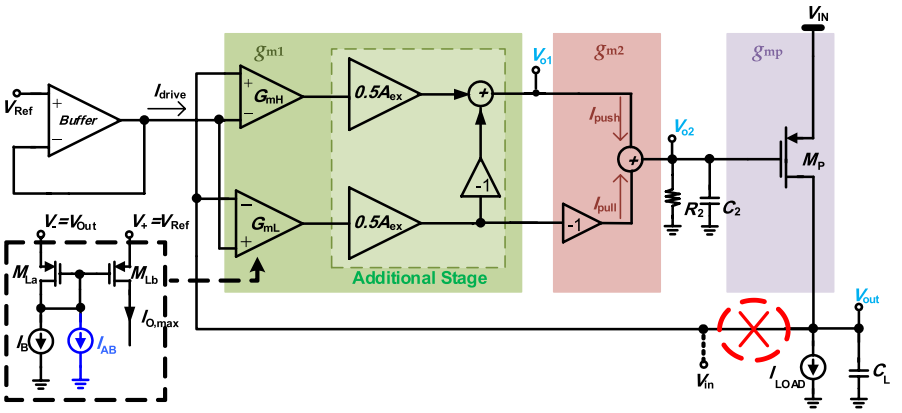

Fig. 1 Conceptual architecture of the proposed LDO regulator

the loop gain and hence to improve both line and load regulations despite dissipating approximately the same static power as the structure in [20]. The two G_m cells, including G_{mL} and G_{mH} which are in the form of a current mirror (M_{La}, M_{Lb}, and I_B), constitute a push–pull stage. By these two cells and assistance of A_{ex} and the current summation circuit, an extra current is provided for charging and discharging of the capacitor C_2. The maximum output current, $I_{O,max}$, is no longer limited by the constant current source, I_B (as in the case of a conventional amplifier with a tail current source). This current is increased due to the difference between V_- and V_+. As it is seen, when V_- is decreased, $I_{O,max}$ is increased, while the source voltage of M_{Lb} is fixed [20]. Besides, in order to achieve an ultra-low quiescent current and improve the gain bandwidth of the regulator, the adaptive biasing technique [8, 17] formed by I_{AB} is added to the first gain stage. The adaptive biasing technique is achieved by making the biasing current proportional to the current in power transistor that is explained more in the following.

2.2 Stability Analysis

The LDO regulator in [20] is composed of only two stages in the open-loop structure, and the output impedance of the regulator is modified to the small quantities due to the small input impedance of the common-gate differential input Gm cells. In [20], the stability is always achieved without needing any compensation scheme. In this paper, an extra stage is added to the error amplifier part of the LDO regulator to boost the loop gain. Therefore, a precise frequency compensation technique is required to ensure the stability of the regulator. The proposed compensation network for the three-stage LDO regulator in an open-loop block diagram is shown in Fig. 2. V_{in} is the input voltage of G_{mL} and G_{mH} cells in Fig. 1

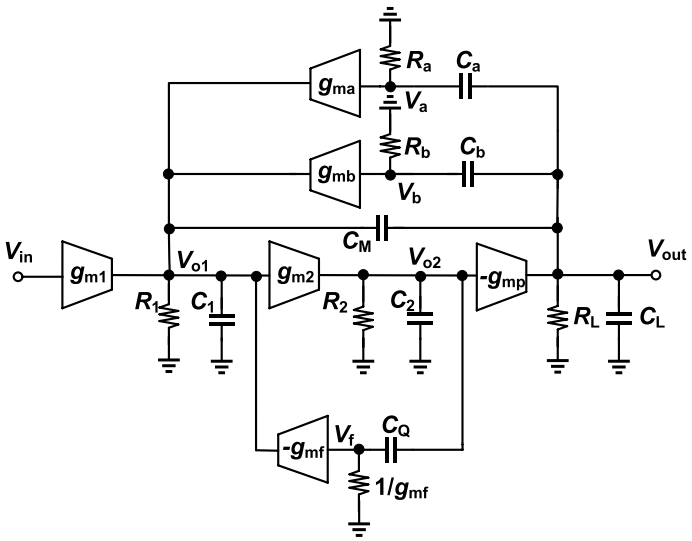

Fig. 2 Open-loop block diagram of the proposed three-stage LDO regulator

which should be opened for stability analysis at the output node (V_{out}). It is worth mentioning that in the small-signal analysis of the loop gain, a resistance equivalent to $\left(\frac{1}{g_{m,La}} || \frac{1}{g_{m,Hb}}\right) = \frac{1}{g_{m,La}+g_{m,Hb}}$ is placed in parallel with the load impedance at the output node when the feedback loop is broken where $g_{m,La}$ and $g_{m,Hb}$ are the transconductance of M_{La} and M_{Hb} transistors in G_{mL} and G_{mH} cells, respectively. Since the current of these transistors is about 100 nA, the equivalent resistance becomes about 120 kΩ. On the other hand, the load resistor is changed from 18 Ω to 30 kΩ owing to the load current range of 30 µA to 40 mA. Therefore, in the small-signal analysis of the loop gain, the loading effect of the G_m cells at the output of the regulator can be neglected as well.

In Fig. 2, g_{m1} is the transconductance of the first stage, and according to Fig. 1, it includes G_{mL} and G_{mH} cells, and the additional stage of A_{ex}. g_{m2} is considered as the transconductance of the second stage including the current summation circuit in Fig. 1 and g_{mp} is the transconductance of the third stage as the representative of the power transistor. R_1, R_2, and R_L are the output resistances of the first, second, and third (output) stages, respectively. Also, C_1 and C_2 depict the parasitic capacitances at the output of the first and second stages, respectively, and C_L is the load capacitance.

The stability of the proposed LDO regulator is achieved by three different compensation techniques including Miller, cascode, and Q-reduction. With the Miller compensation capacitor (C_M), the poles are split and the dominant pole is placed at very low frequency and it is not at the output of the regulator. The parasitic pole at the output is located at high frequencies. By using two current buffers and two cascode compensation capacitors (C_a and C_b), a left half-plane zero is created to reduce the effect of non-dominant poles and hence to improve the stability and power supply rejection (PSR) of the regulator [29]. g_{ma} and g_{mb} represent the transconductance, and R_a and R_b are the input resistance of the current buffers. These two current feedback paths are chosen to be the same which yields to $C_a = C_b$, $R_a = R_b = 1/g_{ma} = 1/g_{mb}$ [21, 28, 29]. In addition, these two capacitors affect the dominate pole and split it further from other non-dominate poles. The Q-reduction capacitor (C_Q) and the g_{mf} current buffer with the input resistance of $R_{mf} = 1/g_{mf}$ reduce both the on-chip capacitance and the minimum output current requirement [12]. One of the reasons for using three compensation capacitors instead of a single Miller capacitor is that the proposed regulator is not stable with only the Miller compensation capacitor at low load current. According to the simulation results and the results from the regulator in [7, 20], the minimum load current for stability of this regulator is about 1 mA when only the Miller capacitor with a value of 0.8 pF is used. However, by using the proposed compensation technique, it is reduced to about 30 µA while the total value of the compensation capacitors is about 0.5 pF.

The overall open-loop transfer function of the proposed LDO regulator is derived by the analysis of the small-signal model shown in Fig. 3. Like the analysis of multistage amplifiers in [5, 6], it is assumed that $C_L \gg C_Q$, C_M, C_a, C_b, $C_2 \gg C_1$, and $g_{m1}R_1$, $g_{m2}R_2$, $g_{mp}R_L \gg 1$. Hence, the overall open-loop transfer function is obtained as follows:

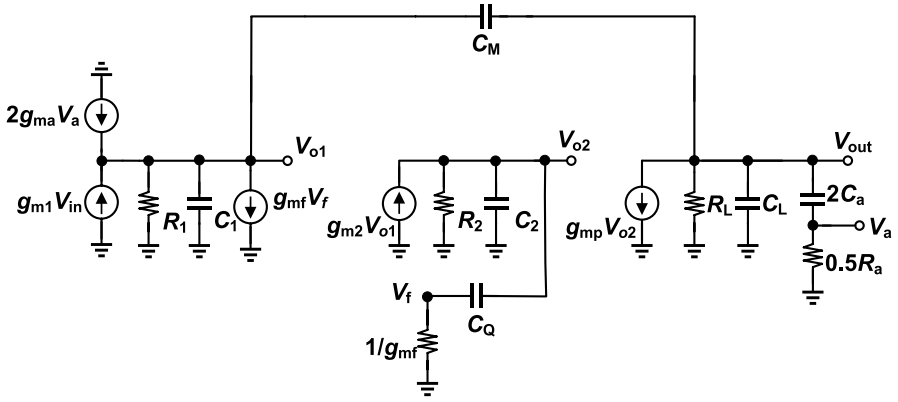

Fig. 3 Small-signal model of the proposed LDO regulator

$$A_v(s) = A_{dc} \times \frac{\left(1+\left(\frac{C_a}{g_{ma}}+\frac{C_Q}{g_{mf}}\right)s\right)\left(1-\frac{C_M}{g_{mp}}s\right)\left(1+\frac{C_2}{g_{m2}}s\right)}{\left(1+\frac{s}{\omega_{p1}}\right)\left(1+\left(\frac{C_Q C_L}{(2C_a+C_M)g_{mp}}\right)s+\frac{C_2 C_M C_L}{(2C_a+C_M)g_{m2}g_{mp}}s^2+\frac{C_2 C_M C_L (C_a g_{mf}+C_Q g_{ma})}{(2C_a+C_M)g_{m2}g_{mp}g_{ma}g_{mf}}s^3\right)} \tag{1}$$

where A_{dc} is the dc gain. ω_{p1} and ω_{GBW} are the dominant pole and the gain bandwidth (GBW), respectively. They are given by:

$$\begin{cases} A_{dc} = g_{m1}g_{m2}g_{mp}R_1R_2R_L \\ \omega_{p1} = \dfrac{1}{g_{m2}g_{mp}R_1R_2R_L(2C_a+C_M)} \end{cases} \Rightarrow \omega_{GBW} \approx A_{dc} \times \omega_{p1} = \frac{g_{m1}}{2C_a+C_M} \tag{2}$$

Since the output current of a voltage regulator is variable, its stability should be examined at different load conditions mainly owing to the changes in g_{mp}. Here, the stability of the proposed LDO regulator is examined in two different conditions.

2.2.1 Stability at Small Load Currents

In this case, the power transistor is in the weak inversion and the g_{mp} is small, but it is still larger than g_{m1} and g_{m2} (due to the large size of M_P). Therefore, a pair of complex poles is constituted in the frequency response of the regulator. To estimate the pole-zero locations at small load currents, the transfer function is obtained as:

$$A_v(s) \approx A_{dc}\frac{\left(1+\frac{s}{\omega_{z1}}\right)\left(1+\frac{s}{\omega_{z2}}\right)\left(1+\frac{s}{\omega_{z3}}\right)}{\left(1+\frac{s}{\omega_{p1}}\right)\left(1+\frac{s}{Q\omega_0}+\frac{s^2}{\omega_0^2}\right)\left(1+\frac{s}{\omega_{p4}}\right)} \tag{3}$$

By decomposing the denominator of relation (1) in the form of (3), the poles, zeros and the corresponding resonant frequency, ω_0, and the quality factor, Q, are given by:

$$\omega_{z1}=\frac{1}{\frac{C_a}{g_{ma}}+\frac{C_Q}{g_{mf}}},\ \omega_{z2}=\frac{g_{m2}}{C_2},\ \omega_{z3}=-\frac{g_{mp}}{C_M},\ \omega_{p4}\approx\frac{1}{\frac{C_a}{g_{ma}}+\frac{C_Q}{g_{mf}}}$$
$$\omega_0=\sqrt{\frac{(2C_a+C_M)g_{m2}g_{mp}}{C_2C_MC_L}},\ Q=\sqrt{\frac{(2C_a+C_M)C_2C_Mg_{mp}}{g_{m2}C_LC_Q^2}} \tag{4}$$

As it is clear from the relation (4), the right half-plane zero ω_{z3} is placed at a higher frequency. The pole ω_{p4} is almost cancelled with the zero ω_{z1}, and only two complex poles affect the stability of the regulator at small load currents.

$$\omega_{p2,3}=\frac{g_{m2}C_Q}{2C_2C_M}\pm\frac{1}{2}\sqrt{\left(\frac{g_{m2}C_Q}{C_2C_M}\right)^2-4\frac{g_{m2}g_{mp}(2C_a+C_M)}{C_2C_MC_L}}$$
$$\Rightarrow\omega_{p2,3}=\frac{g_{m2}C_Q}{2C_2C_M}\pm\frac{g_{m2}C_Q}{2C_2C_M}\sqrt{1-4Q^2}=\frac{g_{m2}C_Q}{2C_2C_M}\left(1\pm\sqrt{1-4Q^2}\right) \tag{5}$$

The Q-reduction capacitor, C_Q, affects Q and location of complex poles. According to the relation (5), a large C_Q can improve the phase margin of the proposed LDO regulator at light load currents by increasing the value of real part of complex poles and moving them to higher frequencies. On the other hand, an appropriate value of C_Q can be chosen providing by this condition. If $Q<0.5$ is achieved, then not only the stability of the regulator would be increased but also the time response of the regulator would be improved by decreasing the overshoot of the output signal at small load currents [12]. Therefore, the stability of the proposed LDO regulator at small load currents can be achieved by considering a reasonable value for capacitor C_Q as:

$$C_Q^2>\frac{4(2C_a+C_M)C_2C_Mg_{mp}}{g_{m2}C_L}\Rightarrow C_Q>2\sqrt{\frac{(2C_a+C_M)C_2C_Mg_{mp}}{g_{m2}C_L}} \tag{6}$$

Accordingly, the minimum value of C_Q should be considered regarding to the above condition.

The other condition for stability at small load currents is that the resonance frequency, ω_0, should be at least twice as large as the GBW [7]. This condition results in:

$$\sqrt{\frac{(2C_a+C_M)g_{m2}g_{mp}}{C_2C_MC_L}}>\frac{5g_{m1}}{(C_M+2C_a)}\overset{C_M\approx 2C_a}{\rightarrow}g_{mp}>\frac{25g_{m1}^2C_2C_L}{8g_{m2}C_M^2} \tag{7}$$

By knowing $g_{mp}=\sqrt{2\mu_pC_{ox}(W/L)\left(1+\lambda(V_{IN}-V_{out})\right)I_{Load}}$ and the stability condition of the regulator, the minimum required load current is obtained as follows:

$$I_{\text{Load}} > \frac{625 g_{m1}^4 C_2^2 C_{\text{L}}^2}{32 \mu_p C_{\text{ox}} (W/L)\big(1+\lambda(V_{\text{IN}}-V_{\text{out}})\big) g_{m2}^2 C_{\text{M}}^4} \Rightarrow I_{\text{Load,Minimum}} \propto k C_{\text{L,Maximum}}^2 \tag{8}$$

According to the relation (8), the minimum required load current is measured and it is proportional to the load capacitance. So the LDO regulator can be worked for even lower load currents (less than 30 μA for this work) while using smaller load capacitance at the output of the regulator.

2.2.2 Stability at Large Load Currents

In this case, the load current is large and the power transistor is biased in the strong inversion. So, g_{mp} is much larger than g_{m1} and g_{m2}. At this condition, the second-order function at the denominator of (1) has two real poles, and it is simplified as:

$$A_{\text{v}}(s) \approx A_{\text{dc}} \frac{\left(1+\frac{s}{\omega_{z1}}\right)\left(1+\frac{s}{\omega_{z2}}\right)\left(1+\frac{s}{\omega_{z3}}\right)}{\left(1+\frac{s}{\omega_{p1}}\right)\left(1+\frac{s}{\omega_{p2}}\right)\left(1+\frac{s}{\omega_{p3}}\right)\left(1+\frac{s}{\omega_{p4}}\right)} \tag{9}$$

where the value of the poles and zeros is given by:

$$\begin{aligned} &\omega_{z1} = \frac{1}{\frac{C_{\text{a}}}{g_{\text{ma}}} + \frac{C_{\text{Q}}}{g_{\text{mf}}}}, \quad \omega_{z2} = \frac{g_{m2}}{C_2}, \quad \omega_{z3} = -\frac{g_{\text{mp}}}{C_{\text{M}}} \\ &\omega_{p3} = \frac{g_{m2}}{C_{\text{M}}}, \quad \omega_{p2} = \frac{(2C_{\text{a}} + C_{\text{M}}) g_{\text{mp}}}{C_{\text{Q}} C_{\text{L}}}, \quad \omega_{p4} \approx \frac{1}{\frac{Ca}{g_{\text{ma}}} + \frac{C_{\text{Q}}}{g_{\text{mf}}}} \end{aligned} \tag{10}$$

In this case, ω_{z3} is still placed at a higher frequency and ω_{z1} and ω_{p4} cancel each other. Therefore, in this case, we almost have one dominant pole, one non-dominant pole, and a right half-plane zero that is located at high frequencies. Owing to the large value of g_{mp}, the stability of the regulator is easily achieved at large load currents.

3 Circuit Level Implementation

Figure 4 shows the circuit realization of the proposed LDO regulator where the overall loop gain amplifier is implemented by a pseudo-folded-cascode structure with a common-gate differential input pair and consists of M_1–M_{10} transistors. The transconductance of the first stage in the error amplifier (g_{m1}) is determined by transistors in the G_{mL} and G_{mH} cells and M_1–M_2 transistors. The second stage is realized by transistors M_{11}–M_{14}. Transistors M_{11} and M_{12} make two parallel paths to form the push–pull output stage as the current summation part of the circuit, and it is plotted in Figs. 1 and 2 as a part of G_{m2}. In addition, these two transistors enable the proposed amplifier with large output voltage swing at the

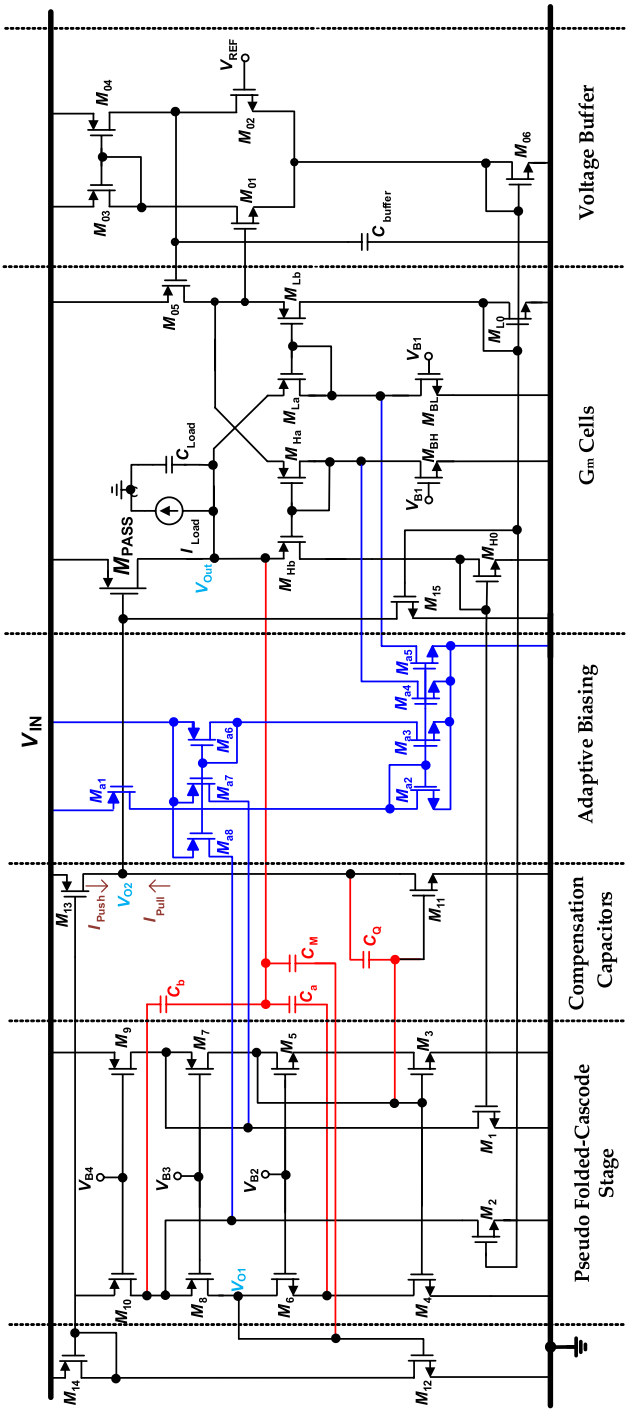

Fig. 4 Circuit level realization of the proposed LDO regulator without the biasing circuit

gate of the power transistor. A large power PMOS transistor (M_P) with a transconductance of g_{mp} is used in the third stage. All these transistors except M_P always operate in the strong inversion region.

The quiescent current is defined as the leakage current of the whole circuit at the lowest load current (30 µA in this work) which has been fixed to 1.83 µA in this work. Since this small quiescent current deteriorates the performance at higher load current, an adaptive biasing circuit is introduced to increase the bias current of the regulator with direct relation to the load current. As a result, much more leakage current for the circuit is dissipated when the load current is increased. However, the adaptive biasing network comprised of M_{a1}–M_{a8} transistors is biased in the weak inversion region like the transistor of M_P at small load currents so that no additional current (I_{AB}) is not summed with the bias current. As long as the load current is increased, a specified current with a proportion of the load current is transferred to the G_{mL} and G_{mH} cells by M_{a1}–M_{a8} transistors and the bias current rises, leading to the large g_{m1} for the error amplifier. As a result, the GBW of the LDO regulator ($g_{m1}/(2C_a + C_M)$) is also improved at large load currents. Due to using two G_m cells before the error amplifier and two parallel paths inside the error amplifier, the slew rate of the regulator at the gate of the power transistor is being symmetrical and improved. A push–pull output stage with the assistance of G_m cells can provide more current at the output of the error amplifier to charge and/or discharge the gate of the power transistor during the instantaneous transient. It is worth mentioning that M_{a7} and M_{a8} transistors can also be directly mirrored from M_{a1} transistor. In this case, the adaptive biasing circuit is simplified.

The transistor M_{15} is designed to be off in the steady state of the circuit. When V_{out} increases due to the rapid decrease in the load current, this sudden change is transferred to the gate of M_{15} and makes a new path to the gate of M_P to discharge. Consequently, M_{15} provides more discharging current for the gate capacitance of the power transistor and enhances the slewing at the gate of the power MOSFET.

Because of the small input impedance of the common-gate differential input Gm cells, the required reference voltage should be buffered before applying to these low-impedance nodes. Thus, as shown in Fig. 4, a voltage buffer comprised of M_{01}–M_{06} transistors [7] is utilized and it is designed to drive the Gm cells with about 200 nA current consumption. In addition, the stability of two-stage voltage buffer is achieved by using C_{buffer} as the compensation capacitor. An ideal V_{Ref} is considered in the proposed LDO regulator like the other works reported in [4, 7, 14, 20, 18] where the FVF cells have been utilized in the error amplifier to benefit from the current-mode amplification. Indeed, the voltage reference design is out of the scope of this paper similar to many previously published papers on LDO regulators. For this purpose, a voltage buffer is used between the voltage reference and the LDO regulator to isolate them.

The V_{B1}–V_{B4} bias voltages are realized with a simple bias circuit given in [23]. The bias circuit consumes about 400 nA. The channel length of all transistors except M_P is designed to be more than five times of the minimum feature size of the utilized technology to achieve a low quiescent current in the steady state and also ensure that the error amplifier has fast transient response and high gain.

4 Simulation Results and Discussions

To evaluate the usefulness of the proposed LDO regulator, it has been designed and simulated in TSMC 90-nm CMOS process. The compensation capacitors have been realized with metal-insulator-metal (MIM) capacitors. The core area without the output capacitor is $64.5 \times 83.7\ \mu m^2$. According to the post-layout simulation results, the proposed regulator has an acceptable performance in load currents from 30 µA to 40 mA with an output voltage of 750 mV over the input supply voltage variations from 0.9 to 1.2 V. By adding a pseudo-folded-cascode stage to the error amplifier, the open-loop gain of the regulator is increased up to 74 dB in order to improve both the line and load regulations. The total quiescent current of the proposed LDO regulator, including the bias circuit and V_{Ref} buffer circuit, is 1.83 µA and 7.7 µA at load currents of 30 µA (no load) and 40 mA (full load), respectively.

The total amount of compensation capacitors for the stability of the proposed LDO regulator is about 0.5 pF that is not larger than the case in which only one Miller compensation capacitor is used. The external reference voltage is 0.75 V, and a maximum capacitor of 100 pF is added at the regulator output to model the C_L in simulations. In Table 1, the aspect ratio of all transistors and value of all capacitors are shown which are used in the circuit design of the proposed LDO regulator. As it is seen, the channel length of all transistors is larger than the power transistor to achieve low quiescent current and high gain.

Figure 5 shows the simulated loop gain frequency response of the proposed LDO regulator under different load current conditions. The stability of the proposed regulator is achieved by three compensation techniques. According to Fig. 5, the minimum phase margin of the loop gain is 46° in the minimum load current of 30 µA with a low-frequency gain of 74 dB, whereas the lowest loop gain is 41 dB in 40 mA load current with a phase margin of 77°. Table 2 summarizes the simulated loop gain frequency response of the proposed regulator in different process corner cases and temperature variations for load currents of 30 µA and 40 mA. As it is seen, the proposed LDO regulator is stable over PVT variations and different load conditions.

Table 1 Simulated device parameters

Value	Parameter	Value	Parameter
3 × 150 nm/900 nm	$(W/L)_{a1,a2}$	50 × 10 µm/100 nm	$(W/L)_{P}$
150 nm/900 nm	$(W/L)_{a3,a4,a5}$	150 nm/900 nm	$(W/L)_{1,2}$
200 nm/900 nm	$(W/L)_{a6,a7,a8}$	150 nm/720 nm	$(W/L)_{3,4,11,12,BH,BL}$
300 nm/400 nm	$(W/L)_{Ha,La,Hb,Lb}$	400 nm/720 nm	$(W/L)_{7,8}$
150 nm/720 nm	$(W/L)_{M01–M04}$	160 nm/720 nm	$(W/L)_{5,6}$
2 × 150 nm/720 nm	$(W/L)_{M06}$	4 × 500 nm/720 nm	$(W/L)_{13}$
4 × 150 nm/720 nm	$(W/L)_{M05}$	500 nm/720 nm	$(W/L)_{14}$
150 nm/2 µm	$(W/L)_{b1,b2,b5,b6,b7,b8}$	4 × 150 nm/720 nm	$(W/L)_{L0,H0}$
130 nm/4 µm	$(W/L)_{b3,b4}$	2 × 150 nm/720 nm	$(W/L)_{15}$
3 × 180 nm/3 µm	$(W/L)_{b9,b10}$	70 fF, 70 fF	C_a, C_b
180 nm/3 µm	$(W/L)_{b11,b12}$	200 fF, 150 fF, 1 pF	C_M, C_Q, C_{buffer}

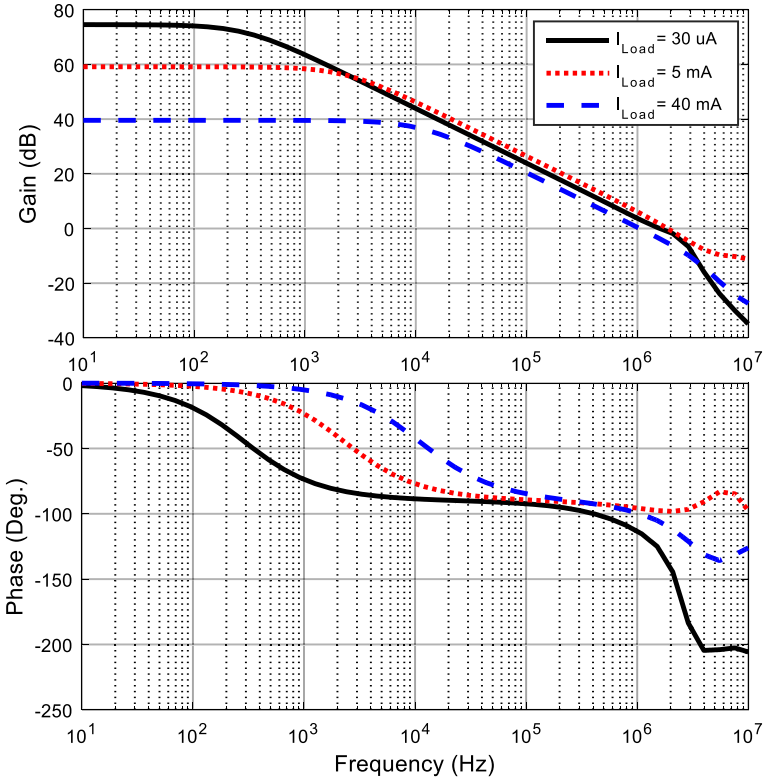

Fig. 5 Open-loop frequency response of the proposed LDO regulator under different load currents with $C_L = 100$ pF

Table 2 Simulated open-loop frequency response of the proposed regulator in different conditions

$I_{Load} = 30$ µA			
Process	FF (−40 °C)	TT (27 °C)	SS (85 °C)
DC gain (dB)	71.2	74.1	76.7
ω_{GBW} (MHz)	1.15	1.2	2.3
Phase margin (°)	44	46.3	63
$I_{Load} = 40$ mA			
Process	FF (−40 °C)	TT (27 °C)	SS (85 °C)
DC gain (dB)	47.8	41.5	36.1
ω_{GBW} (MHz)	0.92	0.73	0.64
Phase margin (°)	88	77	63

The simulated load regulation with two different supply voltages of 0.9 V and 1.2 V is shown in Fig. 6. The achieved load regulations are about 36 µV/mA and 88 µV/mA for $V_{IN} = 0.9$ V and 1.2 V, respectively. Figure 7 also shows the simulated line regulation for load currents of 30 µA and 40 mA. When V_{IN}

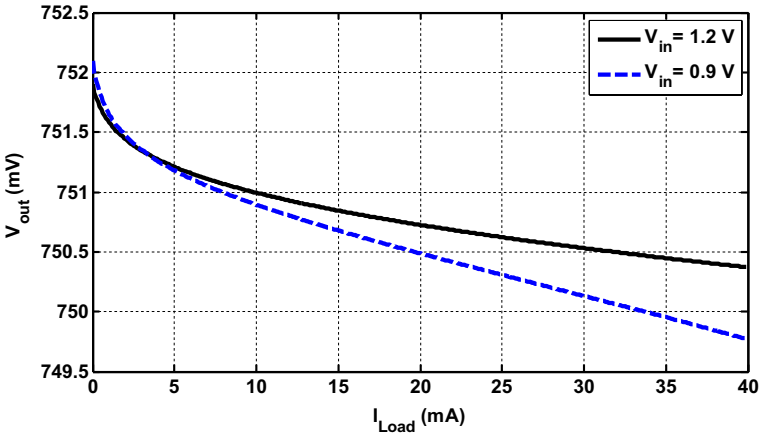

Fig. 6 Simulated load regulation in two different supply voltages and $I_{\mathrm{Load}} = 30$ µA to $I_{\mathrm{Load}} = 40$ mA

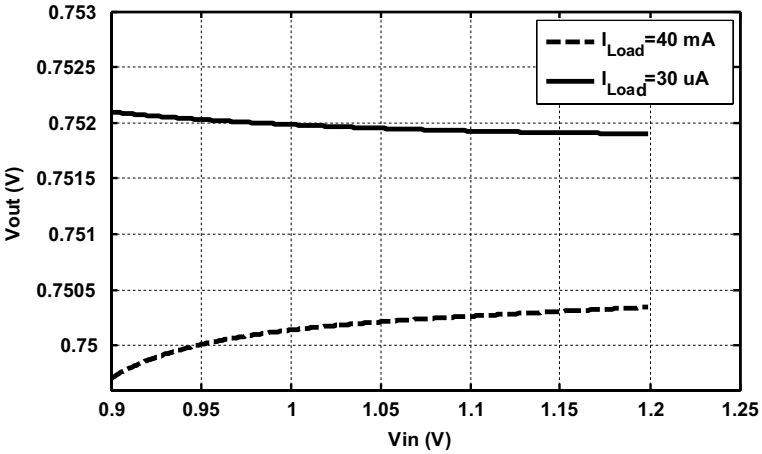

Fig. 7 Simulated line regulation for $I_{\mathrm{Load}} = 30$ µA and $I_{\mathrm{Load}} = 40$ mA

changes from 0.9 to 1.2 V, the achieved line regulations are about 0.8 mV/V and 2.8 mV/V for $I_{\mathrm{Load}} = 30$ µA and $I_{\mathrm{Load}} = 40$ mA, respectively.

The load and line transient responses of the proposed LDO regulator are simulated to verify the stability and evaluate the transient performance. The simulated load transient responses with an output capacitor of 100 pF and $C_{\mathrm{L}} = 40$ pF are shown in Fig. 8, where the load current is changed from 30 µA to 40 mA with the rise and fall times of 200 ns and $V_{\mathrm{IN}} = 0.9$ V. Consequently, when the output capacitor, C_{L}, is reduced, the transient load behavior of the proposed LDO regulator can respond to the intensive changes of load current more quickly. In this simulation, the recovery time is about 0.85 µs at $I_{\mathrm{Q}} = 1.83$ µA.

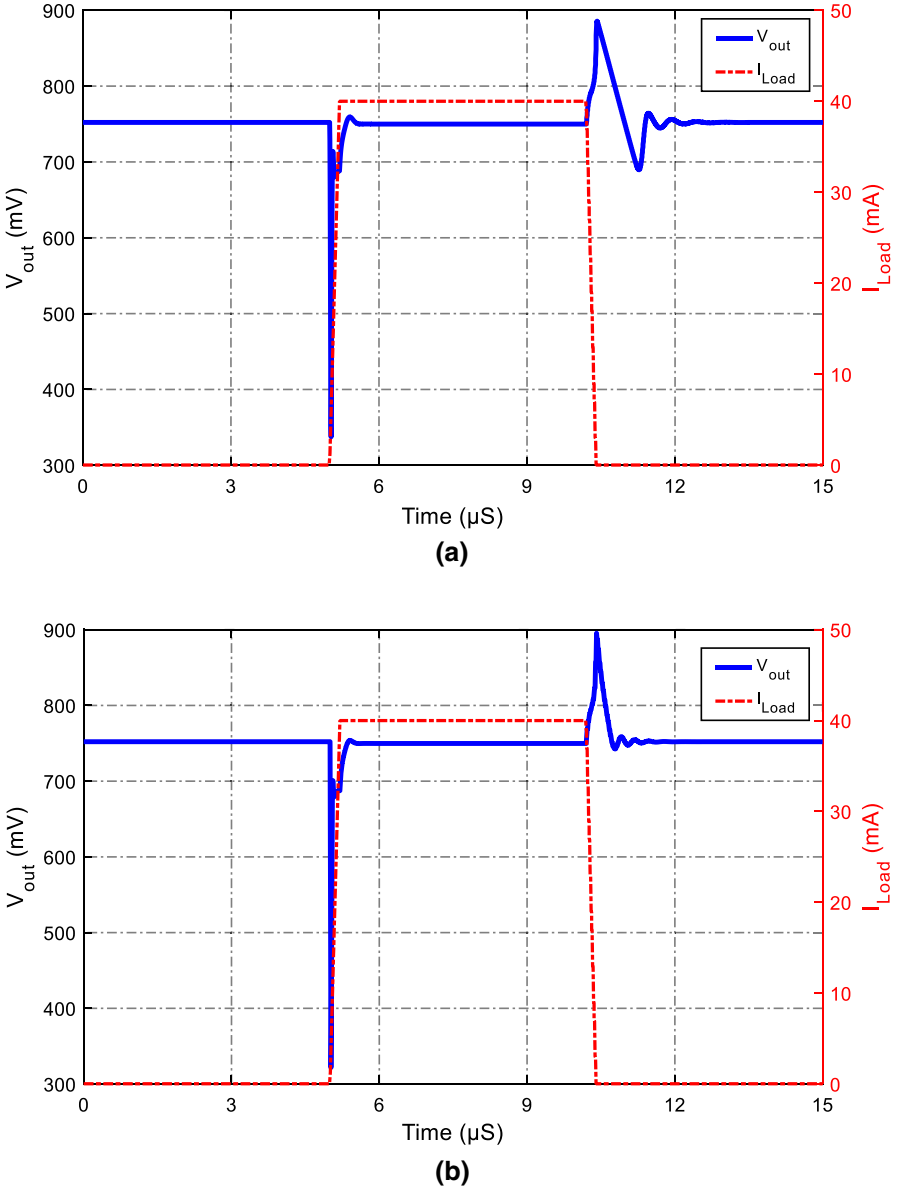

Fig. 8 Simulated load transient response with $V_{out}=0.75$ V and $V_{in}=0.9$ V: **a** $C_L=100$ pF and **b** $C_L=40$ pF

Figure 9 illustrates the simulated transient line response of the proposed LDO regulator with $C_L=100$ pF and two different $I_{Load}=30$ μA and $I_{Load}=40$ mA, respectively. V_{IN} varies from 0.9 to 1.2 V within rise and fall times of 200 ns. The result shows that the output voltage of the regulator is recovered within 0.4 μs, while the maximum output voltage spike is less than 100 mV. Figure 10

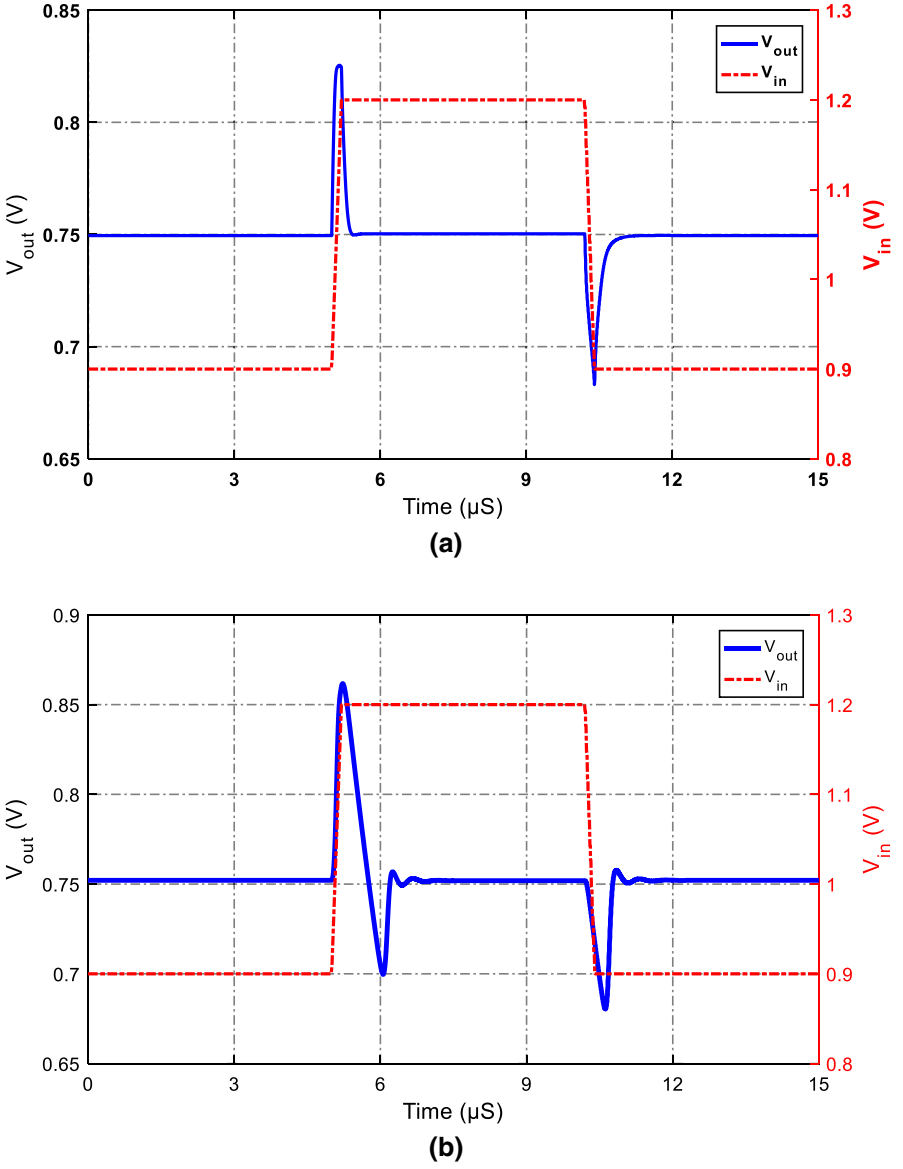

Fig. 9 Simulated line transient response with $V_{out}=0.75$ V, $C_L=100$ pF: **a** $I_{Load}=40$ mA and **b** $I_{Load}=30$ μA

shows the simulated power supply rejection (PSR) of the proposed LDO regulator for $C_L=100$ pF at two different load currents of 30 μA and 40 mA. When I_{Load} is 30 μA, the LDO regulator achieves about −52 dB at 1 kHz and −41 dB at 100 kHz. When I_{Load} increases to 40 mA, the LDO regulator achieves about −43 dB at 1 kHz and −39 dB at 100 kHz.

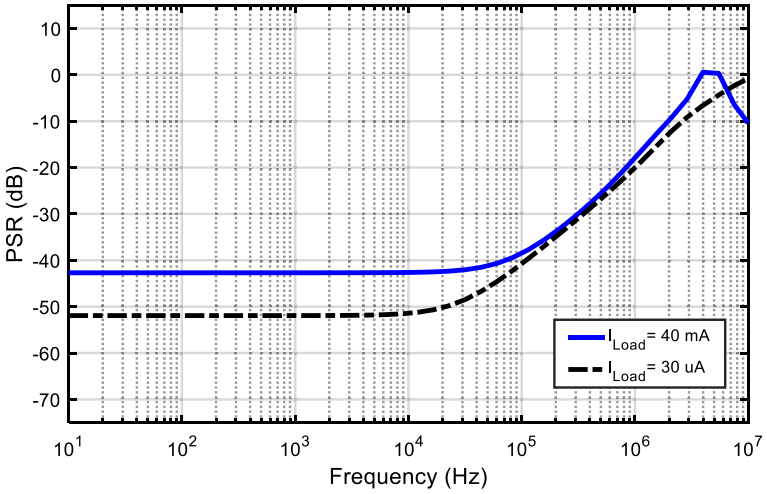

Fig. 10 Simulated PSR of the proposed LDO regulator at $C_L = 100$ pF

The robustness of the proposed LDO regulator against process and mismatch variations were evaluated through extensive circuit level Monte Carlo simulations. The simulated output voltage is shown in Fig. 11 for 1000 runs in which both process and local variations of device parameters were taken into account according to the statistical and mismatch models of 90-nm TSMC CMOS process. As it is seen, the standard deviation of the output voltage is about 19 mV. This value can be reduced by using larger devices in voltage buffer circuit.

Table 3 illustrates the performance comparison between the proposed LDO regulator and several previously reported LDO regulators. The figure-of-merit (FoM)

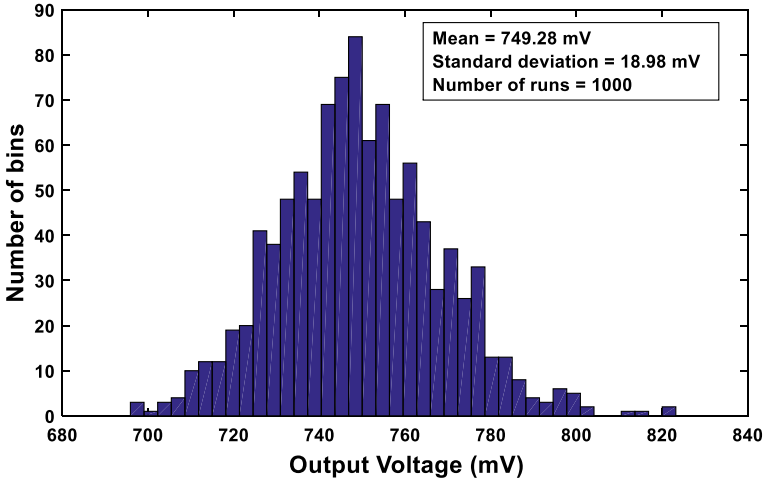

Fig. 11 DC Monte Carlo simulation result of the proposed LDO regulator

Table 3 Performance comparison between the proposed and some previously reported LDO regulators

Parameter	[20]	[4][a]	[14]	[13][a]	[30][a]	[11]	[1][a]	[27]	[2]	[15]	This work[a]
Year	2007	2014	2020	2017	2017	2018	2019	2017	2018	2017	2020
Tech. (µm)	0.35	0.18	0.065	0.065	0.18	0.18	0.18	0.09	0.065	0.18	0.09
$I_{L,Max}$ (mA)	50	100	100	10	100	50	100	2.4	25	600	40
V_{DO} (mV)	100	200	150	250	200	200	100	500	200	200	150
I_Q (µA)	1.2	3.7	14	49.4	16.6	1.8–3.9	42	5.13	1.6–2.42	40	1.83
T_R (µs)	4	6	3.2	0.38	1.3	0.2	2	15	0.0012	0.22	0.85
PSR (dB) @ 1 kHz	N/A	− 65	− 33	− 37	− 65	− 51	− 46	N/A	− 48	− 46	− 43
$C_{on\text{-}Chip}$ (pF)	0	N/A	6	16	2.8	0	4	0	0.6	N/A	0.49
C_L range (pF)	0–100	0–100	0–100	470p	0–100	0–100	0–100	N/A	0.25	2.2 µF	0–100
LNR (mV/V)	4.75	1	12	4	0.16	8.5	2.3	4.916	0.7	N/A	1
LDR (µV/mA)	148	70	90	140	2.7	550	1	1500	280.5	N/A	36
FoM (ns)	0.096	0.22	44.8	1.877	0.216	0.02	0.84	32.03	0.08	15	0.038

LNR line regulation, *LDR* load regulation

[a]Post-layout simulation results

used in [3, 12, 15, 20] is utilized to compare different LDO regulators in terms of important parameters such as the quiescent current (I_Q), the maximum load current ($I_{L,max}$), and the load transient response time (T_R). Indeed, T_R is the required average time of the regulator to respond to the created overshoot and undershoot on the output voltage under sudden changes of the load current or power supply. The figure-of-merit (FoM) is given by:

$$\text{FoM} = T_R \frac{I_Q}{I_{L,Max}} \tag{11}$$

A lower value of this FoM implies a better transient performance. According to Table 3, the proposed LDO regulator achieves an outstanding FoM and it is between the state-of-the-art works. It is worth mentioning that the proposed regulator consumes only a quiescent current of 1.83 µA at small load current. So, the power consumption of the proposed regulator is much lower than the other regulators and it is about 2.8 µW. In addition, the load and line regulation parameters are better than the other LDO regulators. It should be mentioned that the post-layout circuit level simulation results of the proposed LDO regulator is reported here, while some of the references listed in Table 3 are reporting the measured results and this is not a fair comparison. Nevertheless, the achieved outstanding FoM of the simulated LDO regulator verifies the efficiency of the proposed techniques.

5 Conclusions

In this paper, a high-gain and low-power LDO regulator has been proposed. The combination of three Miller, cascode, and Q-reduction techniques is used in the frequency compensation of the regulator to achieve the stability with ultra-low power consumption. A three-stage error amplifier is utilized, and the loop gain of the regulator is increased by using a pseudo-folded-cascode amplifier in the first stage. The adaptive biasing technique is employed to provide larger gain bandwidth and enhance the slew rate at the gate of the power transistor. The utilized G_m cells based on the FVF structure and the push–pull architecture at the gate of the power transistor improve the transient response of the regulator. The quiescent current becomes very low by using G_m cells and Q-reduction capacitor. Post-layout simulation results verify the usefulness of the proposed regulator, and hence, it can be used in implantable biomedical applications where ultra-low power consumption is needed.

References

1. Y. Bastan, M. Janipoor-Deylamani, P. Amiri, Fast-transient capacitor-less low-dropout regulator with input current-differencing and dynamic current-boosting. Analog Integr. Circuit Signal Process. **99**(5), 371–381 (2019)
2. S. Bu, K.-N. Leung, Y. Lu, J. Guo, Y. Zheng, A fully integrated low-dropout regulator with differentiator-based active zero compensation. IEEE Trans. Circuits Syst. I Regul. Pap. **65**(10), 3578–3591 (2018)

3. S.S. Chong, P.K. Chan, A 0.9-µA quiescent current output-capacitorless LDO regulator with adaptive power transistors in 65-nm CMOS. IEEE Trans. Circuits Syst. I Reg. Pap. **60**(4), 1072–1081 (2013)
4. R. Fathipour, A. Saberkari, H. Martinez, E. Alarcon, High slew rate current mode transconductance error amplifier for low quiescent current output-capacitorless CMOS LDO regulator. Integr. VLSI J. **47**(2), 204–212 (2014)
5. S. Golabi, M. Yavari, A three-stage class AB operational amplifier with enhanced slew rate for switched-capacitor circuits. Analog Integr. Circuits Signal Process. **83**(1), 111–118 (2015)
6. S. Golabi, M. Yavari, Design of CMOS three-stage amplifiers for fast-settling switched-capacitor circuits. Analog Integr. Circuits Signal Process. **80**(2), 195–208 (2014)
7. J. Guo, K.N. Leung, A 6 µW chip-area-efficient output-capacitorless LDO in 90-nm CMOS technology. IEEE J. Solid State Circuits **45**(9), 1896–1905 (2010)
8. X. Han, T. Burger, Q. Huang, An output-capacitor-free adaptively biased LDO regulator with robust frequency compensation in 0.13 µm CMOS for SoC application, In *IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 2699–2702 (2016)
9. P. Hazucha et al., Area-efficient linear regulator with ultra-fast load regulation. IEEE J. Solid State Circuits **40**(4), 933–940 (2005)
10. H. Ho, K.N. Leung, Dynamic bias-current boosting technique for ultralow power low-dropout regulator in biomedical applications. IEEE Trans. Circuits Syst. II Exp. Briefs **58**(3), 174–178 (2011)
11. S.R. Khan, I. Nadeem, Low quiescent current capacitorless small gain stages LDO with controlled pass transistors. Analog Integr. Circuits Signal Process. **94**(2), 323–331 (2018)
12. S.K. Lau, P.K.T. Mok, K.N. Leung, A low dropout voltage regulator for SoC with Q-reduction. IEEE J. Solid State Circuits **42**(3), 658–664 (2007)
13. C. Li, P.-K. Chan, FVF LDO regulator with dual dynamic-load composite gain stage. Analog Integr. Circuit. Signal Process **92**(1), 131–140 (2017)
14. G. Li, H. Qian, J. Guo, B. Mo, Y. Lu, D. Chen, Dual active-feedback frequency compensation for output-capacitorless LDO with transient and stability enhancement in 65-nm CMOS. IEEE Trans. Power Electron. **35**(1), 415–429 (2020)
15. K. Li, Y. Zheng, S. Liter, A transient-enhanced low dropout regulator with rail to rail dynamic impedance attenuation buffer suitable for commercial design. Microelectron. J. **63**(5), 27–34 (2017)
16. Y. Lu, Y. Wang, Q. Pan, W.-H. Ki, C.-P. Yue, A fully-integrated low-dropout regulator with full-spectrum power supply rejection. IEEE Trans. Circuits Syst. I Reg. Pap. **62**(3), 707–716 (2015)
17. A. Maity, A. Patra, A single-stage low-dropout regulator with a wide dynamic range for generic applications. IEEE Trans. Very Large Scale Integr. Syst. **24**(6), 2117–2127 (2016)
18. A. Maity, A. Patra, Tradeoffs aware design procedure for an adaptively biased capacitorless low dropout regulator using nested Miller compensation. IEEE Trans. Power Electron. **31**(1), 369–380 (2016)
19. V. Majidzadeh, A. Schmid, Y. Leblebici, A fully on-chip LDO voltage regulator for remotely powered cortical implants, in *European Solid-State Circuits Conference (ESSCIRC)*, pp. 424–427 (2009)
20. T.Y. Man, P.K.T. Mok, M. Chan, A high slew-rate push-pull output amplifier for low-quiescent current low-dropout regulators with transient response improvement. IEEE Trans. Circuits Syst. II Exp. Briefs **54**(9), 755–759 (2007)
21. M. Mojarad, M. Yavari, A low power four-stage amplifier for driving large capacitive loads. Int. J. Circuit Theory Appl. **42**(9), 978–988 (2014)
22. O. Omeni, A.C.W. Wong, A.J. Burdett, C. Toumazou, Energy efficient medium access protocol for wireless medical body area sensor networks. IEEE Trans. Biomed. Circuits Syst. **2**(4), 251–259 (2008)
23. B. Razavi, *Design of Analog CMOS Integrated Circuits* (McGraw-Hill, New York, 2001)
24. J.G.A. Rincon-Mora, *Analog IC Design with Low-Dropout Regulators (LDOs)* (McGraw-Hill, New York, 2009)
25. M.R. Salehi, R. Dastanian, E. Abiri, S. Nejadhasan, A 147 µW, 0.8 V and 7.5 (mV/V) LIR regulator for UHF RFID application. Int. J. Electron. Commun. **69**(1), 133–140 (2015)
26. L.S.Y. Wong, S. Hossain, A. Ta, J. Edvinsson, D.H. Rivas, H. Nääs, A very low-power CMOS mixed-signal IC for implantable pacemaker applications. IEEE J. Solid State Circuits **39**(12), 2446–2456 (2004)
27. W.-B. Yang, Y.-Y. Lin, Y.-L. Lo, Design of fast-locked digitally controlled low-dropout regulator for ultra-low voltage input. Circuits Syst. Signal Process. **36**(12), 5041–5061 (2017)

28. M. Yavari, A design procedure for CMOS three-stage NMC amplifiers. IEICE Trans. Fundam. **E94-A**(2), 639–645 (2011)
29. M. Yavari, Active-feedback single miller capacitor frequency compensation techniques for three-stage amplifiers. J. Circuits Syst. Comput. **19**(7), 1381–1398 (2010)
30. Y. Zeng, Y. Li, X. Zhang, H.-Z. Tan, A push-pulled FVF based output-capacitorless LDO with adaptive power transistors. Microelectron. J. **64**(6), 69–77 (2017)