A Calibration Technique for Pipelined ADCs Using Self-Measurement and Histogram-Based Test Methods

Tohid Moosazadeh and Mohammad Yavari, *Member, IEEE*

***Abstract*—This brief presents a digital background calibration technique for pipelined analog-to-digital converters (ADCs) to correct the capacitor mismatch, finite dc gain, and nonlinearity of residue amplifiers. It estimates the calibration coefficients at start-up by a modified self-measurement method with low-precision stimulation signals in the multistage calibration. Then, during the ADC normal operation, a sliding histogram in the vicinity of the decision boundaries of stage comparators is utilized to adjust the calibration coefficients in order to follow the variation of errors. To do so, the ratio of information achieved from the initial and new histograms is used to update the calibration coefficients. Behavioral simulation results of a 12-bit pipelined ADC show that the proposed calibration technique improves the ADC linearity by more than 4 bits and it is robust against the variation of errors.**

***Index Terms*—Digital background calibration technique, gain error, gain nonlinearity, pipelined analog-to-digital converters (ADCs).**

I. Introduction

DIGITAL calibration techniques have been widely used in high-performance pipelined analog-to-digital converters (ADCs) [1]–[9]. Correlation-based methods modulate the analog errors by a pseudorandom noise (PN) sequence and then extract the modulated information in digital domain to achieve the required performance [1], [2]. In these methods, the input signal appears as an uncorrelated noise with larger amplitude than the PN sequence, resulting in a large convergence time. In equalization-based calibration techniques, the errors are generally measured using the calibration signals [3], [4]. Although these techniques achieve a fast conversion rate, they need extra analog circuits to produce high-precision calibration signals.

Histogram-based calibration techniques correct the errors by measuring the code density at the ADC output [5]. However, their performance highly depends on the input signal statistics. To alleviate this issue, a combination of the foreground and background calibration techniques is utilized in [6] and [7]. At the start-up, the errors are estimated by using a foreground calibration such as [8] and [9], and then, the ADC output histogram is used to follow the variation of errors in the background mode.

In this brief, a new calibration technique is proposed for pipelined ADCs, which employs a modified self-measurement method with relaxed accuracy calibration signals to correct the errors at the ADC start-up. Then, a hardware efficient histogram-based method called the "sliding histogram" is used during the ADC normal operation to track the variation of errors and realize a background calibration scheme.

This brief is organized as follows. In Section II, the modeling of errors in pipelined ADCs is presented. The proposed calibration technique is described in Section III. Behavioral simulation results are provided in Section IV, and finally, Section V concludes this brief.

Manuscript received October 31, 2014; revised January 24, 2015 and March 15, 2015; accepted April 25, 2015. Date of publication May 21, 2015; date of current version August 28, 2015. This brief was recommended by Associate Editor B. Sahoo.

The authors are with the Integrated Circuits Design Laboratory, Department of Electrical Engineering, Amirkabir University of Technology, Tehran 15914, Iran (e-mail: myavari@aut.ac.ir).

Color versions of one or more of the figures in this brief are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TCSII.2015.2435851

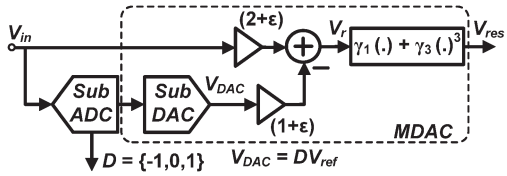

Fig. 1. Architecture of a nonideal 1.5-bit stage.

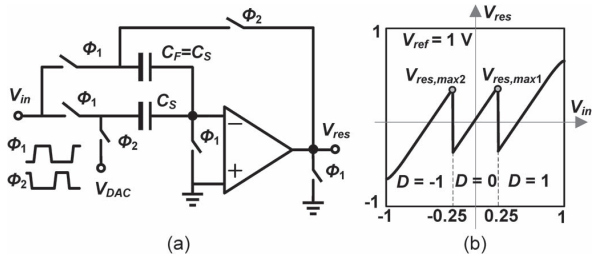

Fig. 2. (a) MDAC circuit and (b) its transfer function including the circuit nonidealities.

II. ADC Error Modeling

Fig. 1 shows the commonly used 1.5-bit stage structure in pipelined ADCs including the circuit nonidealities. Here, the input signal $V_{\rm in}$ is quantized to $D = \{-1, 0, 1\}$ using a sub-ADC with decision points of $\pm V_{\rm ref}/4$. Then, the quantized input signal is converted back to the analog domain with a sub-digital-to-analog converter (sub-DAC). The sub-DAC output $V_{\rm DAC} = DV_{\rm ref}$ is subtracted from the amplified input signal to produce the residue signal by employing a multiplying DAC (MDAC) shown in Fig. 2(a). The MDAC circuit samples the input signal during Φ_1 on both C_S and C_F. Then, during Φ_2, the capacitor C_F is placed in the feedback path, while the bottom plate of C_S is connected to $V_{\rm DAC}$ to produce the residue signal.

Considering the circuit nonidealities such as the capacitor mismatch ε, finite amplifier dc gain, and nonlinearity, which are modeled by γ_1 and γ_3 in Fig. 1, the stage residue signal $V_{\rm res}$ can be expressed by a third-order polynomial [10] as

$$\begin{aligned} V_{\rm res} &= \gamma_1 V_r + \gamma_3 V_r^3 \\ V_r &= (2+\varepsilon)V_{\rm in} - (1+\varepsilon)V_{\rm DAC}. \end{aligned} \tag{1}$$

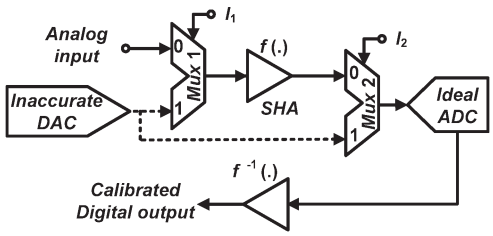

Fig. 3. Self-measurement method in [11].

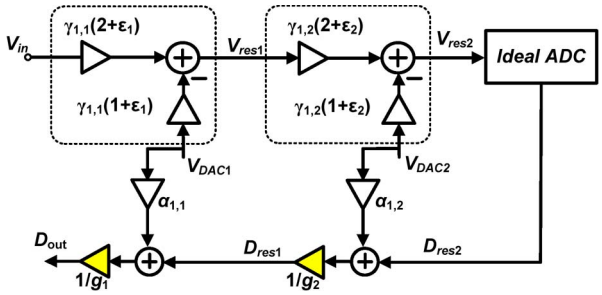

Fig. 4. Multistage calibration with the self-measurement method.

It should be mentioned that (1) is an appropriate model for low- to medium-resolution ADCs. A more precise model using higher order terms of V_r should be considered in (1) for high-resolution ADCs [8]. The transfer function of $V_{\rm res}$ including the aforementioned circuit nonidealities is shown in Fig. 2(b). To estimate the stage input signal $V_{\rm in}$, the inverse of (1) is approximated by $V_r \approx (1/\gamma_1)V_{\rm res} - (\gamma_3/\gamma_1^4)V_{\rm res}^3$. Therefore, we have

$$V_{\rm in} \approx \frac{V_{\rm res} + \alpha_3 V_{\rm res}^3 + \alpha_1 D V_{\rm ref}}{g} \tag{2}$$

where g, α_1, and α_3 are the calibration coefficients as

$$g = \gamma_1(2+\varepsilon), \quad \alpha_1 = \gamma_1(1+\varepsilon), \quad \alpha_3 = -\gamma_3/\gamma_1^3. \tag{3}$$

Assuming that $D_{\rm in} \equiv V_{\rm in}/V_{\rm ref}$ and $D_{\rm res} \equiv V_{\rm res}/V_{\rm ref}$ to denote the digitized input and residue signals, respectively, $D_{\rm in}$ will be as

$$D_{\rm in} \approx \frac{D_{\rm res} + \alpha_3 D_{\rm res}^3 + \alpha_1 D}{g}. \tag{4}$$

Hence, the calibration process is to estimate g, α_1, and α_3 for each of the 1.5-bit stages. It is performed recursively from the last stage to the first one where the calibrated stages produce the digitized output signal for the stage under the calibration.

III. Proposed Calibration Technique

A. Concept of the Self-Measurement Method

The starting point of the foreground phase in the proposed calibration technique is the self-measurement method which has been presented in [11] to correct the front-end sample and hold amplifier (SHA) nonlinearity in a pipelined ADC. Fig. 3 illustrates the concept of this method, where the SHA nonlinearity is corrected by estimating its inverse transfer function $f^{-1}(.)$ in digital domain.

During the self-measurement intervals, when I_1 or I_2 is high, an inaccurate DAC with several dc voltage levels is used in the SHA input, while the output is digitized by an ideal pipelined ADC. Then, the DAC is disconnected from the SHA input, and it is applied to the ADC. Therefore, the digital equivalents of the SHA input and output signals are available, and $f^{-1}(.)$ is properly estimated in digital domain with the ADC resolution.

Herein, the accuracy of the DAC signals is not important as long as they remain constant during the calibration. However, in practice, the accuracy of measurements will be affected by the thermal noise. It can be alleviated by repeating the measurements several times and using their average values.

B. Proposed Self-Measurement Method

The conventional self-measurement method can also be employed in the MDAC using the sub-DAC path which has a similar gain property as the SHA. This configuration can measure α_1 and α_3 in (4). However, the gain error g is the main drawback of this approach since it prevents the multistage calibration. Any uncorrected gain error in the latter stages affects the coefficients of the previous stages in the conventional self-measurement method. For more clarification, suppose a pipelined ADC with two 1.5-bit stages followed by an ideal backend ADC shown in Fig. 4. Here, for simplicity, the 1.5-bit stages are supposed to have only the gain error ($\gamma_3 = 0$). The calibration starts from the second stage to reach the first one. Conventional self-measurement method in the second stage measures $\alpha_{1,2} = \gamma_{1,2}(1+\varepsilon_2)$, where the unmeasured g_2 is considered as its ideal value, i.e., 2. In this case, a linear output $D_{\rm res1}$ containing the gain error is resulted. Then, the second stage is combined with the backend ADC as Fig. 4 to make the backend ADC for the first stage. By repeating the same procedure to the first stage, $\alpha_{1,1} = \gamma_{1,1}(1+\varepsilon_1)$ is estimated independent of the backend ADC gain error, while its output $D_{\rm res1}$ is affected by this error. According to Fig. 4, the digitized output $D_{\rm out}$ will be as

$$D_{\rm out} \equiv \frac{1}{g_1 g_2}\left(\gamma_{1,1}\gamma_{1,2}(2+\varepsilon_1)(2+\varepsilon_2)V_{\rm in} + \left(g_2\alpha_{1,1} - \gamma_{1,2}(2+\varepsilon_2)\alpha_{1,1}\right)V_{\rm DAC1}\right). \tag{5}$$

Therefore, assuming that $g_1 = g_2 = 2$ in the conventional self-measurement method, the digitized input samples are distorted. To solve this problem, the self-measurement method is modified to measure g in (4), which is the main achievement exploited here for the multistage calibration. According to (5), $g_1 = \gamma_{1,1}(2+\varepsilon_1)$ and $g_2 = \gamma_{1,2}(2+\varepsilon_2)$ result in a true calibrated digital output.

At first, the modified self-measurement method applies the calibration signals into the sub-DAC path with a zero input signal ($V_{\rm DAC} = V_{\rm cal}$, and $V_{\rm in} = 0$). In this condition, considering (4), the digitized residue signal $D_{\rm res}$ is related to the digitized calibration signal by the backed-ADC $D_{\rm cal}$ through the relation

$$D_{\rm res} + \alpha_3 D_{\rm res}^3 + \alpha_1 D_{\rm cal} \approx 0 \tag{6}$$

where D is substituted by $D_{\rm cal}$ in (4) which means that the calibration signal is applied to the sub-DAC path. Herein, the least mean square (LMS) algorithm is used to estimate α_1 and α_3 as

$$\begin{aligned} \alpha_1(n+1) &= \alpha_1(n) - \mu_1 e_1(n) D_{\rm cal}(n) \\ \alpha_3(n+1) &= \alpha_3(n) - \mu_3 e_1(n) D_{\rm res}^3(n) \end{aligned} \tag{7}$$

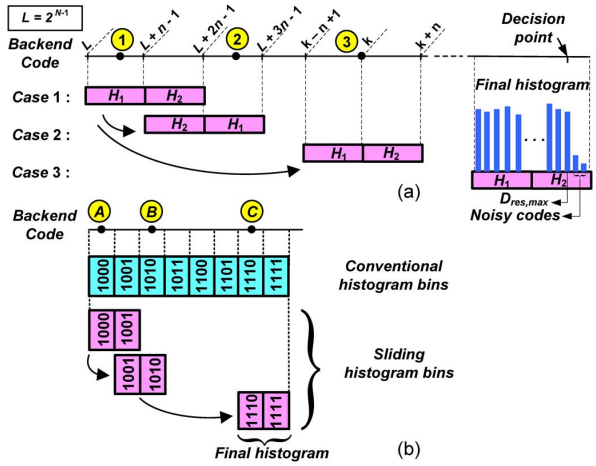

Fig. 5. (a) Concept of the sliding histogram method. (b) Simple example.

where μ_1 and μ_3 are the update step sizes of the LMS algorithm and

$$e_1(n) = D_{\rm res}(n) + \alpha_3(n) D^3_{\rm res}(n) + \alpha_1(n) D_{\rm cal}(n). \quad (8)$$

Having known the values of α_1 and α_3, g is estimated by applying the calibration signals to both of the paths of this stage ($V_{\rm in} = V_{\rm DAC} = V_{\rm cal}$). In this case, $D_{\rm res}$ is related to $D_{\rm cal}$ as

$$(g - \alpha_1) D_{\rm cal} - D_{\rm res} - \alpha_3 D^3_{\rm res} \approx 0 \quad (9)$$

and g is estimated with another LMS algorithm as

$$g(n+1) = g(n) - \mu_g e_2(n) D_{\rm cal}(n) \quad (10)$$

where μ_g is the LMS update step size and

$$e_2(n) = (g(n) - \alpha_1)\, D_{\rm cal}(n) - D_{\rm res}(n) - \alpha_3 D^3_{\rm res}(n). \quad (11)$$

By this way, the modified self-measurement method can be used in the multistage calibration where the calibration coefficients are estimated as (7) and (10) using two LMS algorithms.

Since the LMS algorithm is employed here, considering w coefficients in the inverse model, at least $(w+1)$ independent equations are needed to estimate them [8]. It means that more calibration signals should be utilized in the estimation of a higher order model.

C. Tracking of Errors With Sliding Histogram

A histogram-based calibration technique called the "sliding histogram" is proposed to track the variation of errors due to the temperature and power supply voltage changes in the background. Supposing negligible amount of variations in amplifier nonlinearity and comparator offset for low- to medium-resolution ADCs [6], [7], the relation (4) is simplified as

$$D_{\rm in} = \frac{D_{\rm res} + \alpha_1 D}{g}. \quad (12)$$

The required information to track the changes in the coefficient g can be achieved by $V_{\rm res,max\,1}$ in Fig. 2(b) similar to [7]. Here, this capability is extended to track the changes in α_1 by $V_{\rm res,max\,1}$ and $V_{\rm res,max\,2}$ in Fig. 2(b). Exactly after the foreground calibration, $V_{\rm res,max\,1}$ and $V_{\rm res,max\,2}$ are estimated, and their values are used as the reference in the next estimation to track the variation of errors.

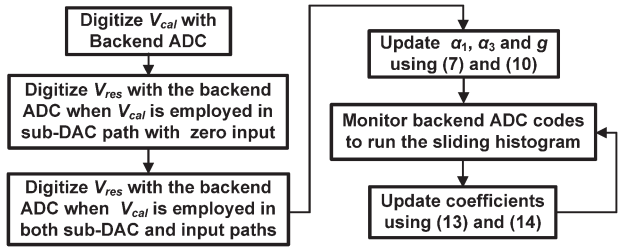

Fig. 6. Flowchart of the proposed calibration technique.

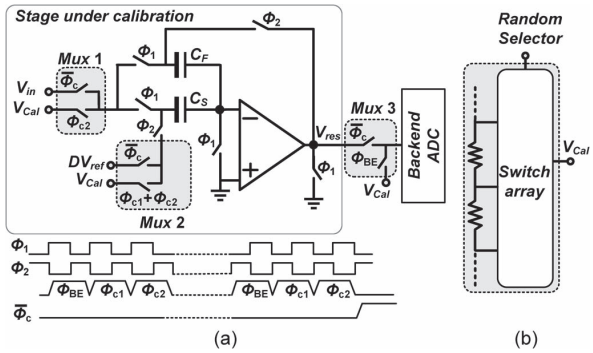

Fig. 7. (a) MDAC structure with the proposed calibration technique. (b) Resistive ladder with a switch array to generate the calibration signals.

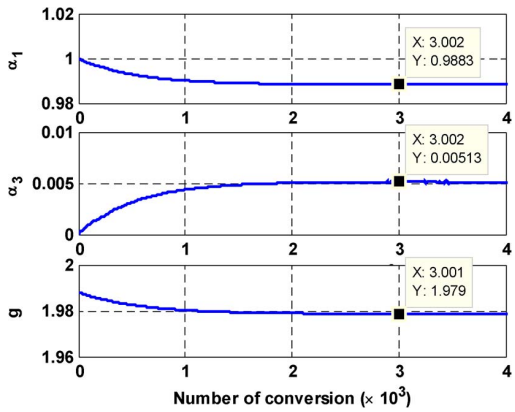

Fig. 8. Initial convergence of the calibration coefficients in the foreground phase.

For $V_{\rm res,max\,1}$, the sub-ADC output D is zero, and the relation (12) is reduced to $D_{\rm in} = D_{\rm res,max\,1}/g$. The ratio of the initially estimated maximum residue signal $D_{\rm res,max\,1,old} = g_{\rm old} D_{\rm in1}$ to its changed value $D_{\rm res,max\,1,new} = g_{\rm new} D_{\rm in2}$ is given by

$$g_{\rm new} = g_{\rm old} \left(\frac{D_{\rm res,max\,1,new}}{D_{\rm res,max\,1,old}} \right) \quad (13)$$

where $D_{\rm in1} = D_{\rm in2}$ is used assuming the negligible variations in the offset voltage of the comparators. In this equation, $g_{\rm old}$ and $g_{\rm new}$ denote the parameter g before and after the variation, respectively. Following the changes of $V_{\rm res,max\,2}$ in Fig. 2(b), the new value of α_1 can be obtained as

$$\alpha_{1,\rm new} = D_{\rm res,max\,2,new} - \frac{D_{\rm res,max\,1,new}}{D_{\rm res,max\,1,old}} (-\alpha_{1,\rm old} + D_{\rm res,max\,2,old}). \quad (14)$$

Therefore, the variation of errors can be corrected by following the changes in $D_{\rm res,max\,1}$ and $D_{\rm res,max\,2}$.

It is worth mentioning that, for high-resolution ADCs, the variation of amplifier nonlinearity due to the temperature and power supply voltage changes is not negligible. Therefore, the relations (13) and (14) limit the accuracy of the background calibration technique in high-resolution applications.

Taking into account the circuit noise, the histogram of backend codes can be used to estimate the true values of the maximum codes [5]. For the noisy codes around the decision points, the height of the histogram bins will be much less than the adjacent bins, and hence, they can simply be discarded [7].

Considering the maximum offset tolerance of a 1.5-bit stage which is $V_{\rm ref}/4$, the output codes of its N-bit backend ADC in the range of $[2^{N-1}, 2^N - 1]$ will contain $D_{\rm res,max\,1}$ and $D_{\rm res,max\,2}$. Therefore, the histogram length will be $L = 2^{N-1}$, and it needs 2^{N-1} digital comparators and counters to be realized [5], [7].

The sliding histogram method uses two n-bin histograms H_1 and H_2 ($n \ll L$) to monitor the backend codes of the stage under the calibration. As shown in Fig. 5(a), they slide from the minimum codes toward the decision point by the occurrence of backend codes. Finally, a short-length histogram is formed around the maximum code. Here, due to the reduced length of the histogram, the required hardware complexity is also reduced.

From Fig. 5(a), H_1 and H_2 cover the codes of the initial ranges of $[L,\ L+n-1]$ and $[L+n,\ L+2n-1]$, respectively. When a backend code is produced, three different cases may occur. In case "1," the code is in the initial range, and H_1 and H_2 start to count the number of that code occurrence. In case "2," the code is in the range of $[L+2n,\ L+3n-1]$, H_1 bins are set to this range, and its counters are reset, while H_2 bins remain as the previous. In other words, H_2 and H_1 will cover $[L+n,\ L+2n-1]$ and $[L+2n,\ L+3n-1]$ ranges, respectively. In case "3," the code k is greater than $L+3n-1$, and the maximum bin of H_1 is set to k, while it is set to $k+n$ in H_2. At the end of sliding, a short-length histogram shown in Fig. 5(a) is created around the maximum residue voltage $D_{\rm res,max}$. Applying this procedure for $D=0$ and $D=-1$ regions leads to $D_{\rm res,max\,1}$ and $D_{\rm res,max\,2}$, respectively, which can be used in relations (13) and (14) to track the variation of the calibration coefficients.

For more clarification, consider a pipelined ADC with a 1.5-bit first stage and a 4-bit backend ADC. Fig. 5(b) shows the conventional and sliding histogram-based calibrations to measure the maximum residue signal. The conventional method needs an eight-bin histogram to count the occurrence of backend codes in the presence of the comparator offset and thermal noise. In the proposed method, two one-bin histograms are used, while one of them is initially set to "1000" code, and the other one is set to "1001." For example, sample "A" in Fig. 5(b) occurs in the range of the initial bins and, therefore, it is counted.

Then, the sample "B" occurs out of the initial range. Therefore, the histograms cover the "1001" and "1010" codes similar to case 2 in Fig. 5(a). After that, the sample "C" occurs like case 3 in Fig. 5(a), and the histograms should slide to the "1110" and "1111" codes. At the end of sliding, a two-bin histogram in the vicinity of $D_{\rm res,max}$ will be produced. This simple example shows that, for a 4-bit backend ADC, the number of histogram bins is reduced four times compared to the conventional method. For long histograms, the reduction rate will be significant. When the ADC's circuit noise is comparable to the quantization noise, it should be considered as a Gaussian white noise with a standard deviation of σ_n. Therefore, by taking into account the noisy bins, a conservative choice for the length of sliding histograms is $n > 3\sigma_n$ [5].

The flowchart of the proposed calibration technique is illustrated in Fig. 6. It estimates the calibration coefficients by the self-measurement method and tracks their variations by the sliding histogram technique.

D. Hardware Complexity

To implement the modified self-measurement method, calibration signals are employed at the input and sub-DAC paths of 1.5-bit stages using analog multiplexers as shown in Fig. 7(a). In the foreground calibration phase, the digitized calibration signal $D_{\rm cal}$ is produced in $\Phi_{\rm BE}$, while the updated information for calibration coefficients in (7) and (10) is provided in Φ_{c1} and Φ_{c2}, respectively. Then, during $\bar{\Phi}_c$, the ADC enters the normal operation mode. A simple resistive ladder with a switch array shown in Fig. 7(b) can be used to produce the calibration signals. The calibration signals should settle fast enough such that the ADC different paths could sample the same signals. The foreground phase also needs some digital multipliers and adders to implement two LMS algorithms in (7), (8), (10), and (11) in addition to the divider, multipliers, and adders in (4).

The sliding histogram method needs some digital logic to control the sliding algorithm in addition to $2n$ digital comparators and counters. Assuming that $\sigma_n = m \times$ LSB of an N-bit backend ADC, at least $6m$ digital comparators and counters are required for the sliding histogram method. Moreover, the relations (13) and (14) require some adders, multipliers, and dividers to be implemented.

Therefore, the hardware complexity of the proposed calibration technique is on the order of some analog multiplexers, a resistive ladder with a switch array, and digital circuits to realize the LMS algorithms along with the sliding histogram method.

IV. Simulation Results

Several behavioral simulation results are provided for a 12-bit pipelined ADC comprising of two 1.5-bit stages and an ideal 10-bit backend ADC. A Gaussian circuit noise is added to the input signal to restrict the ADC effective number of bits to 11.5. In these simulations, a comparator offset with $3\sigma = V_{\rm ref}/8$ and capacitor mismatch ε of -0.2% are considered. An amplifier with 45-dB dc gain is considered, which is corresponding to $\gamma_1 = 0.99$ and $\gamma_3 = -0.5\%$. A 3-bit random selector is used to select the calibration signals as $V_{\rm cal} = \{1,\ 4,\ 8,\ 12,\ 15\}V_{\rm ref}/16$ with a maximum accuracy of 7-bit.

The initial convergence of the first stage calibration coefficients with the calibrated second stage in the foreground phase is shown in Fig. 8. The calibration coefficients α_1, α_3, and g are stable around their theoretical values $\gamma_1(1+\varepsilon) \approx 0.988$, $-\gamma_3/\gamma_1^3 \approx 5.2 \times 10^{-3}$, and $1/\gamma_1(2+\varepsilon) \approx 1.978$, respectively, after almost 3×10^3 conversions. The simulated ADC output spectrum for a full-scale sinusoidal input signal and 4096 FFT points without any calibration is shown in Fig. 9(a). It is also shown in Fig. 9(b) and (c) after the foreground calibration with the modified and conventional self-measurement methods, respectively. The modified self-measurement method improves the signal-to-noise and distortion ratio (SNDR) and spurious free dynamic range (SFDR) more than 25 and 40 dB, respectively, while the conventional method improves them only 6 dB.

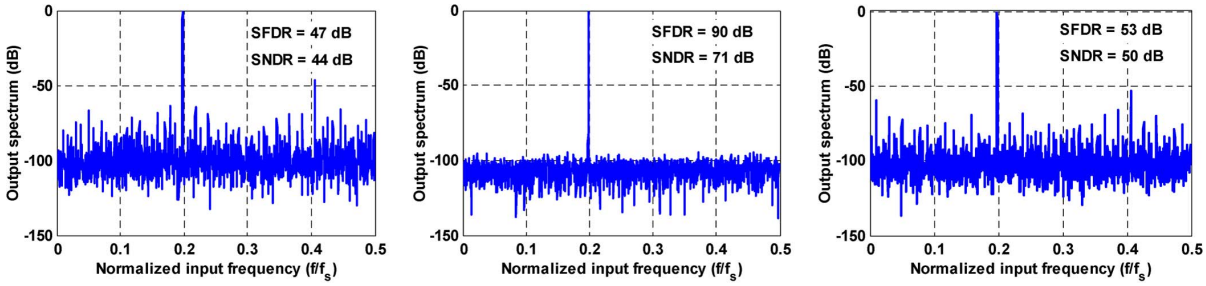

Fig. 9. Simulated ADC output spectrum (a) before any calibration, (b) after the foreground calibration with the modified self-measurement method, and (c) after the foreground calibration with the conventional self-measurement method.

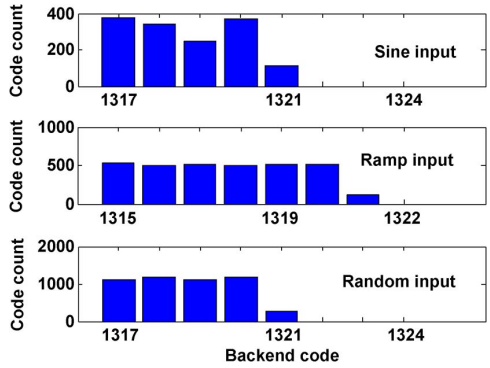

Fig. 10. Histogram of the backend codes in the vicinity of $V_{\rm ref}/4$ for input signals of (a) sine, (b) ramp, and (c) random.

TABLE I
COMPARISON RESULTS WITH SEVERAL OTHER CALIBRATION TECHNIQUES

Ref.	Sensitivity to V_{cal} accuracy	Hist. length	Tracking capability
[4]	High	–	α_1 and α_3
[5]	-	Long	α_1
[6]	High	Long	α_1 and g
[7]	Low	Average	g
[10]	Low	–	–
This work	Low	Short	α_1 and g

To demonstrate the tracking capability of the sliding histogram method, ε and γ_1 in the first stage are changed to -0.4% and 0.95, respectively. In this condition, SNDR and SFDR degrade to 39 and 43 dB, respectively, before tracking the variation of errors, where, after about 2×10^6 samples, they are returned to the values achieved in the foreground phase.

With a sampling frequency on the order of multihertz, the error tracking takes a few seconds. Therefore, considering the slow variation of power supply voltage and temperature which is on the order of minutes as mentioned in [6] and [7], the tracking phase is fast enough to follow the errors.

The probability distribution of the input signal affects the performance of the histogram-based calibration techniques [5]. To examine this issue, the histograms of the first stage output with sine, ramp, and random input signals are obtained after 2×10^6 input samples. The histogram of the codes in the vicinity of $V_{\rm ref}/4$ is shown in Fig. 10, where they are produced with two four-bin sliding histograms. According to this figure, the maximum back-end code is "1320" for each input. It is clear that the noisy code of "1321" should be discarded.

The proposed calibration scheme is compared with several other techniques in Table I. In summary, the hardware complexity is reduced in each phase of the proposed calibration technique; in particular, the background phase has an outstanding hardware reduction rate. Since the number of bins in the sliding method is decreased in comparison with the conventional histogram-based methods, its power consumption will be reduced as well.

V. CONCLUSION

A digital background calibration technique has been presented to correct the gain error and gain nonlinearity in the pipelined ADCs. At start-up, it corrects the errors in the foreground mode using the modified self-measurement method which allows the multistage calibration with accuracy relaxed calibration signals. Then, during the ADC normal operation, a sliding histogram is employed to track the variation of errors. Behavioral simulation results show that the errors are appropriately corrected, and their variations are tracked with very low hardware complexity.

REFERENCES

[1] J. Li and U.-K. Moon, "Background calibration techniques for multistage pipelined ADCs with digital redundancy," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 50, no. 9, pp. 531–538, Sep. 2003.
[2] A. Panigada and I. Galton, "Digital background correction of harmonic distortion in pipelined ADCs," *IEEE Trans. Circuits Syst. I*, vol. 53, no. 9, pp. 1885–1895, Sep. 2006.
[3] X. Wang *et al.*, "A 12-bit 20-Msample/s pipelined analog-to-digital converter with nested digital background calibration," *IEEE J. Solid-State Circuits*, vol. 39, no. 11, pp. 1799–1808, Nov. 2004.
[4] C. R. Garce *et al.*, "A 12-bit 80-msample/s pipelined ADC with bootstrapped digital calibration," *IEEE J. Solid-State Circuits*, vol. 40, no. 5, pp. 1038–1046, May 2005.
[5] L. Brooks and H.-S. Lee, "Background calibration of pipelined ADCs via decision boundary gap estimation," *IEEE Trans. Circuits Syst. I,*, vol. 55, no. 10, pp. 2969–2979, Nov. 2008.
[6] S. H. W. Chiang *et al.*, "A 10-bit 800-MHz 19-mW CMOS ADC," *IEEE J. Solid-State Circuits*, vol. 49, no. 4, pp. 935–949, Apr. 2014.
[7] C. Ravi, T. Rahul, and B. Sahoo, "Histogram based deterministic digital background calibration for pipelined ADCs," in *Proc. IEEE VLSI Des. Embedded Syst.*, Jan. 2014, pp. 569–574.
[8] B. Zeinali, T. Moosazadeh, M. Yavari, and A. Rodriguez-Vazquez, "Equalization-based digital background calibration technique for pipelined ADCs," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 22, no. 2, pp. 322–333, Feb. 2014.
[9] B. Sahoo and B. Razavi, "A 10-b 1-GHz 33-mW CMOS ADC," *IEEE J. Solid-State Circuits*, vol. 48, no. 6, pp. 1442–1452, Jun. 2013.
[10] A. Verma and B. Razavi, "A 10-bit 500-MS/s 55-mW CMOS ADC," *IEEE J. Solid-State Circuits*, vol. 4, no. 11, pp. 3039–3050, Nov. 2009.
[11] P. Harpe, A. Zanikopoulos, H. Hegt, and A. V. Roermund, "Digital post-correction of front-end track-and-hold circuits in ADCs," in *Proc. IEEE ISCAS*, May 2006, pp. 1503–1506.