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A novel digital calibration technique for pipelined ADCs

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Abstract: This paper presents a digital background calibration technique to correct the capacitors mismatch, gain error and gain nonlinearities of 1.5 bit/stage pipelined ADCs. The calibration technique uses a modified structure for the ADC stages, the skip-fill method and LMS algorithm and does not require any accurate calibration signal and any added analog circuitry; just some digital circuits are needed to fill the skipped samples and realize the LMS algorithm. Circuit level simulation results in a 90-nm CMOS technology are provided for a 12-bit 80-MS/s pipelined ADC to verify the effectiveness of the proposed calibration technique.

Keywords: pipelined ADCs, capacitor mismatch, gain error, amplifier nonlinearity, digital background calibration, skip-fill method

Classification: Integrated circuits

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1 Introduction

The design of high-speed, high-resolution analog-to-digital converters (ADCs) is a key issue in high-performance digital communication systems. The pipelined ADCs can produce such speeds but the design of high precision analog elements becomes more complicated as the device dimensions and supply voltages are scaled down. The capacitors mismatch, gain error, and gain nonlinearity are the main precision limitation factors for high-resolution pipelined ADCs in deep-submicron low-voltage CMOS technologies [1, 2].

A common way to overcome these precision limitations is to apply a calibration method to the converter. Recently, a few digital calibration techniques that cancel the precision limitations of pipelined ADCs have been proposed [1, 2, 3, 4]. In these methods, the errors are generally measured using a calibration signal where the precision of this signal in deep-submicron technologies is an important issue. An accurate DAC calibrated with an additional calibration cycle is used in [1] to produce accurate calibration signals where in [2] with driving the mean square of 128 local errors across the input range to zero, they are measured using a medium-precision calibration signal. A high-precision on-chip DAC is used for 10-bit resolution in [3] and in [4] an accurate calibration signal produced with the DAC noise cancellation technique is used. Here, an efficient method is proposed which uses the lowest extra analog elements without the need for an accurate calibration signal.

2 ADC errors modeling

A pipelined ADC is composed of several low-resolution stages. Commonly, the 1.5-bit/stage architecture is used for high-speed pipelined ADCs [3]. Figure 1 (a) shows a single-ended switched-capacitor circuit implementation of the 1.5-bit stage with a capacitor non-flip-around multiplying digital-to-analog converter (MDAC). During ϕ_1, the stage input signal is sampled and then during ϕ_2, the difference of input signal and analog equivalent of the sub-ADC output (V_{dac}) is amplified. This configuration is chosen to simplify the modeling of the ADC stages and the calibration process like [1, 2].

As discussed in [2], the inverse function of the ADC stages with the above-mentioned structure in digital domain can be approximated as a third-order polynomial function given by:

$$D_{in} = D + \beta_1 D_{out} + \beta_3 D_{out}^3 \tag{1}$$

where D_{in} and D_{out} are the digital equivalent of stage input and output, respectively, and D is the stage sub-ADC output. The stage capacitors mismatch, gain errors, and gain nonlinearities of the amplifier are considered in the model with the β_1 and β_3 coefficients [2]. Having known β_1 and β_3 in (1) for all stages, the inverse function of ADC in digital domain is calculated and thus its input signal can be digitized without any dependency to the analog elements preciseness.

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3 Proposed calibration technique

The goal of the proposed calibration technique is the measurement of coefficients in (1) by using constant calibration signals without any dependency to their accuracy. The ADC uses 14 1.5-bit stages and a 2-bit flash ADC as last stage to achieve 12-bit resolution. In the stages 1 and 2, both linear and nonlinear terms in (1) are considered where in stages 3 to 14 only the linear term is considered ($\beta_3 = 0$). Each calibration cycle begins with the 14^{th} stage and is done stage by stage up to the first stage. The background calibration was performed by skip-fill method proposed in [5]. As shown in Fig. 1 (b), for the i^{th} stage background calibration, the ADC input sample is skipped at n_0T_S and then the calibration signal, V_{cal}, is inserted to this stage in the produced time slot at $[n_0+0.5(i-1)]T_S$ where T_S and n_0 are the sampling period and time index respectively. So, in the proposed technique, the calibration is performed at the created time slots without interrupting the ADC normal operation.

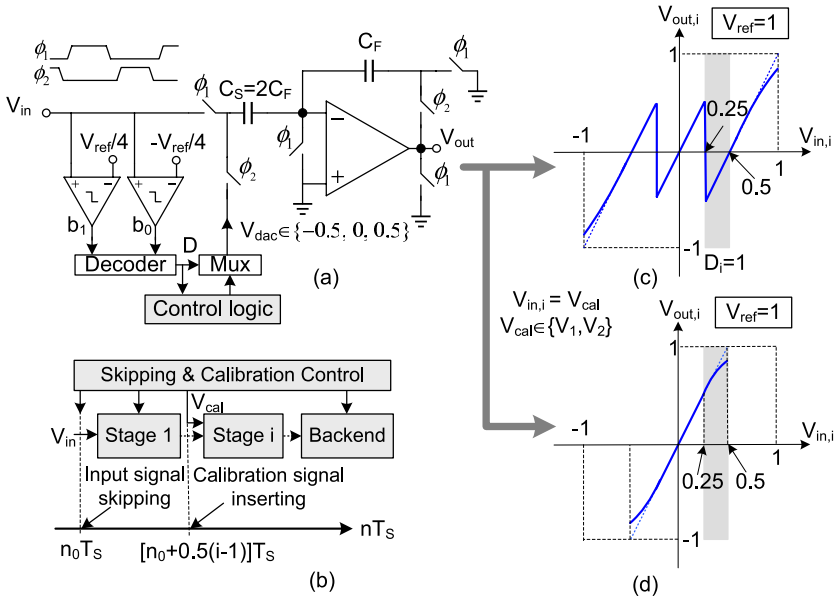

Fig. 1. (a) A 1.5 bit stage with capacitor non-flip-around MDAC, (b) background implementation of calibration, (c) the i^{th} stage transfer function in 1.5-bit mode, and (d) the i^{th} stage transfer function in multiply-by-two mode.

To calibrate β_1 for the stages 3 to 14, the same concept as [1] is used to measure the stage transfer function gaps in the comparators threshold voltage, $\pm 0.25\,V_{ref}$. If the stage output is accurately digitized by the backend stages, then for $i = 3$ to 14, we have $D_{in,i} = D_i + \beta_{1i}D_{out,i}$, where $D_{in,i}$ and $D_{out,i}$ are the digital equivalent of the i^{th} stage input and output, respectively, D_i is its sub-ADC output and β_{1i} is the linear term coefficient in i^{th} stage inverse function.

To implement the proposed technique in these stages assuming zero offset

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comparators, each stage must be configured as two different modes in the calibration. In the first mode, with skipping a sample in the ADC input, the i^{th} stage is configured as 1.5-bit mode at the appropriate time as shown in Fig. 1 (c) and a constant calibration signal, $V_{cal} = V_1$, is applied to the i^{th} stage input. V_1 is produced by a resistor ladder which is chosen with low precision in the range $0.25\,V_{ref} < V_1 < 0.5\,V_{ref}$ (so $V_{dac} = 0.5\,V_{ref}$) and near the stage comparator threshold voltage same as [1] concept. Then, D_i and the digitized output with backend stages in this mode, $D_{out1,i}$, are stored in a memory. In the second mode, as shown in Fig. 1 (d), with skipping another sample in the ADC input, the i^{th} stage is configured as multiply-by-two mode ($V_{dac} = 0$) and the digitized stage output for V_1 with backend stages, $D_{out2,i}$, is also stored in a memory. Indeed, in the multiply-by-two mode, the i^{th} stage is configured as a sample and hold and D_i is not used. With these two stored data and from (2), the digital equivalent of V_1 for the i^{th} stage in these two modes, $D_{in1,i}$ and $D_{in2,i}$, ($D_{in1,i} = D_{in2,i}$) are as follows:

$$\left.\begin{array}{l} D_{in1,i} = D_i + \beta_{1i} D_{out1,i} \\ D_{in2,i} = \beta_{1i} D_{out2,i} \end{array}\right\} \Rightarrow \beta_{1i}(D_{out2,i} - D_{out1,i}) = D_i. \tag{2}$$

Therefore β_{1i} can be extracted without any dependency on V_1. Moreover, it must be considered that when the i^{th} stage is in the calibration process, the backend stages have been calibrated and produce an acceptable accurate digital equivalent for this stage output.

By extending the applied technique, both β_1 and β_3 for stages 1 and 2, can also be extracted. In addition to V_1, another calibration signal, $V_{cal} = V_2$, is applied to these stages. V_2 is also produced by the mentioned resistor ladder in the range $0.25\,V_{ref} < V_2 < 0.5\,V_{ref}$ and should be greater than V_1 as well as possible to measure the variation in amplifier gain caused by large amplitude input. However, with full-scale calibration signal ($0.5\,V_{ref}$ for multiply-by-two mode), the nonzero amplifier offset would cause over ranging. To maximize V_2 amplitude while avoiding such over ranging, the calibration signal is chosen near the stage DAC reference voltage, $0.5\,V_{ref}$. In this condition, to extract β_1 and β_3, according to the explained sample skipping algorithm, V_1 and V_2 are applied in the two different mentioned modes to the stage input and the results are stored in the memory. Hence, from (1) we have:

$$\begin{array}{l} V_{in,i}|_{i=1,2} \in \{V_1, V_2\} : \left\{\begin{array}{l} D_{in1,i} = D_i + \beta_{1i} D_{out1,i} + \beta_{3i} D_{out1,i}^3 \\ D_{in2,i} = \beta_{1i} D_{out2,i} + \beta_{3i} D_{out2,i}^3 \end{array}\right\} \\ \Rightarrow \beta_{1i}(D_{out2,i} - D_{out1,i}) + \beta_{3i}(D_{out2,i}^3 - D_{out1,i}^3) = D_i. \end{array} \tag{3}$$

The least mean square (LMS) algorithm [6] is used to simplify the required digital hardware for solving (2) and (3) as follows:

$$\begin{array}{l} \beta_{1i}(n+1) = \beta_{1i}(n) + \mu_1 e(n)(D_{out2,i} - D_{out1,i}) \\ \beta_{3i}(n+1) = \beta_{3i}(n) + \mu_3 e(n)(D_{out2,i}^3 - D_{out1,i}^3) \end{array} \tag{4}$$

where μ_1 and μ_3 are the LMS update step size in the coefficients extraction and $e(n)$ is given by:

$$e(n) = D_i - \beta_{1i}(n)(D_{out2,i} - D_{out1,i}) - \beta_{3i}(n)(D_{out2,i}^3 - D_{out1,i}^3) \tag{5}$$

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where for stages 3 to 14 is used with $\beta_{3i} = 0$. The accuracy of V_2 would not limit our calibration performance because it is enough that V_2 be less than $0.5V_{ref}$ to avoid over ranging. Moreover, about V_1 accuracy it must be explained that the comparator offset can limit the range of V_1. To avoid this problem, the multiplexer used in the sub-DAC realization controls the stage mode in the V_1 insertion. For zero offset comparators of i^{th} stage, in the 1.5 bit stage mode, V_1 produces a sub-ADC output of $D_i = 1$ and $V_{dac} = 0.5\,V_{ref}$, otherwise the sub-ADC has offset error ($D_i = 0, V_{dac} = 0$) and to calibrate the stage accurately, in the second insertion of V_1, it is configured with $V_{dac} = 0.5\,V_{ref}$ using mode control logic, although $D_i = 0$.

4 ADC circuit implementation details

To evaluate the performance of the proposed calibration technique, a 12-bit 80 MS/s pipelined ADC has been designed in the circuit level using standard 90-nm CMOS technology with 1-V supply voltage. In the designed ADC, the input sample and hold circuit is eliminated with time constant matching of existing paths in the first stage. With thermal noise considerations, the stages 1 to 4 have 4 pF, 1.8 pF, 0.9 pF and 0.4 pF sampling capacitors, respectively, and the rest of the stages use 0.2 pF sampling capacitor where maximum 0.1% capacitor mismatch is considered in each stage. A two-stage Miller compensated amplifier with two cascaded common-source amplifiers is used as the ADC amplifiers where its open loop DC gain is only 38 dB with maximum closed-loop gain variation of 10 LSB of 12 bit resolution. The charge-distribution structure with a dynamic latch is used as the ADC comparators [7]. In addition, the bootstrapping technique is used in the sampling switches needing high linearity [8]. For skipped samples recovering, an 80-taps FIR filter is used to realize the nonlinear Lagrange interpolation.

5 Simulation results

The analog circuits of ADC are simulated with HSPICE while the calibration process is implemented with MATLAB. Figures 2 (a) and 2 (b) plot the simulated DNL and INL before and after the calibration, respectively. The uncalibrated ADC has a peak INL of 45 LSB where after calibration, the peak INL falls below 0.25 LSB. Figure 2 (c) shows the simulated output spectrum for a 1 MHz, 1.2-V peak-to-peak differential analog input sampled at 80 MHz where the SNDR and SFDR improvements are over 35 dB and 39 dB, respectively. For survey of ADC performance in the Nyquist band, the SNDR and SFDR are calculated for several input signal frequency. The simulation results are shown in Fig. 2 (d). The peak SNDR is equal to 73 dB after calibration for an input frequency of 10 MHz. Each stage calibration time is about 2^{12} ADC sampling periods, so the total calibration time is about 14×2^{12} ADC sampling periods. The achieved performance for the pipelined ADC and the comparison with recently reported ADCs is shown in Table I using a figure of merit (FoM) defined by $FoM = \frac{Power}{2^{ENOB} f_S} V_{DD}$ as [4], where $Power$, f_S and V_{DD} refer to the ADC power consumption, sampling

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frequency and supply voltage respectively and *ENOB* shows its effective number of bits. The simulated ADC shows the lowest FoM verifying the usefulness of the proposed calibration technique in design of high-speed and high-resolution pipelined ADCs.

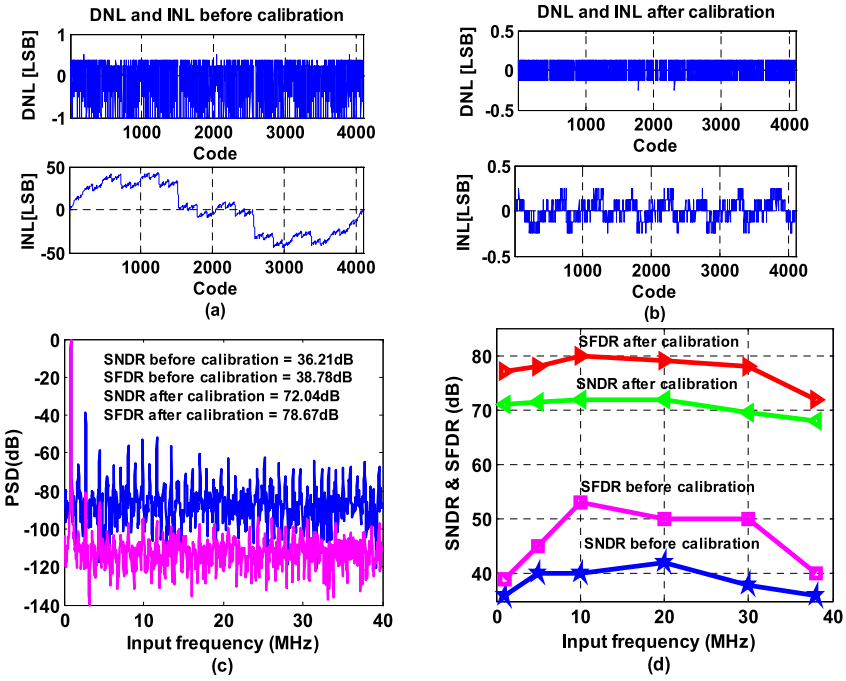

Fig. 2. (a) INL and DNL before calibration, (b) INL and DNL after calibration, (c) output spectrum before and after calibration for 0 dBFS input signal, and (d) SNDR and SFDR vs. ADC input signal frequency.

Table I. Performance comparison of the simulated ADC.

Ref.	Process	V_{DD} (V)	f_s (MS/s)	INL (LSB)	DNL (LSB)	SFDR (dB)	SNDR (dB)	AnalogPower (mW)	FoM (pJ.V/step)
This Work	90 nm	1	80	±0.25	−0.25	78	72	57.8	0.22
[1]	0.25 μm	2.5	80	+0.24	+0.09	84.5	72.6	340	3
[2]	90 nm	1.2	200	+1.3	+0.59	-	64	348	1.6
[3]	90 nm	1.2	500	1	0.4	-	52	55	0.4
[4]	90 nm	1.2	100	3.6	0.54	85	69.5	93	0.44

6 Conclusion

A digital background calibration technique was proposed to correct the capacitors mismatch, gain error and gain nonlinearities of the amplifiers in the 1.5 bit/stage pipelined ADCs. The proposed algorithm does not require any accurate calibration signal and is only realized by digital circuits. The circuit level simulation results show the effectiveness of the proposed calibration technique.

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