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A pseudo-differential MDAC with a gain-boosting inverter for pipelined ADCs

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Abstract In this paper, a power-efficient pseudo-differential (PD) multiplying digital-to-analog converter (MDAC) is presented for pipelined analog-to-digital converters (ADCs). The proposed MDAC eliminates the explicit common-mode feedback circuit which is required in fully-differential configurations without any power penalty. Furthermore, a new class-AB gain-boosting inverter is proposed to be used in PD MDAC structures for further power saving. This inverter provides dynamic load current with no significant static power consumption and achieves high DC gain using a new gain-boosting technique. To demonstrate the effectiveness of the proposed circuits, they are utilized in the realization of a 1.5-bit/stage 10 bit 100 MS/s pipelined ADC.

Keywords Inverter-based switched-capacitor circuits · Gain-boosting · Pipelined ADCs · Pseudo-differential MDAC · Nano-meter CMOS technologies

1 Introduction

Pipelined analog-to-digital converters (ADCs) are utilized for high-speed and medium to high resolution applications with small area and low power consumption. It is a popular architecture for high performance digital communications and high quality video systems [1]. The rapid growth of these applications demands the design of pipelined ADCs with high speed, low power consumption, and small area in scaled down CMOS technologies [2]. As technologies scale down, the design of analog circuits especially high DC gain and low power operational amplifiers (opamps) becomes more challenging mainly due to the reduced voltage headroom and short channel effects. To overcome these challenges, a few number of design techniques have been reported [2–7]. Pseudo-differential (PD) amplifiers avoid the voltage drop across the tail current source, and hence, allow wider signal ranges and make the circuit attractive for low power applications [2]. However, removing the tail current source results in large common-mode (CM) variations in the amplifier. The body driven opamp [3] has poor noise performance and results in lower bandwidth. The digitally assisted opamp [4] adds to the design complexity and needs a complicated signal processing. To remove the need of pipelined ADCs for the power hungry opamp, the comparator based [5], dynamic residue amplifier [6], and capacitive charge pump [7] techniques have been reported.

Recently, inverters are used as simple opamps in PD switched-capacitors circuits making them more power efficient [8, 9]. The simplicity of an inverter makes it as an attractive architecture. However, the DC gain of a simple inverter in more scaled CMOS technologies is very low and not applicable as an opamp for high performance ADCs. Moreover, due to the inverter single-ended nature, a PD configuration should be utilized to enhance the CM noise rejection. Several solutions have been proposed to alleviate the inverter DC gain requirement. The correlated double sampling technique [2] and a digital calibration technique [8] are used to compensate the inverter low DC gain effects. In [9], a gain-boosting inverter based on the regulated cascode structure is used as the opamp in a sigma–delta modulator. This inverter uses low threshold voltage in gain-boosting transistors.

In this paper, a power-efficient PD multiplying digital-to-analog converter (MDAC) employing a new gain-boosting

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inverter is proposed for pipelined ADCs. Indeed, the main contribution of this work is eliminating the CM feedback (CMFB) circuit of fully-differential amplifiers in pipelined ADCs using the proposed MDAC and replacing the power hungry amplifiers with the new gain-boosting inverter. To demonstrate the usefulness of the proposed MDAC and inverter, a low-voltage low-power pipelined ADC is designed and simulated in a 90 nm CMOS process.

The paper is organized as follows. In Sect. 2, the PD pipelined ADCs are analyzed. The proposed PD MDAC and gain-boosting inverter are explained in Sects. 3 and 4, respectively. The implementation of these circuits in a 10-bit 100 MS/s pipelined ADC and the simulation results are presented in Sect. 5. Finally, Sect. 6 concludes the paper.

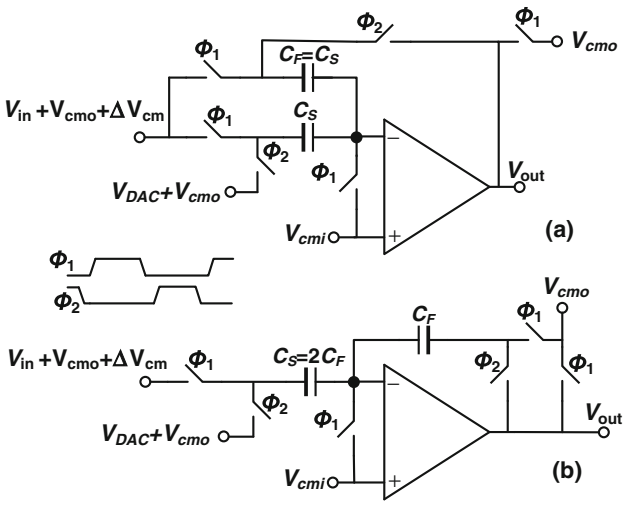

Fig. 1 Single-ended circuit implementation of **a** CFA and **b** CNFA MDACs

2 PD pipelined ADCs

The MDAC circuit in pipelined ADCs is composed from the sampling and amplifying networks where typically a PD sampling network and a fully-differential amplifier are utilized. Fully-differential amplifiers improve the signal dynamic range over their single-ended counterpart because they provide better CM noise rejection and low distortion performance, and increase the output voltage swing. However, to obtain the above advantages in fully-differential amplifiers, the CMFB circuit is needed to fix the CM voltage of high impedance nodes and suppress the CM signal components. Moreover, in these amplifiers, there is a tail current source to reduce the CM noise which decreases the signal swing. Generally, the fully-differential implementations provide better signal-to-noise ratio but at the cost of more power consumption.

In conventional pipelined ADCs, the power dissipation is mainly determined by the amplifiers DC bias current according to the required settling accuracy at the given sampling rate and it depends on the topology and the dynamic performance of the amplifiers. The PD pipelined ADCs use a PD sampling network and PD amplifiers to reduce the DC bias current while maintaining the high speed operation. Although these PD ADCs achieve lower power consumption than their fully-differential counterpart, as demonstrated in [10], they still require an equivalent CMFB circuit to control the output DC voltage. Otherwise, any input CM variation becomes larger along the pipeline.

Two well-known structures of the MDAC circuit in pipelined ADCs are the capacitor flip-around (CFA) and capacitor non-flip-around (CNFA) schemes. The single-ended circuit implementation of these MDACs for a 1.5-bit resolution is depicted in Fig. 1. In the fully-differential structure, they are sensitive to the input CM voltage variation without using any CMFB circuit. In the following, the effect of input CM voltage variation, ΔV_{cm}, is analyzed. Using the charge conservation law in the CFA MDAC structure shown in Fig. 1(a) and assuming an ideal amplifier, we can write:

$$V_{out} = \frac{C_S + C_F}{C_F} V_{in} - \frac{C_S}{C_F} V_{DAC} + V_{cmo} + \frac{C_S + C_F}{C_F} \Delta V_{cm}, \tag{1}$$

where the CM voltage of MDACs input and output signals and also the DAC signal is V_{cmo} and V_{cmi} is the input CM voltage of the amplifier. The same analysis for CNFA structure shown in Fig. 1(b) results in:

$$V_{out} = \frac{C_S}{C_F}(V_{in} - V_{DAC}) + V_{cmo} + \frac{C_S}{C_F} \Delta V_{cm}. \tag{2}$$

Therefore, in these structures, the input CM voltage variation is amplified by the same gain of the input signal. As a result, small CM deviations at the input of the pipelined ADC results in serious CM level shifts at the back-end stages, because the deviation at the nth stage becomes $2^n \times \Delta V_{cm}$ for the deviation of ΔV_{cm} at the ADC input.

The main advantage of PD amplifiers is that they eliminate the tail current source which allows wider input and output swing and low power consumption. However, without the tail current source, the CM gain will be large resulting in increased CM variations at the amplifier. So, PD amplifiers like as fully-differential ones require an extra CMFB circuit. The CMFB circuit degrades the amplifier performance and has to be carefully designed to avoid instability and nonlinearity resulting in the complex circuitry and more power consumption.

The CM leakage problem in PD amplifiers can be solved by using CM feedforward technique [11]. In this method,

input CM signals are inversely feed forwarded through another path to the output nodes. The CM signals coming from both paths would be cancelled out at the output node which results in a decreased CM gain. The complexity and extra power consumption are the major disadvantages of this technique.

A hybrid structure including both fully-differential and PD stages in pipelined ADCs was employed in [10] at the cost of increased power consumption and design complexity due to employing the fully-differential MDACs. To operate in the low supply voltages, it is necessary to use the PD architectures with CM level control in the whole stages of the pipelined ADC. This is introduced in [2] in order to fully exploit the low-power advantage of the PD architecture. The MDAC in [2] uses the combined fully-differential and PD sampling network and PD amplifiers without any CMFB circuit. The differential gain of this MDAC is still two, but the CM gain is just one, because one pair of sampling capacitors is differentially sampled without any CM reference. This equivalent CMFB operation is achieved with no speed penalty. However, large input CM voltage variations can still disturb the MDAC operation. In [12], a CM voltage stabilizer is used in the non-floating sampling path of [2] which is implemented by a sigma–delta modulator to reduce the MDAC CM gain.

In [8, 13], the input and output CM voltages are decoupled using a PD sampling network for MDAC which suppresses the input CM voltage variations at the cost of reduced speed in [8] and increased power consumption in [11].

In next section, the proposed MDAC is described. It solves the CM components amplification in the PD amplifiers without any speed reduction and increased power consumption in comparison with the conventional MDACs.

3 Proposed PD MDAC

3.1 Structure of the proposed MDAC

To avoid the amplification of the CM voltage variation in the conventional MDACs, a new 1.5-bit MDAC is developed by using the differential (floating) sampling scheme and it is shown in Fig. 2. This MDAC employs six equal size capacitors ($C_{S1} = C_{S2} = C_F$) in the sampling and feedback networks. To analysis the effect of input signal CM voltage variation, ΔV_{cm}, the sampling, Φ_1, and amplifying phases, Φ_2, of the proposed MDAC are separately shown in Fig. 3. The main assumption in the proposed MDAC is the equal CM voltages in its input and output signals which is shown by V_{cm}.

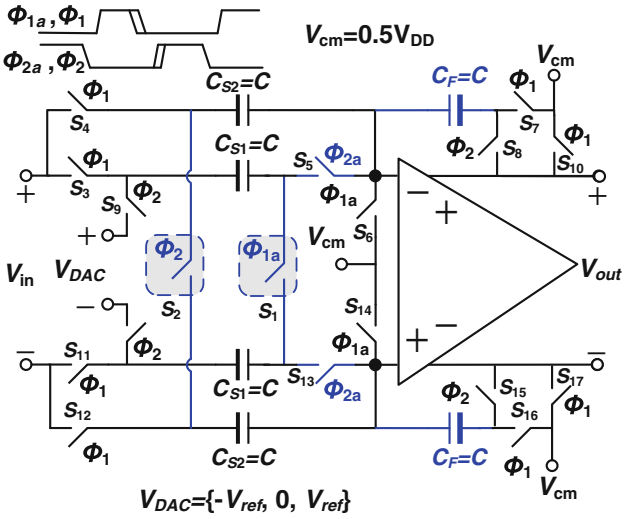

Fig. 2 Proposed input CM voltage insensitive MDAC

As depicted in Fig. 3(a), in the sampling phase, the top plates of C_{S1} capacitors are connected to each other with a floating switch (S_1 in Fig. 2). So, the differential signal is sampled at these capacitors and its CM voltage is cancelled. Capacitors C_{S2} sample the difference of the input signal and amplifier input CM voltage, V_{cm}, while capacitors C_F are discharged. As shown in Fig. 2, the bottom plate sampling is utilized to eliminate the signal dependent charge injection by turning off Φ_{1a} slightly earlier than Φ_1. At the end of Φ_1 phase, the stored charge on the capacitors, Q_1, is given by:

$$Q_1 = C_{S1}V_{in+} + (V_{in+} + \Delta V_{cm})C_{S2}, \tag{3}$$

where the single-ended charges are considered to analysis the output CM voltage of the MDAC. During amplifying phase, as shown in Fig. 2, the floating potential is level shifted to V_{cm} by turning on Φ_{2a} slightly earlier than Φ_2. The equivalent circuit for the amplifying phase is shown in Fig. 3(b). Capacitors C_{S1} are connected to the DAC voltages and the bottom plate of capacitors C_{S2} are connected to each other with another floating switch (S_2 in Fig. 2) to transfer only the differential charge to the capacitors C_F placed in the feedback path. At the end of Φ_2 phase, the total charge stored in the upper side capacitors, Q_2, is as follows:

$$Q_2 = C_{S1}V_{DAC+} + \Delta V_{cm}C_{S2} + (V_{out+} - V_{cm})C_F. \tag{4}$$

Hence, by using the charge conservation law for Q_1 and Q_2, we have:

$$V_{out+} = \frac{C_{S1} + C_{S2}}{C_F}V_{in+} - \frac{C_{S1}}{C_F}V_{DAC+} + V_{cm}. \tag{5}$$

Therefore, the output CM voltage is V_{cm} without using a separate CMFB circuit and the input CM voltage variations

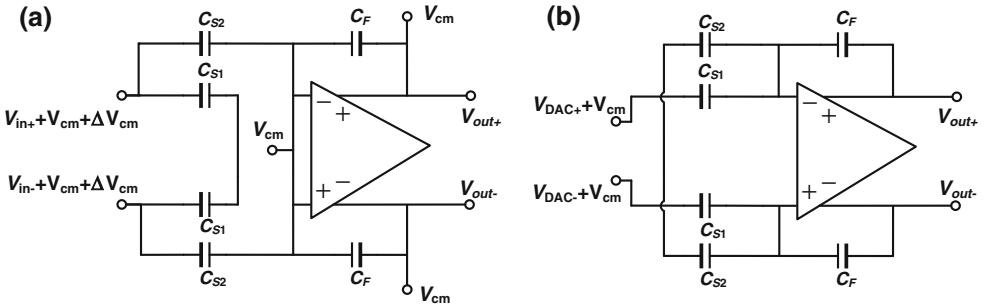

Fig. 3 Proposed MDAC in **a** sampling and **b** amplifying phases

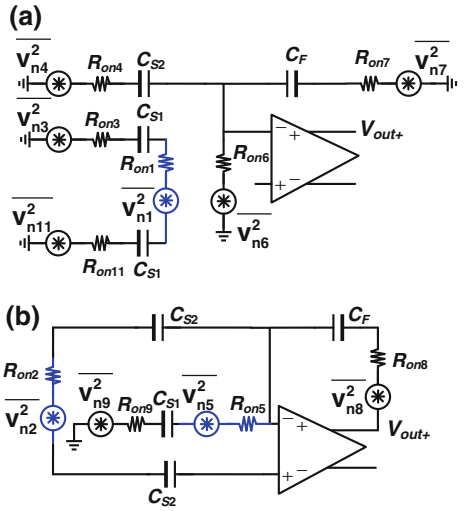

Fig. 4 Modeling the thermal noise of switches for the proposed MDAC in **a** sampling and **b** amplification phases

cannot affect it. In other words, an equivalent CMFB circuit is inherently implemented in the proposed MDAC.

For $C_{S1} = C_{S2} = C_F = C$, in this scheme similar to the conventional CFA structure, the signal sees a gain of two, while the gain of the DAC signal is one. The feedback factor, β, for the proposed MDAC by neglecting the amplifier input parasitic capacitance is given by:

$$\beta = C_F/(C_{S1} + C_{S2} + C_F), \tag{6}$$

where for the both conventional CFA and CNFA structures, it is as follows:

$$\beta_{CFA,CNFA} = C_F/(C_S + C_F). \tag{7}$$

In the CFA structure, $C_S = C_F$ and thus $\beta_{CFA} = 1/2$, while for the CNFA structure, $C_S = 2C_F$ and $\beta_{CNFA} = 1/3$. Therefore, the feedback factor of the proposed MDAC is equal to the β_{CNFA} and it is smaller than β_{CFA}.

Indeed, the proposed MDAC is achieved by using the floating sampling in the CNFA structure where the sampling capacitors are divided into two same parts, and hence, it is insensitive to the input CM voltage variation.

3.2 Switches thermal noise

In the following, the input-referred thermal noise for the proposed MDAC is calculated. The equivalent noise model for switches of the proposed MDAC in sampling and amplification phases are depicted in Fig. 4 where the single-ended structure is considered for simplicity. The thermal noise of switches is modeled by their on-resistance, R_{on}, and a voltage source with a power spectral density of $4kTR_{on}$. Here, k is the Boltzmann constant and T is the absolute temperature. By considering Fig. 4(a), the total noise power stored in the capacitors at the sampling phase is given by [14]:

$$\overline{V^2_{CS1,\Phi1}} = \frac{kT}{C_{S1}}, \quad \overline{V^2_{CS2,\Phi1}} = \frac{kT}{C_{S2}}, \quad \overline{V^2_{CF,\Phi1}} = \frac{kT}{C_F}. \tag{8}$$

In the next phase, Φ_2, by considering Fig. 4(b), similarly we have:

$$\overline{V^2_{CS1,\Phi2}} = \frac{kT}{C_{S1}}, \quad \overline{V^2_{CS2,\Phi2}} = \frac{kT}{C_{S2}}, \quad \overline{V^2_{CF,\Phi2}} = \frac{kT}{C_F}. \tag{9}$$

Therefore, the total output noise power of the proposed MDAC due to the switches thermal noise is given by:

$$\overline{V^2_{n\_out,sw}} = \frac{2kT}{C_F} + \frac{2kT}{C_{S1}}\left(\frac{C_{S1}}{C_F}\right)^2 + \frac{2kT}{C_{S2}}\left(\frac{C_{S2}}{C_F}\right)^2. \tag{10}$$

The closed-loop signal gain for the proposed MDAC is $(C_{S1} + C_{S2})/C_F$. So, the input-referred thermal noise power due to the switches is obtained as:

$$\overline{V^2_{n\_in,sw}} = 2kT\left(\frac{C_F + C_{S1} + C_{S2}}{(C_{S1} + C_{S2})^2}\right). \tag{11}$$

For $C_{S1} = C_{S2} = C_F = C$, we have:

$$\overline{V^2_{n\_in,sw}} = 1.5 \times kT/C. \tag{12}$$

The input-referred thermal noise power of the conventional CFA and CNFA MDACs in single-ended structure is kT/C and $1.5 \times kT/C$, respectively [15]. Therefore, the noise contribution of the proposed MDAC due to its switches is 1.5 times higher than the conventional

CFA MDAC and it is similar to the CNFA one. For the same thermal noise contribution, the proposed and CNFA MDACs need the capacitors of 1.5 times larger than the CFA structure. The total capacitor used in the fully-differential CFA MDAC is $4C$ and for the same noise contribution, the proposed and CNFA MDACs need the total capacitor of $6 \times (1.5 \times C) = 9C$.

3.3 Circuit non-ideality effects

To analyze the proposed MDAC in a more realistic situation, some secondary effects that cannot be neglected in the real implementations are considered here.

The finite open-loop DC gain of the amplifier, A, its input parasitic capacitance, C_P, and capacitors mismatch considered as $C_{S1} = (1 + \varepsilon_1)C_F$ and $C_{S2} = (1 + \varepsilon_2)C_F$ can deviate the transfer function of the stage from (5). By considering these effects, it can be easily shown that the relation (5) will be changed as:

$$V_{out+} = \overbrace{\frac{1}{1+\frac{1}{A}\left(3+\varepsilon_1+\varepsilon_2+\frac{C_P}{C_F}\right)}}^{\alpha} \times ((2+\varepsilon_1+\varepsilon_2)V_{in+} - (1+\varepsilon_1)V_{DAC+} + V_{cm}). \quad (13)$$

So, the output CM voltage is affected by α. In derivation of (13), the parasitic capacitance of the floating switches, S_1 and S_2 in Fig. 2, are neglected. It is worth mentioning that with typical values of $\varepsilon_1 = \varepsilon_2 = 0.1$ % (10-bit resolution), $C_P = 20$ % $\times$ C_F and $A = 70$ dB (open-loop gain for 10-bit resolution), the output CM voltage will be $0.9999 \times V_{cm}$. As a result, the output CM voltage is determined with a sufficient accuracy.

The switches induced offset voltages are problematic in conventional PD pipeline architectures. If no compensation is used, the offset will quickly accumulate and saturate the usable signal swing due to the large interstate gain of the pipeline. Interestingly, in the proposed MDAC, by using the bottom-plate sampling, only the signal independent charge injection is important and it will appear as a CM variation in the amplifying phase. In conventional MDACs, the switches induced CM variation is cancelled through the CMFB circuit, but the proposed MDAC does not have any CMFB circuit. Fortunately, in the pipelined ADCs with the proposed MDAC, every stage output CM variations will be omitted with the next stage MDAC and will not grow along the pipeline. So, the effect of the signal independent charge injection in the proposed MDAC is alleviated similar to the conventional one.

In the proposed MDAC circuit, the on-resistance of the switches controlled by Φ_{2a} phases adds a series resistance to the amplifying network in comparison with the conventional one resulting in the speed reduction. So, these switches should be more carefully designed to prevent any speed degradation.

In the pipelined ADC with redundancy, the amplifier offset voltage can usually be tolerated with digital correction. At the output of the proposed MDAC, the offset voltage of the amplifier will be appeared like the conventional MDACs. So, to meet the tolerable offset range, the proposed inverter should be laid out carefully like the conventional amplifiers used in the pipelined ADCs.

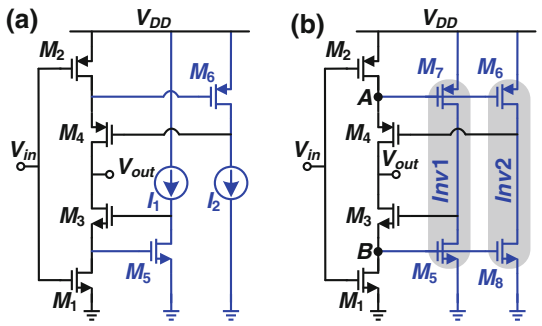

Fig. 5 **a** Regulated cascode inverter and **b** proposed gain-boosting inverter

4 Proposed gain-boosting inverter

4.1 Circuit description

Figure 5(a) shows the inverter presented in [9]. Transistors M_1–M_4 make the cascode inverter and transistors M_5 and M_6 which are biased with I_1 and I_2 current sources regulate the drain-source voltage of M_1 and M_2, respectively. By using this structure, the boosted small-signal output resistance, R_{out1}, of the inverter is given by:

$$R_{out1} \approx (g_{m3}r_{o3}r_{o1}g_{m5}(r_{o5}||r_1))||(g_{m4}r_{o4}r_{o2}g_{m6}(r_{o6}||r_2)), \quad (14)$$

where g_{mi} is the transconductance and r_{oi} is the output resistance of the respective transistor M_i (for $i = 1$–6) while r_1 and r_2 are the output resistance of the current sources I_1 and I_2, respectively.

Figure 5(b) illustrates the proposed inverter which does not need any bias voltage. In this scheme, extra driving transistors are adapted instead of current sources I_1 and I_2 in Fig. 5(a). Current sources I_1 and I_2 are replaced with driving transistors of M_7 and M_8 by connecting their gates to the nodes A and B, respectively. As it is clear, the small-signal variations in nodes A and B are at the same direction. So, M_5 with M_7 and M_6 with M_8 also work as the simple inverters. Due to the V_{AB} voltage difference between the gates of M_7–M_5 and M_6–M_8 transistors, these inverters can be biased with a small static current. As a result, in the

proposed inverter, the gain-boosting is realized using two simple inverters named *Inv*1 and *Inv*2 in Fig. 5(b).

The low frequency voltage gain, A_{v0}, of the proposed inverter can be obtained as follows:

$$A_{v0} \approx G_m R_{out2}, \tag{15}$$

where $G_m = g_{m1} + g_{m2}$ and R_{out2} is the inverter output resistance which is given by:

$$R_{out2} \approx (g_{m3} r_{o3} r_{o1} A_{Inv1}) || (g_{m4} r_{o4} r_{o2} A_{Inv2}). \tag{16}$$

To obtain A_{Inv1} and A_{Inv2}, firstly the relation of V_A and V_B should be derived resulting in:

$$k = \frac{V_A}{V_B} = \frac{g_{m4} r_{o4} + g_{m6}(r_{o6} || r_{o8})(g_{m4} - g_{m3})}{g_{m3} r_{o3} + g_{m5}(r_{o5} || r_{o7})(g_{m3} - g_{m4})}. \tag{17}$$

Therefore we have,

$$\begin{aligned} A_{Inv1} &= (g_{m5} + k g_{m7})(r_{o5} || r_{o7}), \\ A_{Inv2} &= (k g_{m6} + g_{m8})(r_{o6} || r_{o8}). \end{aligned} \tag{18}$$

As is seen, the gain-boosting ability of the proposed inverter as well as its output resistance is increased compared to the conventional regulated cascode inverter.

4.2 Class AB scheme

As shown in Fig. 6(a), to reduce the static current, a class AB scheme is utilized in the proposed inverter. This scheme can be easily employed in switched-capacitor circuits where the amplifier is idle at half of the clock cycle such as the pipelined ADCs. Capacitors C_{B1} and C_{B2} work as the voltage level shifters. In Φ_1 phase, when the inverter is idle, the capacitors are charged with the difference of input CM voltage and appropriate bias voltages (V_{B1} and V_{B2} in Fig. 6(a)) while in the next phase, the gate voltage of the input transistors are level shifted versus the input signal CM voltage. Therefore, the gate voltage of the transistors M_1 and M_2 follows the input signal. The equivalent transconductance, G_m, of the inverter is given by:

$$G_m = \frac{C_{B1}}{C_{B1} + C_{P1}} g_{m1} + \frac{C_{B2}}{C_{B2} + C_{P2}} g_{m2}, \tag{19}$$

where C_{P1} and C_{P2} are the parasitic capacitances at the gate of M_1 and M_2 transistors, respectively. So, the equivalent transconductance is decreased due to the charge sharing at the gates of M_1 and M_2. In order to reduce the impact of parasitic capacitances, the class AB capacitors are chosen sufficiently larger than the parasitic capacitances. The bias voltages V_{B1} and V_{B2} are generated by the circuit shown in Fig. 6(b) which works only in the idle phase of the inverter and turns off in the next clock phase using S_1 switch.

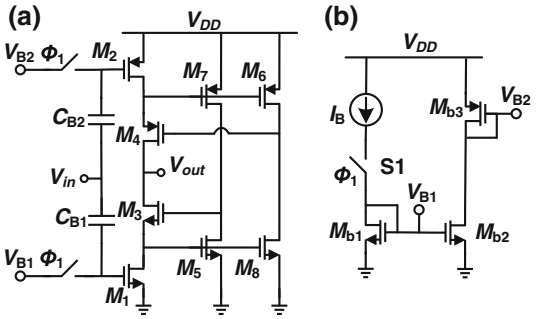

Fig. 6 **a** Class AB scheme of the proposed inverter and **b** bias circuit

4.3 Output swing

In the proposed class AB inverter, V_{B1} and V_{B2} are chosen such that the gate-source voltage of input transistors is slightly greater than their threshold voltage, V_{TH}. The input signal CM voltage, V_{cm}, of $0.5V_{DD}$ is considered and all of the transistors are sized to work in the saturation region. The minimum and maximum output voltages are given by:

$$V_{out,min} = V_{eff3} + V_{GS5,8} = V_{eff3} + V_{eff5,8} + V_{TH5,8}, \tag{20}$$

$$\begin{aligned} V_{out,max} &= V_{DD} - \left(V_{eff4} + V_{SG6,7}\right) \\ &= V_{DD} - \left(V_{eff4} + V_{eff6,7} + \left|V_{TH6,7}\right|\right), \end{aligned} \tag{21}$$

where $V_{eff} = (V_{GS} - V_{TH})$ is the transistor overdrive voltage. As is seen from the relations (20) and (21), the output voltage range of the proposed inverter is reduced by $(V_{TH5,8} + V_{TH6,7})$ in comparison with the simple cascode inverter. As mentioned in [16], by increasing the transistor channel length from the minimum value (L_{min}), the threshold voltage is firstly increased and then it is decreased due to the short channel effects in nano-meter CMOS technologies. In the proposed inverter, to prevent the output swing reduction and preserving saturation region for gain-boosting transistors, the channel length of transistors M_5–M_8 are chosen larger than L_{min} to have low threshold voltage. In this case, an appropriate output voltage swing will be achieved in low supply voltages. For example in 90 nm CMOS technology, for minimum channel length transistors, V_{TH} is in the order of 0.25–0.3 V while it is decreased to 0.12–0.15 V for the channel length of $4L_{min}$.

4.4 Input-referred thermal noise

The total input-referred thermal noise of the proposed inverter can be calculated as follows:

$$\overline{V_{nt}^2} = \sum_{i=1}^{8} d_i \overline{V_{ni}^2}, \tag{22}$$

where $\overline{V_{ni}^2} = 4kT\gamma / g_{mi}$ is the thermal noise of transistor M_i and it is modeled as a series voltage source with the gate terminal and d_i's are given by:

$$d_1 = \left(\frac{g_{m1}}{g_{m1}+g_{m2}}\right)^2, \quad d_2 = \left(\frac{g_{m2}}{g_{m1}+g_{m2}}\right)^2,$$
$$d_3 = \left(\frac{g_{m8}r_{o1} - g_{m6}r_{o2}}{g_{m6}r_{o1}r_{o2}(g_{m1}+g_{m2})}\right)^2, \quad d_4 = \left(\frac{g_{m7}r_{o2} - g_{m5}r_{o1}}{g_{m5}r_{o1}r_{o2}(g_{m1}+g_{m2})}\right)^2,$$
$$d_5 = d_7 = \left(\frac{(g_{m8}r_{o1} - g_{m6}r_{o2})g_{m5,7}(r_{o5}||r_{o7})}{g_{m6}r_{o1}r_{o2}(g_{m1}+g_{m2})}\right)^2,$$
$$d_6 = d_8 = \left(\frac{(g_{m7}r_{o2} - g_{m5}r_{o1})g_{m6,8}(r_{o6}||r_{o8})}{g_{m5}r_{o1}r_{o2}(g_{m1}+g_{m2})}\right)^2. \tag{23}$$

From (23), it is concluded that the input transistors M_1 and M_2 are the dominant noise sources in the proposed inverter as well as the simple cascode circuit. So, the noise performance of both cascode inverters is the same. Hence, the total input-referred thermal noise of the proposed inverter is approximately given by:

$$\overline{V_{nt}^2} \approx \overline{V_{n1}^2} + \overline{V_{n2}^2} = \frac{4kT\gamma}{g_{m1}+g_{m2}}, \tag{24}$$

where γ is the excess noise factor in short channel transistors.

Now we can calculate the effect of the inverter noise in the proposed MDAC circuit. The input-referred thermal noise power of the proposed differential MDAC due to the inverter thermal noise is obtained as:

$$\overline{V_{n\_in,inv}^2} = \overline{V_{nt}^2} \times B_n, \tag{25}$$

where B_n is the noise bandwidth and it is given by [14, 15]:

$$B_n = \frac{\pi}{2} \times \frac{G_m}{2\pi C_{Load}} \times \beta,$$
$$C_{Load} = \left(C'_{S1} + C'_{S2}\right) + \beta(C_{S1} + C_{S2}), \tag{26}$$

where C'_{S1} and C'_{S2} are the next stage sampling capacitors. With a capacitor scaling factor of two in the pipelined ADC stages ($C_{S1} = C_{S2} = C_F = 2C'_{S1} = 2C'_{S2} = C$), the input-referred thermal noise power of the proposed MDAC in the single-ended structure due to the inverter's thermal noise will be as:

$$\overline{V_{n\_in,inv}^2} = 0.2\gamma kT/C. \tag{27}$$

So, the total input-referred noise power of the proposed PD MDAC using (12) and (27) is obtained as:

$$\overline{V_{n,tot}^2} = 2\left(\overline{V_{n\_in,sw}^2} + \overline{V_{n\_in,inv}^2}\right) = (3 + 0.4\gamma)kT/C. \tag{28}$$

5 Circuit implementation and simulation results

5.1 MDAC and inverter

HSPICE simulation results are provided to evaluate the performance of the proposed inverter based MDAC using a 90 nm CMOS technology with 1 V power supply. It is designed for the first stage of a 10 bit resolution pipelined ADC with 1.5-bit MDACs. To have sufficient capacitors matching and considering the total input-referred thermal noise power given in (28), the MDAC capacitors of $C = 0.8$ pF are selected. As mentioned before, the capacitors scaling factor of two is considered in the pipelined ADC stages. So, the load capacitance of the inverter is 1.33 and 0.8 pF in open- and closed-loop simulations, respectively, corresponding to an effective load capacitance of $C_{Load} = 1.33$ pF in both simulations. The level shifter capacitors at the inverter input have a negligible effect on C_{Load}, because they are in series with the input transistors gate parasitic capacitance.

Table 1 Device parameters used in the simulation of the proposed inverter

Parameters	Values
$(W/L)_{1,2}$ (μm)	9 × 7/0.09
$(W/L)_{3,4}$ (μm)	10 × 9/0.09
$(W/L)_{5,8}$ (μm)	5 × 3/0.36
$(W/L)_{6,7}$ (μm)	5 × 9/0.36
$C_{B1,2}$, pF	2

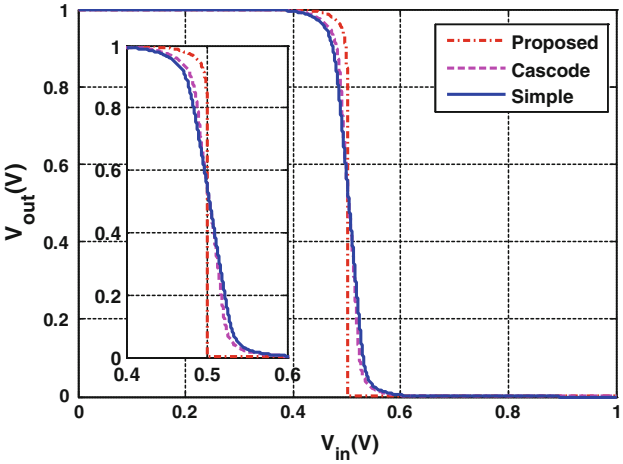

Fig. 7 Simulated VTC of the simple, cascode, and proposed inverters

The device parameters of the simulated inverter are summarized in Table 1. The voltage transfer curve (VTC) of the simple inverter and cascode one in comparison with the proposed inverter is plotted in Fig. 7. For VTC simulation, the inverters are derived in the open-loop configuration with the load capacitance of C_{Load}. A ramp signal with a height of V_{DD} is applied to the input of the inverters. As shown in this figure, a sharp transient region for VTC in the proposed inverter is achieved. With biasing the inverter input at $0.5V_{DD}$, the transition region of VTC is used for

amplification. Thus, the proposed inverter has a large gain in comparison with two other inverters. The simulated frequency response of the proposed inverter for different process corner cases and temperature variations is shown in Fig. 8.

The large signal transient response of the proposed MDAC to a step input with 0.5 V differential height for different process corner cases and temperature variations is illustrated in Fig. 9(a). To compare the proposed MDAC with the conventional ones, their step response with the same condition as Fig. 9(a) is presented in Fig. 9(b) while all of them employ the proposed inverter. Figure 9(b) shows that the proposed MDAC has the same performance as the CNFA MDAC and slightly worse than the CFA structure as theoretically expected. Table 2 summarizes the simulation results of the proposed MDAC using the new inverter where the MDAC total harmonic distortion (THD) is simulated for 1 *Vpp* differential output swing.

The first stage of the pipelined ADC has the most stringent performance requirements. In an *N*-bit ADC, for the output allowable error of less than half LSB of the remaining stages resolution, the amplifier DC gain, *A*, and unity gain bandwidth, f_u, requirements are:

$$A > \frac{2^N}{\beta}, \quad f_u > \frac{N \times F_S \times Ln(2)}{\pi \times \beta}. \tag{29}$$

So, the required DC gain and unity gain bandwidth of the proposed MDAC and CNFA structure are higher than CFA specifications, because these two structures have a smaller feedback factor compared to the CFA MDAC. As shown in Table 2, the proposed MDAC and inverter satisfy the specifications of a 10 bit 100 MS/s pipelined ADC with low power consumption ($A > 69.7$ dB and $f_u > 661.9$ MHz).

5.2 A prototype pipelined ADC

A 1.5-bit/stage PD pipelined ADC is designed for high-speed applications using the proposed MDAC and inverter. The front-end sample and hold amplifier is eliminated using time constant matching method in the first stage to reduce the ADC power consumption. The core pipeline structure consists of eight 1.5-bit stages followed by a 2-bit back-end flash ADC. All of the 1.5-bit stages use the proposed MDAC with gain-boosting inverter. The simulated pipeline ADC architecture is shown in Fig. 10.

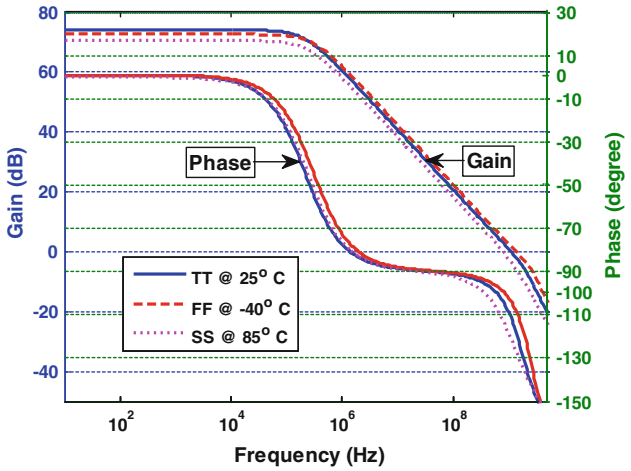

Fig. 8 Simulated frequency response of the proposed inverter

Table 2 Simulation results of the proposed MDAC

Parameters	TT at 25 °C	SS at 85 °C	FF at −40 °C
DC gain (dB)	74.1	70.5	72.6
Unity gain bandwidth (GHz)	1.17	0.84	1.39
Phase margin (°)	67	64	72
Power (mW)	0.71	0.58	0.81
THD (dB) at $f_{in} = 50$ MHz	−69.04	−60	−70.23
Settling time with 0.1 % error (ns)	3.86	4.39	3.69
Input referred thermal noise of inverter at 100 kHz ($V/\sqrt{Hz}$)	5.66×10^{-9}	6.1×10^{-9}	5.1×10^{-9}

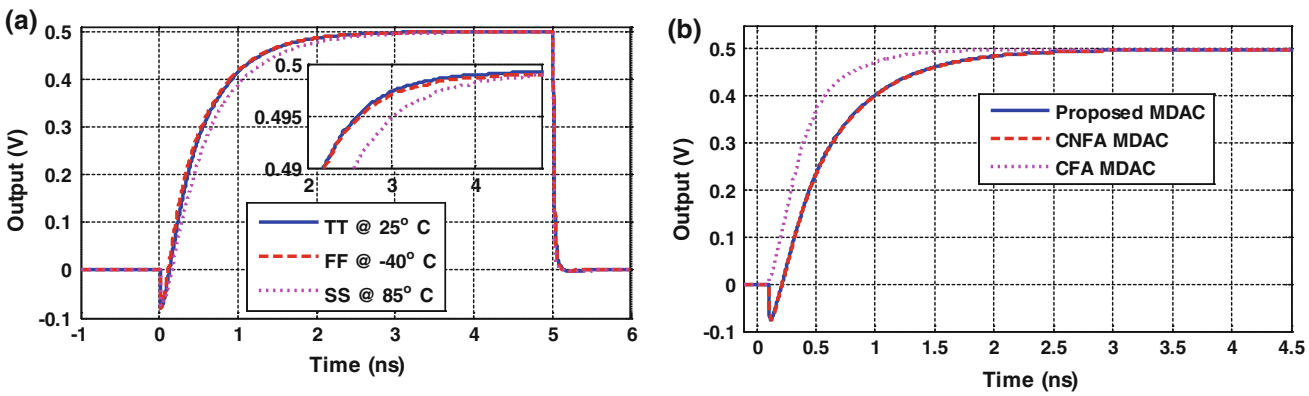

Fig. 9 Transient simulation results of **a** the proposed and **b** CFA and CNFA MDACs

As shown in Fig. 11(a), a capacitively coupled comparator [17] is employed in the stages sub-ADC. In this structure, $C_{in} = 80$ fF and $C_{ref} = 20$ fF are used for $\pm 0.25 V_{ref}$ realization. Moreover, because of redundancy in ADC stages, a simple dynamic latch shown in Fig. 11(b) is employed. The input offset voltage for this latch is measured using Monte-Carlo simulations. Mismatch of the transistors is modeled with their dimensions W and L as:

$$\sigma_{Vth} = \frac{A_{VTH}}{\sqrt{WL}}, \quad \sigma_{\beta} = \frac{A_{\beta}}{\sqrt{WL}}, \tag{30}$$

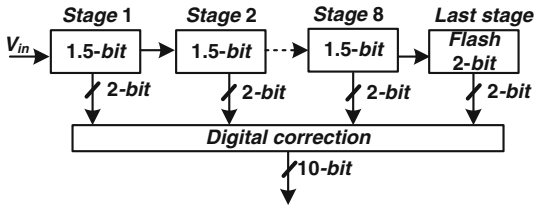

Fig. 10 Architecture of the simulated pipelined ADC

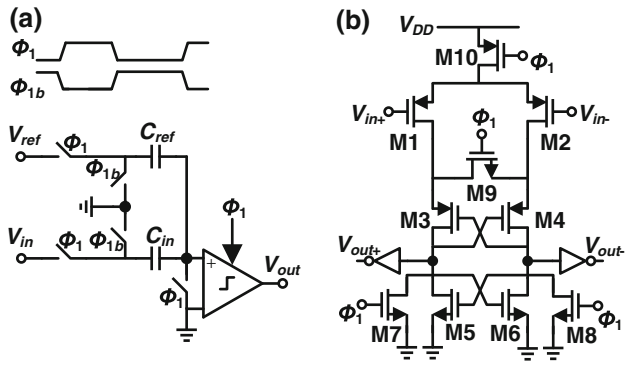

Fig. 11 **a** Comparator architecture and **b** dynamic latch

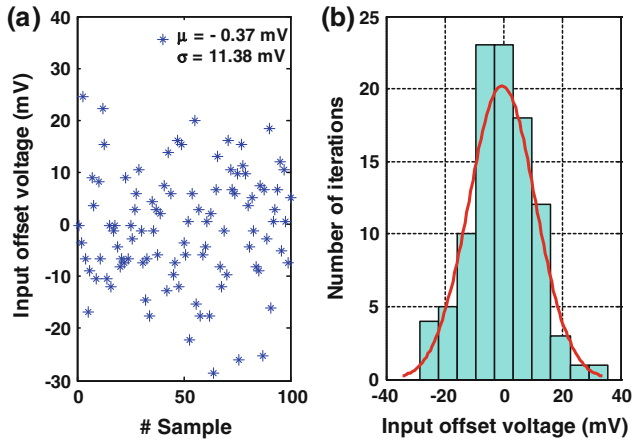

Fig. 12 **a** Monte-Carlo simulation results of the latch input offset voltage and **b** the achieved histogram

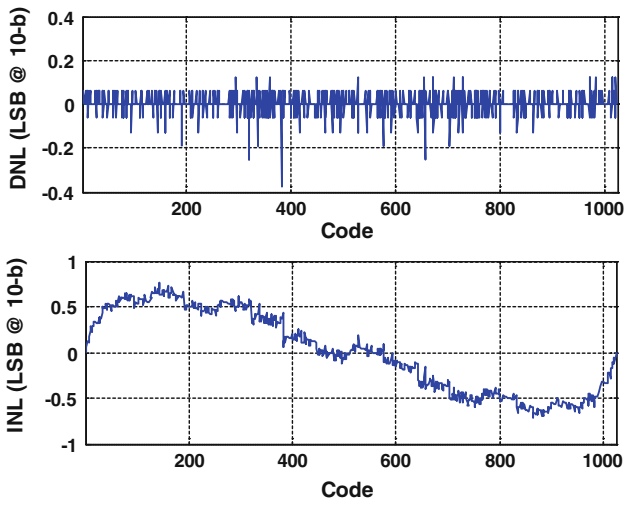

Fig. 13 Simulated DNL and INL

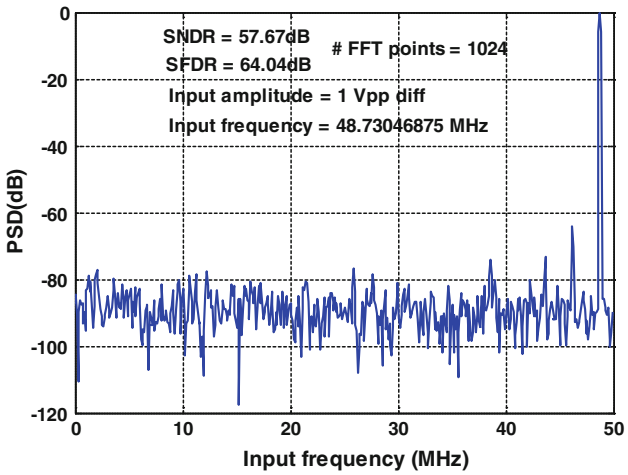

Fig. 14 Output spectrum of the simulated ADC by including the circuit noise

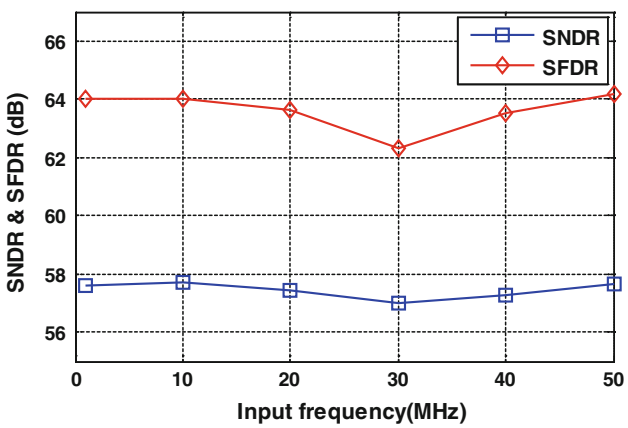

Fig. 15 Simulated SNDR and SFDR versus the input signal frequency

where A_{VTH} and A_{β} are the Pelgrom's coefficients for the threshold voltage and current factor, respectively [18]. In this technology, $A_{VTH} = 3.5$ mV × μm and $A_{\beta} = 1.07$ % μm were considered and a Monte-Carlo simulation with 100 iterations was performed. The input offset voltage of the simulated comparator in different iterations and the resulting histogram are depicted in Fig. 12(a), (b), respectively. The standard deviation (σ) and the mean value (μ) for the input-referred offset voltage are obtained as 11.38 and −0.37 mV, respectively. Therefore, the offset voltage (3σ) of the simulated latch is 34.15 mV which is tolerable in the 1.5-bit stage pipelined ADC with $V_{ref} = 0.5$ V ($3\sigma < V_{ref}/4$).

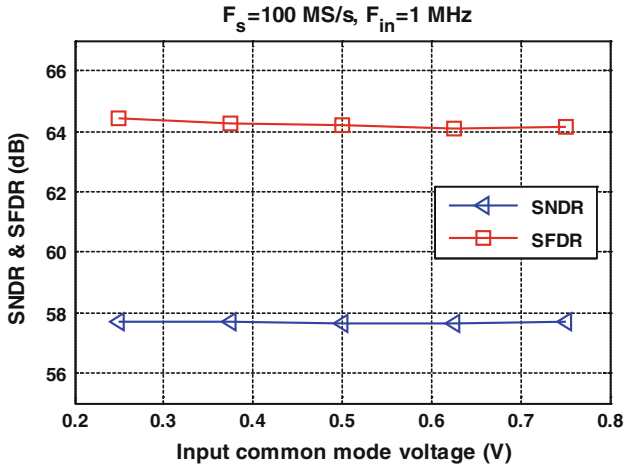

Fig. 16 Simulated SNDR and SFDR versus the input CM voltage for full-scale input signal ($V_{pp\text{-}diff} = 1$ V)

The sampling capacitors used in the first stage are 0.8 pF and they are scaled down with a factor of two for the next four stages and the rest stages use 0.1 pF sampling capacitor.

The power consumption for the simulated ADC is 5.91 mW from a 1 V power supply. The maximum differential input signal is 1 V peak to peak. The simulated differential nonlinearity (DNL) and integral nonlinearity (INL) errors are shown in Fig. 13. In these simulations, the comparators offset voltage and amplifiers' imperfections are modeled at the system level and a slowly varying ramp is used as the

Table 3 Performance comparison of the simulated ADC with several recently reported pipelined ADCs

References	Tech. (μm)	Resolution (bit)	V_{DD} (V)	f_S (MS/s)	SNDR (dB)	SFDR (dB)	DNL (LSB)	INL (LSB)	Power[a] (mW)	FoM (fJ/conversion-step)
This work[b]	0.09	10	1	100	57.6	64	0.37	0.76	5.91	95
[6]	0.09	9.4	1.2	50	49.4	–	0.38	1.29	1.44	119
[7]	0.18	10	1.8	50	58.2	66	0.35	0.8	9.9	300
[8]	0.09	12	1.2	30	65.2	–	0.82	1.25	2.95	66
[12]	0.18	10	1.8	60	53.6	64.8	0.73	1.44	13	554
[19]	0.09	10	1	30	55	–	0.81	1	4.5	98
[20]	0.09	10	1.2	500	56	–	0.4	1	55	213
[21]	0.18	10	1.8	50	58	72.8	0.39	0.81	12	370
[22]	0.18	10	1.8	50	58	74	0.4	0.7	9.2	290
[23][b]	0.09	10	1	100	64	74	0.12	0.3	27	210
[24][b]	0.09	10	1	200	58.5	–	–	–	30.9	220
[25]	0.35	10	1.5	30	58.2	66.3	0.36	0.42	38.6	1,937
[26]	0.13	10	1.2	40	57.25	77.65	0.2	0.3	15.6	655
[27][b]	0.065	10	1.2	100	59.3	69.3	–	–	12.7	168
[28]	0.13	10	1.2	60	58.77	67.05	0.6	0.61	18	423
[29][b]	0.065	10	1.2	100	59	67.4	–	–	21.4	294
[30]	0.045	10	1.1	120	55.6	70.6	0.44	0.75	52	880
[31][b]	0.13	10	1	40	56.04	64.4	<1	<1	3.9	188
[32][b]	0.18	10	1.8	250	61.8	78.2	–	–	30	140
[33]	0.09	10	1.2	320	53	66	0.96	1.75	24	205
[34]	0.13	10	1.2	50	59	70.8	–	–	43.2	1,200
[35][b]	0.13	10	1.2	100	58.8	70.4	–	–	5.9	83
[36][b]	0.18	11	1.8	40	65	78	–	–	21	361
[37]	0.09	8	1.2	60	44.2	60	0.54	0.77	5.9	742

[a] For fabricated ADCs only core circuits (excluding the reference voltage buffers) power is considered

[b] Simulation results

input signal. The absolute peak DNL and INL errors are 0.37 and 0.76 LSB, respectively.

The ADC output spectrum for the full scale input signal at frequency of 48.7 MHz is shown in Fig. 14. The total thermal noise for ADCs circuit is calculated using (28) for each stage and added to the circuit simulation results manually, and hence, the output spectrum includes the total circuit noise. The achieved SNDR and SFDR with 1,024 FFT points at a 48.73046875 MHz input frequency are 57.7 and 64 dB, respectively.

Figure 15 plots the simulated SNDR and SFDR versus the input signal frequency showing approximately the same dynamic performance for the whole input frequencies. The ADC SNDR and SFDR versus the input CM voltage are shown in Fig. 16. Even under large input CM variation, the proposed pipelined ADC has a stable performance. This result demonstrates the effectiveness of the proposed scheme for MDAC.

The achieved performance of the simulated pipelined ADC is summarized in Table 3 and the comparison with several recently reported pipelined ADCs is performed using the following figure of merit (FoM):

$$\text{FoM} = \frac{\text{Power}}{2^{ENoB} \times f_S}, \tag{31}$$

where Power and f_S refer to the ADC power consumption and sampling frequency, respectively, and *ENoB* is the ADC effective number of bits. To have a fair comparison, only core ADC circuits' power (excluding the power consumption in the buffer circuits of the reference voltages) is considered. It should be noted that although the reported results for the presented pipelined ADC are based on the HSPICE simulation results while most of the other ADCs are implemented on chip, but its outstanding *FoM* verifies the performance of the proposed PD MDAC with gain-boosting class AB inverter as good candidates to be employed in low power and high speed pipelined ADCs.

6 Conclusions

A PD MDAC with a power-efficient class-AB gain-boosting inverter has been proposed for pipelined ADCs. The MDAC circuit is insensitive to the input CM voltage variations. To verify the usefulness of the proposed techniques, a prototype 10 bit 100 MS/s pipelined ADC has been implemented in a 90 nm CMOS technology where all stages dissipate the same amount of static power. The simulation results clearly demonstrate the power efficiency of the proposed inverter and PD MDAC topology and its potential for the design of low power and high speed pipelined ADCs in nano-meter CMOS technologies.

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