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RESEARCH ARTICLE

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Shifting the sampled input signal in successive approximation register analog-to-digital converters to reduce the digital-to-analog converter switching energy and area

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Summary

In this paper, a switching scheme is presented to reduce the capacitive digital-to-analog converter (DAC) switching energy, area, and the number of switches in successive approximation register (SAR) analog-to-digital converters (ADCs). In the proposed DAC switching method, after a few most significant bits (MSBs) decision, the sampled differential input signal is shifted into two special regions where the required DAC switching energy and area is less than the other regions. This technique can be utilized in most of the previously reported DAC switching schemes to further reduce the capacitive DAC switching energy and area. The conventional and two recently presented DAC switching techniques are utilized in the proposed SAR ADC to evaluate its usefulness.

KEYWORDS

charge-redistribution digital-to-analog converters (DACs), DAC switching energy, Successive approximation register (SAR) analog-to-digital converters (ADCs), switched-capacitor circuits

1 | INTRODUCTION

Successive approximation register (SAR) analog-to-digital converters (ADCs) generally consume low power in medium resolutions and bandwidths,[1–8] and this property makes them suitable for an extensive variety of applications specifically in energy-limited applications,[1] multichannel neural recording systems,[2] wearable sensors,[3] and low energy wireless sensor network chips.[4] In charge-redistribution SAR ADCs, the power consumption of the capacitor switching in the digital-to-analog converter (DAC) usually is dominant.[1–5,9–15] Recently, several techniques have been presented to reduce the DAC switching energy and capacitor size.[1–26]

In Zhang et al.,[1] a hybrid DAC consisting of most significant bits (MSBs) with a capacitive DAC (CDAC) and *least significant bits* (LSBs) with an MOS DAC is utilized to reduce the overall DAC area and switching energy. In Mao et al.,[3] a multisegmentation DAC with a hybrid switching scheme is proposed to reduce the total number of the unit capacitors. A two-step architecture with an MSB capacitor splitting and monotonic switching scheme is used in Ding et al.[5] to reduce the total capacitance size and DAC area. The MSB-splitting DAC and the LSB-down techniques are combined in Wang and Wu[6] for switching energy reduction. In Zhou et al.,[7] a two-step quantization results in both switching energy and capacitor area reductions. Using a reference-free technique to avoid the static power dissipation of the on-chip reference generation and also a common-mode based charge recovery switching method reduces the switching energy in Zhu et al.[8] The binary-window DAC switching scheme is proposed in Chung et al.[24] to linearize

the SAR ADC performance effectively by using a small sampling capacitor, and hence, with reduced area and power consumption.

In other methods, various techniques such as capacitor splitting,[12] closed-loop charge recycling,[15] charge-sharing,[14,16,20] sub-DAC merged switching,[19] and segmented SAR ADC[23] are used to reduce the DAC switching energy and area. However, except,[11,17,18] any solution is not intended to reduce the number of the required switches in the DAC capacitor array. The large number of switches occupies more area, and in some cases, a complicated control logic is required. Also, in some designs, owing to the large number of switches, the power consumption of the digital control circuit is increased.[11]

In this paper, a new SAR ADC is proposed, which exploits the shifting of the sampled input signal to reduce the capacitive DAC switching energy, area, the required number of switches. Most of the previously reported energy efficient DAC switching techniques can be utilized in the proposed SAR ADC to further reduce the switching energy and DAC area. The rest of the paper is organized as follows. In Section 2, the main idea, the structure of the proposed SAR ADC and the application of the conventional and two recently reported DAC switching schemes in the proposed ADC are presented. The analysis of the proposed SAR ADC is provided in Section 3 with some detailed discussions and comparisons with several other SAR ADCs. Finally, Section 4 concludes the paper.

2 | PROPOSED SAR ADC

2.1 | Main idea

In an N-bit SAR ADC, if we divide the differential input signal range of $-V_{Ref} \le V_{in} = V_{in+} - V_{in-} \le V_{Ref}$ into $2^{(k+1)}$ equal regions, the $(k+1)$ MSBs will be different in all these regions and the remained $(N-k-1)$ LSBs are repeated in the regions where $0 \le k \le N-1$. So, by shifting the sampled differential input signal by $V_{Ref}/2^k$ steps in order to move from one region into the other regions, the LSBs will be the same and only $(k+1)$ MSBs will be changed. Figure 1 shows an example of this idea where the differential input signal range is divided into eight regions. As it is seen, the

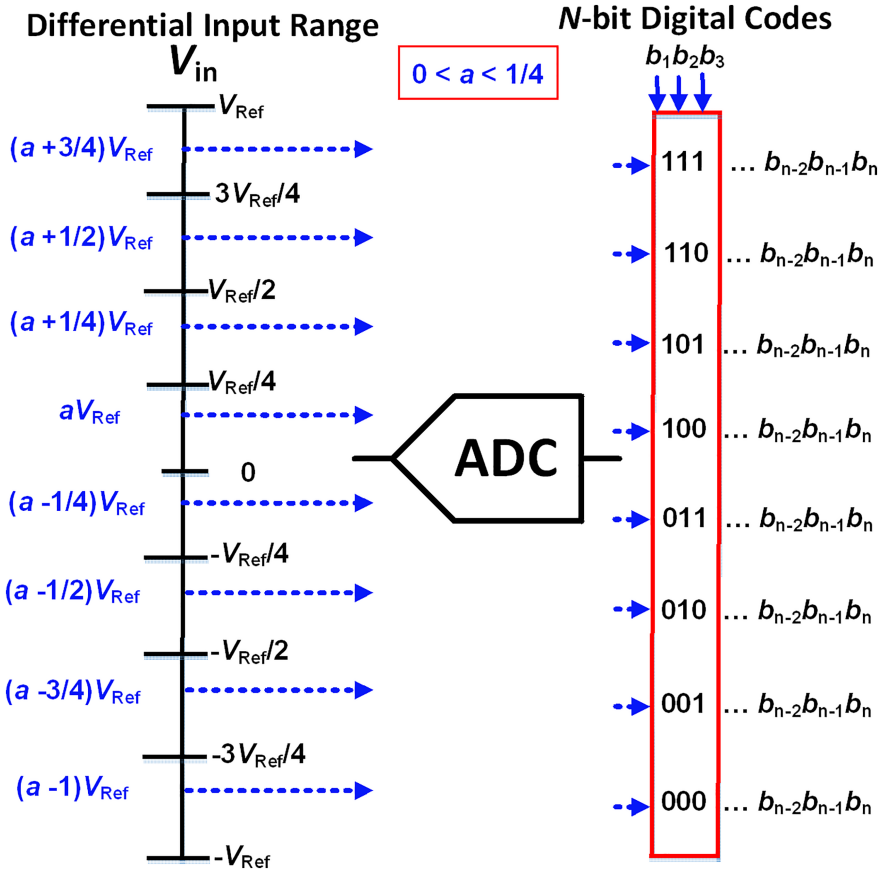

FIGURE 1 The differential input signal range of an N-bit ADC and its corresponding output bits ($k = 2$) [Colour figure can be viewed at wileyonlinelibrary.com] [Colour figure can be viewed at wileyonlinelibrary.com]

three MSBs are different in all these regions, and the remaining LSBs are the same when the input signal is shifted by $V_{Ref}/4$ steps. On the other hand, the DAC switching energy depends on the output digital codes.[7,10,12,16] So, to extract the digital output codes, the required DAC switching energy in some regions of the input signal is higher than the other regions. Therefore, by shifting the sampled input signal to special regions where the required DAC switching energy is less than the other regions, the total DAC switching energy is reduced. In this paper, this property of SAR ADCs is utilized to reduce the switching energy, area, and number of the required switches in DAC capacitor arrays.

Two issues are considered in the selection of the regions to shift the sampled input signal into these regions. First, these regions should need less capacitors in their capacitive array. To do this, the negative differential input signals are shifted to the positive regions. Second, the targeted regions should have less switching energy than the rest of regions. As an example, Figure 2 shows the utilization of the proposed shifting technique in the switching scheme presented in Yuan and Lam.[10] In this example, $k = 2$ and after three MSBs decision, the sampled input signals in the ranges of $V_{in+} - V_{in-} < 0$ and $0 < V_{in+} - V_{in-} < (1-1/2^k)V_{Ref}$ are shifted into $0 < V_{in+} - V_{in-} < V_{Ref}/\ /2^k$ and $(1-1/2^k)V_{Ref} < V_{in+} - V_{in-} < V_{Ref}$ regions, respectively, where the required DAC switching energy is less than the other regions. The sampled input signals in the region of $(1-1/2^k)V_{Ref} < V_{in+} - V_{in-} < V_{Ref}$ are not shifted.

2.2 | Structure of the proposed SAR ADC

Figure 3 illustrates the overall structure of the conventional[27] and proposed 10-bit SAR ADCs where $k = 2$ has been considered in the proposed ADC. As it is seen, the lower capacitor array connected to the V_{DAC-} is exactly the same as the capacitor array of the conventional structure for a 10-bit ADC. The upper capacitor array connected to the V_{DAC+} is similar to the capacitor array of the conventional structure, but for $(k + 1)$ bit. This is because they are used to extract the first $(k + 1)$ MSBs. In the proposed structure, a dual input differential comparator is employed to resolve the bits across the large range of input signals.[26] In the proposed ADC, two different capacitive DAC arrays are utilized. The resolution of the upper capacitive DAC array is $(k + 1)$ bit, and it is used first to resolve $(k + 1)$ MSBs and then shift the sampled input signal to two special regions. The resolution of the lower capacitive DAC is N-bit and different DAC switching schemes can be utilized here. In Figure 3(b), the conventional DAC switching method has been utilized in the lower capacitive DAC, whereas we can use most of the recent energy efficient DAC switching schemes as well.

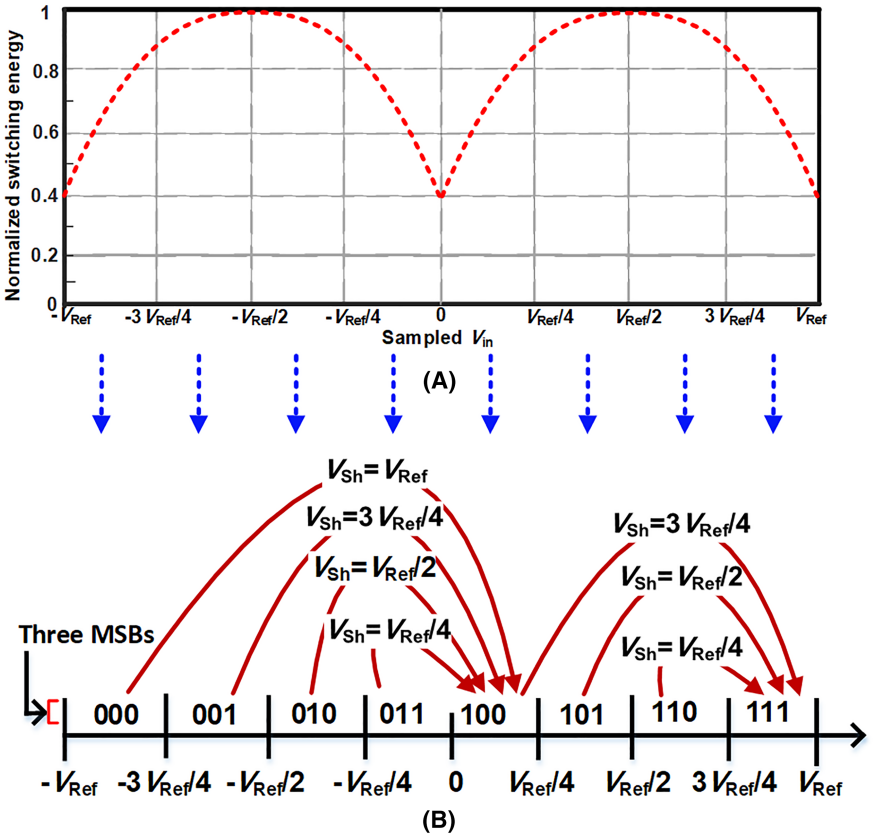

FIGURE 2 (A) Normalized DAC switching energy versus output digital codes in Yuan and Lam[10] and (B) using the proposed input signal shifting method with $k = 2$ [Colour figure can be viewed at wileyonlinelibrary.com]

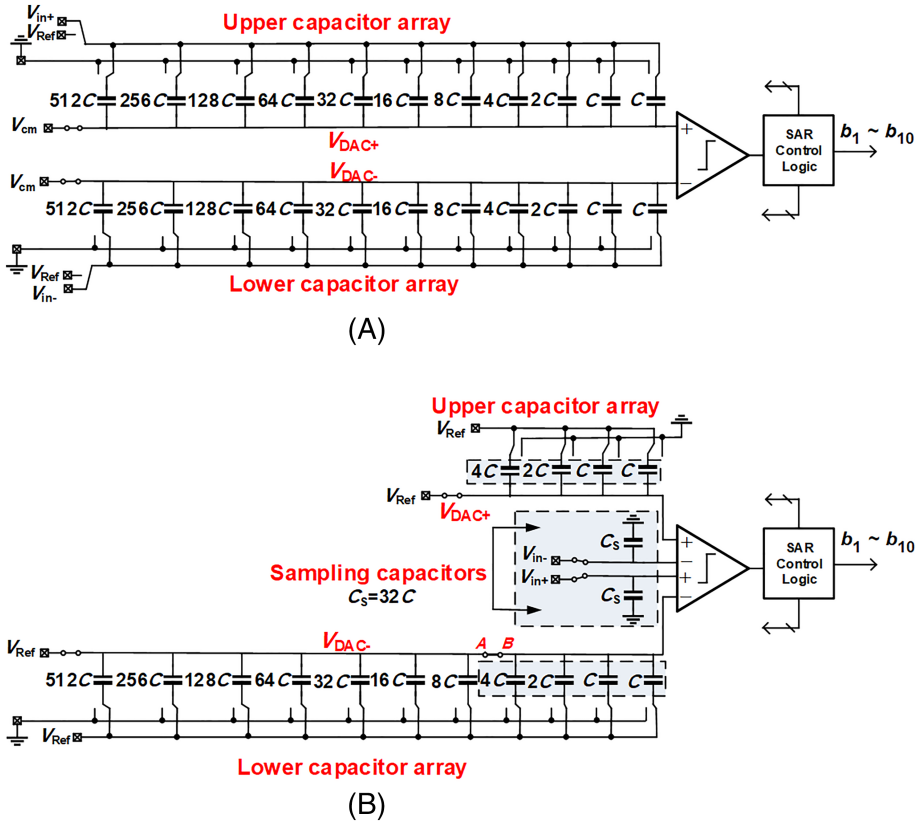

FIGURE 3 Structures of 10-bit SAR ADCs, (A) conventional and (B) proposed ($k = 2$) [Colour figure can be viewed at wileyonlinelibrary.com]

In overall, the upper DAC is used to resolve $(k + 1)$ MSBs, and these MSBs are used to properly shift the sampled input signal to the regions with less switching energy. The lower DAC is used to resolve all N bits corresponding to the sampled input signal.

2.3 | Proposed SAR ADC with conventional DAC switching

For a more detailed analysis of the proposed SAR ADC, the conventional DAC switching scheme[27] is utilized in the lower DAC array. Figure 3 shows the structures of the 10-bit conventional and proposed SAR ADCs with $k = 2$. The proposed DAC switching method for an N-bit SAR ADC is realized in two steps. Initially, $(k + 1)$ MSBs are obtained based on the differential input signal, $V_{in+} - V_{in-}$. In this case, the sampled input signal belongs to one of 2^{k+1} regions between $-V_{Ref}$ to V_{Ref}. In the second step, according to the $(k + 1)$ MSBs, V_{DAC+} (positive input voltage of the comparator) is increased to some extent according to the differential input value to be in one of the regions $0 < V_{in+} - V_{in-} < V_{Ref}/2_k$ or $(1–1/2^k)V_{Ref} < V_{in+} - V_{in-} < V_{Ref}$ for $V_{in} - V_{in-} < 0$ and $0 < V_{in+} - V_{in-} < (1–1/2^k)V_{Ref}$, respectively. When $(1–1/2^k)V_{Ref} < V_{in+} - V_{in-} < V_{Ref}$, we have $V_{DAC+} = 0$, and shifting is not performed. Indeed, in the proposed DAC switching method, after $(k + 1)$ MSBs decision, the sampled differential input signal is shifted into two special regions where the required DAC switching energy, and area is less than the other regions. Shifting of the sampled input signal is performed according to the MSBs, which are first extracted. This operation needs a relatively simple digital circuit.

In the conventional SAR ADC, the following comparison is used to resolve the bits:

$$V_{in+} - V_{in-} > V_{DAC-} - V_{DAC+}. \tag{1}$$

In the proposed ADC, after $(k + 1)$ MSBs decision, V_{DAC+} is constant, and the decision of the remaining bits is performed according to the following comparisons:

$$V_{in+} - V_{in-} > V_{DAC-} - \overbrace{(V_{DAC+})}^{\text{Fixed}} = > V_{in+} - V_{in-} + \overbrace{V_{DAC+}}^{V_{sh}} > \overbrace{V_{DAC-}}^{V_j}, \tag{2}$$

where V_{sh} is the level shifting voltage (for $k = 2$, its value is given in Figure 2B) and V_j is as follows:

$$V_j = V_{DAC-} = V_{j-1} \pm 2^{-(j-1)} V_{Ref}, \quad k+1 < j < N-1. \tag{3}$$

The relation 3 illustrates the conventional DAC switching scheme in the lower capacitive DAC in the proposed SAR ADC. According to relation 2, the shifted input signal is used to resolve the remaining LSBs, and this is performed with the lower capacitive DAC array. The output of the upper DAC is constant during these comparisons, and depending on the MSBs, its output value specifies the shifted value of the input signal.

In the proposed ADC, the bits extraction process is performed in four steps. The first step is sampling the input signal. The second step is to extract $(k + 1)$ MSBs. In the third step, according to the $(k + 1)$ MSBs, the sampled input signal is shifted to one of two special regions. In the fourth step, the remaining N-$(k + 1)$ bits are decided.

Figure 4 shows the proposed DAC switching structure for a differential 4-bit SAR ADC when $k = 1$. As shown in Figure 4A, first, the bottom and top plates of all DAC capacitors are connected to V_{Ref}, and the input signal is sampled into the C_S sampling capacitors. To resolve the two MSBs, the same capacitors in the lower DAC array as with the upper DAC are considered, and the remaining capacitors in the lower DAC are isolated from its array, and they are floating. Hence, the conventional DAC switching scheme is utilized to resolve the two MSBs. As shown in Figure 4B, a simple switch is utilized between Nodes A and B to isolate the capacitors in the lower DAC in order to reduce the charge sharing among the capacitors when some of the capacitors are floating. It is worth mentioning that the floating capacitor technique has also been used in other studies.[15,16,22] The parasitic of this switch can potentially affect the accuracy of the ADC. With this switch, there is a trade-off between the leakage reduction and parasitic effects. So, it should be used with care, and the related parasitics should be considered in the circuit design phase. Besides, like other methods,[15,16,22] this switch can be deleted without affecting the operation of the proposed ADC. Moreover, it is worth mentioning that in the proposed ADC, unlike previous circuits, the floating capacitors are different from the sampling capacitors of the input signal. Therefore, by using a simple and appropriate switch, for example a CMOS switch, we can greatly reduce the leakage while minimizing nonideal effects such as the charge injection.

After resolving the two MSBs, the bottom plates of all capacitors in the upper DAC array are remained constant during the rest of the $(N - 2)$ bits conversion. The bottom plates of the capacitors in lower DAC array are determined according to the sign of the differential input signal. If $V_{in+} - V_{in-} > 0$ (or $b_1 = 1$), the bottom plates of two largest capacitors $2^{N-3}C$ and $2^{N-4}C$ (for 4 bit: $8C$ and $4C$) are connected to V_{Ref} and otherwise (or $b_1 = 0$) they are connected to the ground and V_{Ref}, respectively. Bottom plates of the other capacitors in the lower DAC are connected to the ground. In Figure 4C, the initial states of the bottom plates of capacitors in the upper and lower DAC arrays after two MSBs decision are illustrated. To specify the residual bits, the method shown in Figure 4D is utilized (fourth step) like the conventional ADC.

2.4 | Proposed SAR ADC with two recent DAC switching schemes

It is worth mentioning that the most of the recent DAC switching schemes can be utilized in the proposed SAR ADC. Here, the DAC switching methods presented in Yuan and Lam and Hu et al.[10,15] are utilized in the proposed ADC to further reduce the DAC switching energy, area, and number of the required switches.

In Hu et al.,[15] the closed-loop charge recycling is utilized in the DAC switching of the SAR ADC, and it results in zero switching energy. In this technique, only one reference voltage is utilized, and hence, it has high precision. Figure 5 depicts the structure of the proposed 10-bit SAR ADC using the DAC switching scheme presented in Hu et al.[15] with $k = 2$. The bits extraction is performed as described in the previous subsection and in Hu et al.[15] As shown in Figure 5, the lower and upper DAC arrays are similar to the structure of Hu et al.[15] In this way, the lower DAC array is 10 bit and the upper DAC array is implemented as 3 bit due to $k = 2$. According to Figure 5, in the proposed 10-bit SAR ADC using the DAC switching scheme presented in Hu et al.,[15] the number of the required unit capacitors and switches are 1100 and 90, respectively. However, in Hu et al.,[15] 2044 unit capacitors and 152 switches are needed to realize a 10-bit SAR ADC. Therefore, the proposed SAR ADC results in more switching energy and area savings compared to the presented ADC in.[15]

The DAC switching scheme presented in Yuan and Lam[10] is also utilized in the proposed SAR ADC. Figure 6 illustrates the structure of the proposed 10-bit SAR ADC using the DAC switching method presented in Yuan and Lam[10]

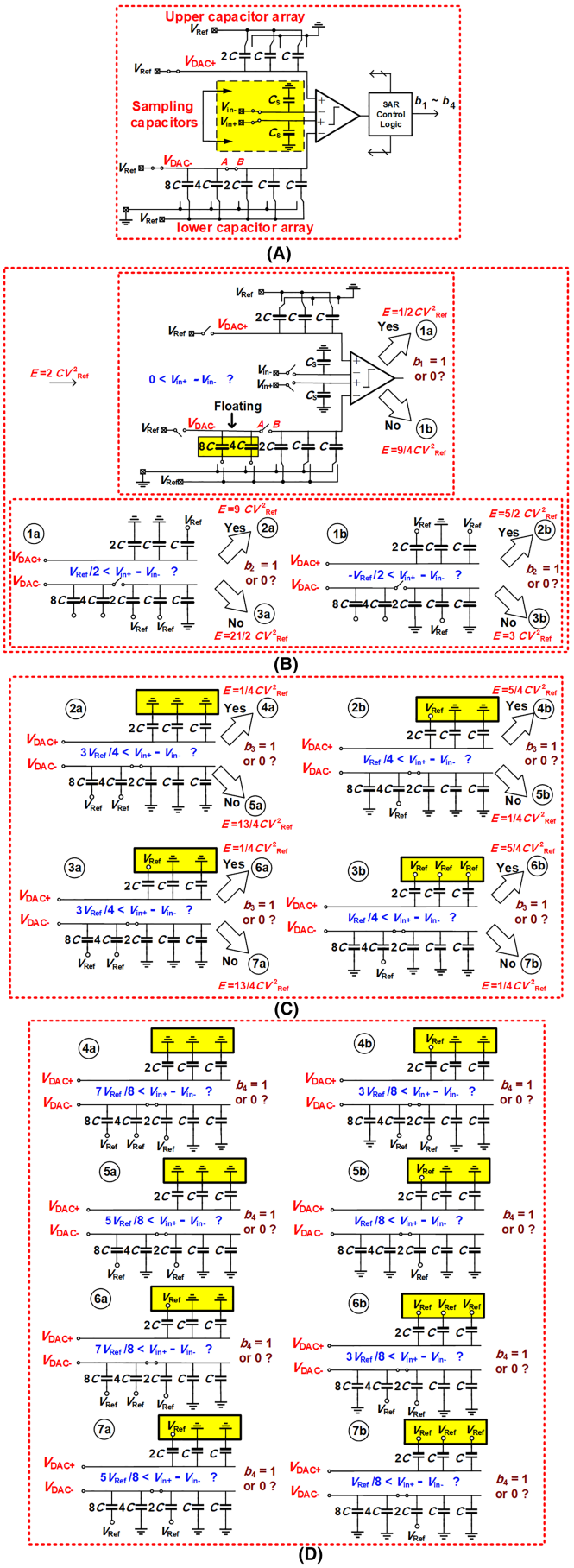

FIGURE 4 Switching steps of the proposed 4-bit ADC with the conventional DAC switching ($k = 1$). (A) Sampling, (B) two MSBs (first and second bits) decision, (C) third-bit decision, and (d) fourth-bit decision [Colour figure can be viewed at wileyonlinelibrary.com]

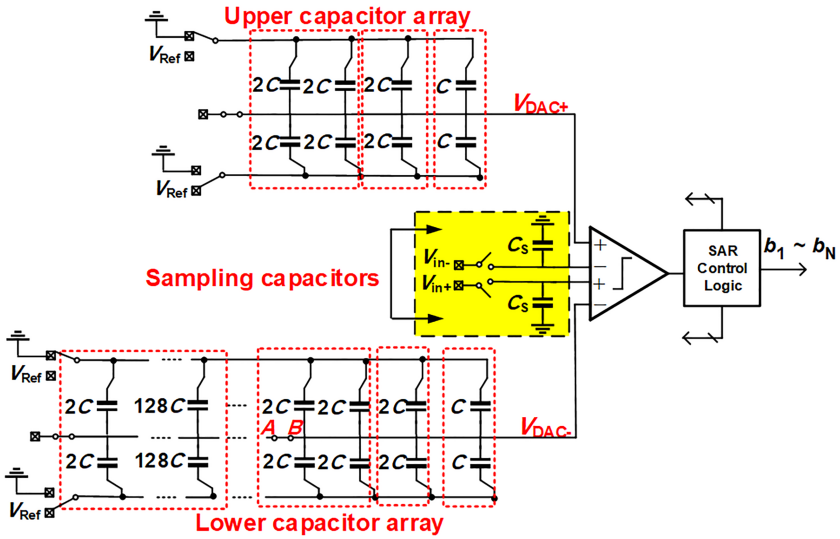

FIGURE 5 The proposed 10-bit SAR ADC with the DAC switching scheme presented in Hu et al.[15] and $k = 2$ [Colour figure can be viewed at wileyonlinelibrary.com]

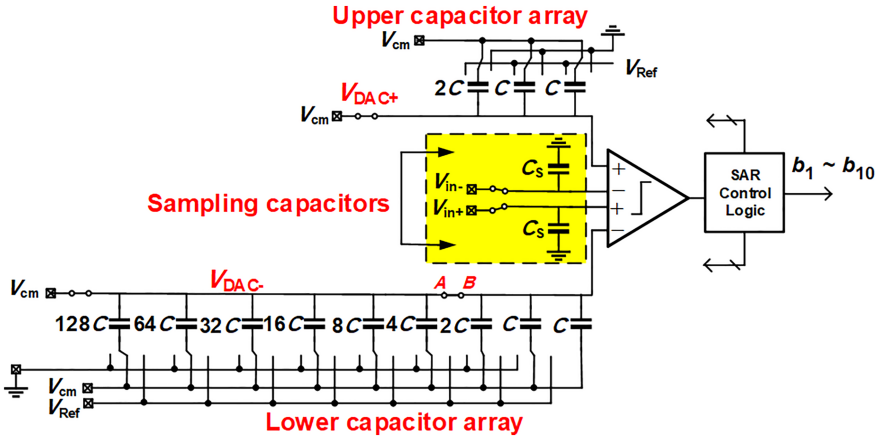

FIGURE 6 The proposed 10-bit SAR ADC with the DAC switching scheme presented in Yuan and Lam[10] and $k = 2$ [Colour figure can be viewed at wileyonlinelibrary.com]

with $k = 2$. As shown in Figure 6, the lower and upper DAC arrays are similar to the structure of.[10] In this ADC, the lower DAC array is 10 bit, and the upper DAC array is 4 bit instead of 3 bit ($k = 2$). According to Zhu et al.,[8] one extra bit in the upper DAC array is used to extract the first three MSBs without any sensitivity to the variations of V_{cm}. Table 1 summarizes the bottom plate voltage of the capacitors in the upper DAC array after extracting the first three MSBs. According to Figure 6, in the proposed 10-bit SAR ADC using the DAC switching scheme presented in Yuan and Lam,[10] the number of the required unit capacitors and switches are 324 and 35, respectively. But, in Yuan and Lam,[10] 512 unit capacitors and 52 switches are used to realize a 10-bit SAR ADC.

TABLE 1 Initial state of the capacitors after three MSBs decision in the proposed N-bit SAR ADC using the DAC switching scheme in Yuan and Lam[10] with $k = 2$

		Initial state after three MSBs decision							
Capacitors	**MSBs decision**	**000**	**001**	**010**	**011**	**100**	**101**	**110**	**111**
Upper DAC array	$2C$	V_{Ref}	V_{Ref}	V_{Ref}	gnd	V_{Ref}	V_{Ref}	gnd	gnd
	C		V_{cm}	gnd		V_{cm}	gnd		
	C				V_{Ref}			V_{Ref}	
Lower DAC array	$2^{N-3}C$ and $2^{N-4}C$	gnd				V_{Ref}			
	Other	V_{cm}							

3 | ANALYSIS OF THE PROPOSED SAR ADC

3.1 | Accuracy

The accuracy of the proposed SAR ADC depends on the utilized DAC switching scheme. So, when only one reference voltage is utilized in the DAC switching, the extraction of bits is performed with high precision. The midlevel reference voltage (V_{cm}) is employed in several recent DAC switching techniques. Some of these methods are sensitive to the variations on the V_{cm}, and some are not. In the case of using a V_{cm}-sensitive DAC switching scheme in the proposed ADC, the extraction of all bits are affected by the variations in V_{cm}. In this case, we can use the technique presented in Zhu et al.[8] to resolve the $(k + 1)$ MSBs without any sensitivity to the variations in V_{cm}. In Zhu et al.,[8] in all bits cycling, the bottom plate of equal number of capacitors in both upper and lower DAC arrays are connected to V_{cm}. Nonetheless, the extraction of the remaining bits will be affected by the V_{cm} variations in the proposed ADC.

3.2 | Switching energy

The total switching energy of the proposed SAR ADC is given by

$$E = E_{res} + E_{ins1} + E_d + E_{sh} + E_{ins2} + E_{oth}, \tag{4}$$

where E_{res}, E_{ins1}, E_d, E_{sh}, E_{ins2}, and E_{oth} are the reset energy, switching energies of the initial state of $(k + 1)$ MSB, $(k + 1)$ MSBs decision, shifting the sampled input signal (V_{sh}), initial state of the lower capacitive DAC array, and other $N - (k + 1)$ bit decision, respectively. E_{res} depends on the amount of residual energy in the utilized DAC switching method. Therefore, the proposed ADC does not have any reset energy when a DAC switching scheme without any reset energy such the conventional one is utilized. For example, for $b_1b_2b_3b_4 = 1111$, as shown in Figure 4, by using the conventional DAC switching scheme in the proposed ADC, we have the following switching energies: $E_{res} = 0$, $E_{ins1} = 2\ CV^2_{Ref}$, $E_d = 1/2\ CV^2_{Ref}$, $E_{sh} + E_{ins2} = 9\ CV^2_{Ref}$, $E_{oth} = 1/4\ CV^2_{Ref}$. The average total switching energy of the proposed 4-bit SAR ADC with the conventional DAC technique, which is shown in Figure 4, is 10.875 CV^2_{Ref}, whereas it is 19.375 CV^2_{Ref} for the conventional 4-bit SAR ADC. So, the proposed ADC reduces the average switching energy about 43.8% in comparison with the conventional ADC.

The average switching energy of the proposed ADC shown in Figure 6 is calculated here for an N-bit resolution with $k = 2$. According to the proofs given in Gao et al.,[13] when the bottom plate voltage of all capacitors is equal such as the proposed ADC, the reset energy is zero. Therefore, the reset energy is zero in the proposed ADC ($E_{res} = 0$) and also for the same reason $E_{ins1} = 0$. Using the tracking energy calculation process, the average switching energy in the decision of the $(N - 3)$ LSBs (E_{oth}) is obtained as

$$\begin{aligned} E_{oth} &= \left(\frac{2^{N-5}}{N-4}\right)\left(0.5\,(N-4) - \sum_{i=4}^{N-1}\frac{1}{2^i}\right)\left(CV^2_{Ref}\right), \quad N > 4 \\ E_{oth} &= 0, \qquad\qquad\qquad\qquad\qquad N \le 4. \end{aligned} \tag{5}$$

The average switching energy consumed during the three MSBs decision (E_d), shifting the sampled input signal (E_{sh}) and the initial state of lower capacitive DAC array after three MSBs decision (E_{ins2}) for the proposed N-bit SAR ADC are given in Table 2. Thus, according to the relations 4 and 5 and Table 2, the total average switching energy for the proposed ADC shown in Figure 7 is obtained as

$$E_{total,av} = \left[\left(\frac{2^{N-5}}{N-4}\right)\left(0.5\,(N-4)\ - \sum_{i=4}^{N-1}\frac{1}{2^i}\right) + 3\times 2^{N-8} + 1.329\right]\left(CV^2_{Ref}\right), \quad (N > 4). \tag{6}$$

Therefore, the total average switching energy of the proposed 10-bit SAR ADC using the DAC switching scheme of Yuan and Lam[10] is 28.695 CV^2_{Ref} when $k = 2$. On the other hand, it is 42.4 CV^2_{Ref} for 10-bit ADC presented in Yuan and Lam.[10] So, 32.3% switching energy reduction is achieved here.

TABLE 2 Different switching energy terms in the proposed N-bit SAR ADC using the DAC switching scheme in Yuan and Lam[10] with $k = 2$

MSBs decision switching energy	000	001	010	011	100	101	110	111
$E_d/(CV^2_{Ref})$	5/8	5/8	9/8	9/8	9/8	9/8	5/8	5/8
$E_{sh}/(CV^2_{Ref})$	0	3/8	1/4	7/8	7/8	7/8	3/8	0
$E_{ins2}/(CV^2_{Ref})$	$3 \times 2^{N-8}$							

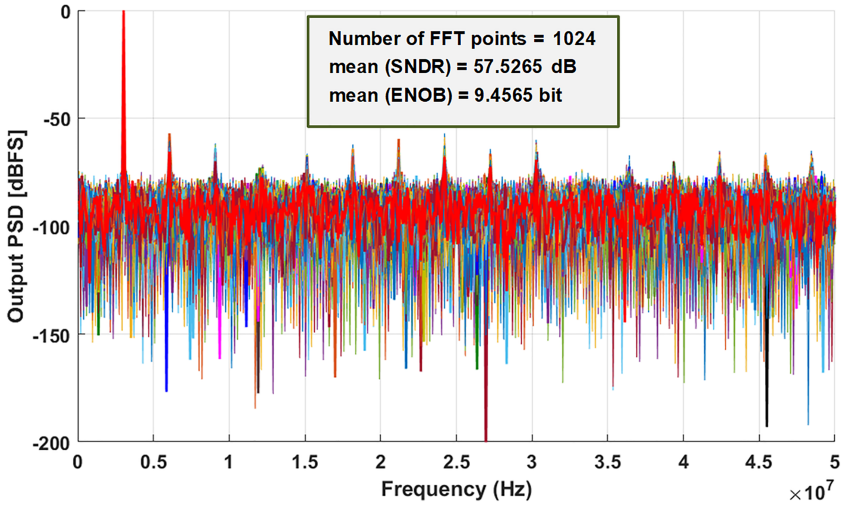

FIGURE 7 The simulated output PSD of the proposed 10-bit SAR ADC (500 runs) [Colour figure can be viewed at wileyonlinelibrary.com]

3.3 | DAC area

As discussed before, the sampled negative input signals are shifted to the positive regions in the proposed SAR ADC. This technique reduces the size of the required capacitors and results in DAC area saving. The number of the required unit capacitors in the conventional,[27] closed-loop charge recycling,[15] and tri-level[10] 10-bit SAR ADCs are 2048, 2044, and 512, respectively. The proposed 10-bit SAR ADC with $k = 2$, and using the conventional, closed-loop charge recycling, and tri-level DACs needs 1032, 1100, and 324 unit capacitors, respectively, without considering the sampling capacitors. Therefore, the proposed ADC reduces the DAC area as well in comparison with the original ADCs using the same DAC switching schemes.

3.4 | Number of switches and logic circuit complexity

The large number of required switches in DAC array needs more area, and in some cases, a complicated control logic is needed. Also, due to the large number of switches, the power consumption of the digital control circuit is significant in some designs like Lui et al.[11] In the proposed ADC, this issue has been considerably addressed. In fact, since most of the capacitors are eliminated in the proposed ADC, most of the switches are also eliminated. The number of required DAC switches in 10-bit conventional,[27] closed-loop charge recycling,[15] and tri-level[10] ADCs are 48, 152, and 52, respectively. The proposed ADC with 10-bit resolution and $k = 2$ needs 31, 88, and 35 switches when using the conventional, closed-loop charge recycling, and tri-level switching DACs, respectively. It is worth mentioning that the logic complexity is increased with k since the number of regions that the input signal to be shifted is also increased.

In the proposed SAR ADC, four steps should be performed by the logic circuit including (1) sampling, (2) extraction of $(k + 1)$ MSBs, (3) signal shift, which is done by changing the bottom plate voltages of the capacitors in the upper DAC array, and (4) extraction of the remained $(N - k - 1)$ bits. The logic circuit in the proposed N-bit SAR ADC in Steps 1 and 2 is exactly the same as the logic circuit of the conventional $(k + 1)$ bit SAR ADC. In Step 3, we need a relatively simple logic circuit that connects the bottom plates of the capacitors in the upper DAC array to the appropriate voltages (V_{Ref}, gnd, or other voltage references according to the original switching scheme). Also, the

voltage of some largest capacitors in the lower DAC array is determined according to k. The number of these capacitors, whose voltage should be determined and remained constant until the last stage of bit extraction, is equal to the number of upper DAC array capacitors of a $(k + 1)$ bit. So, with increasing k, the number of these capacitors is also increased, and obviously, we need a larger logic circuit here. In Step 4, the remaining bits are extracted in a similar way to the original switching scheme, but only in the lower DAC capacitive array.

3.5 | Dynamic performance of the proposed ADC

The linearity of the proposed ADC with the DAC switching scheme presented in Yuan and Lam[10] and $k = 2$ is examined here. A sinusoidal input signal with 3.02734375-MHz frequency is applied to the proposed ADC with 10-bit resolution and 100-MHz sampling rate. This behavioral simulation is performed in MATLAB by considering the mismatch in DAC unit capacitors with $3\,\sigma_u = 0.01\,C_u$.[16,22,26] According to Yousefi et al. and Chen et al.,[22,26] this amount of capacitor mismatch is considered to achieve 10-bit accuracy. Other circuit nonidealities such as the comparator offset and DAC settling error should be considered in the circuit design and the related circuits should be designed based on the required accuracy. The simulated output power spectral density (PSD) of the ADC is shown in Figure 7 where 500 Monte Carlo runs have been performed. The achieved mean signal-to-noise and distortion ratio (SNDR) and effective number of bits (ENOBs) are 57.53 dB and 9.46, respectively.

3.6 | Effects of k on ADC performance

In this section, the effects of different values of k on the proposed ADC performance are evaluated. The switching energy of the proposed 10-bit SAR ADC using the DAC switching scheme presented in Yuan and Lam[10] is calculated for different values of k in MATLAB, and the results are shown in Figure 8. As shown in Figure 8, when k is large, all regions have approximately the same switching energy, and hence, shifting the sampled input signal will be less efficient to reduce the switching energy. On the other hand, due to large number of the regions, the power consumption of the shifting process will be increased. Therefore, the switching energy will not be reduced by increasing k when it is large ($k > 5$).

Figure 9 shows the simulated average switching energy and the number of unit capacitors in the proposed 10-bit SAR ADC with the DAC switching scheme presented in Yuan and Lam.[10] As it is seen, the switching energy does not decrease uniformly with increasing k, and it has an ascending trend for $k > 4$. This is owing to the added power consumption of the shifting process and also less efficiency of the shifting of the input signal when k is large. For example, 32 regions should be considered for $k = 4$. On the other hand, the number of the unit capacitors is increased with k. Thus, large values of k increase the area and complexity of the logic circuit. Furthermore, the number of the required switches for an N-bit proposed SAR ADC is $3(N + k) - 1$. Therefore, $1 \leq k \leq 3$ is recommended.

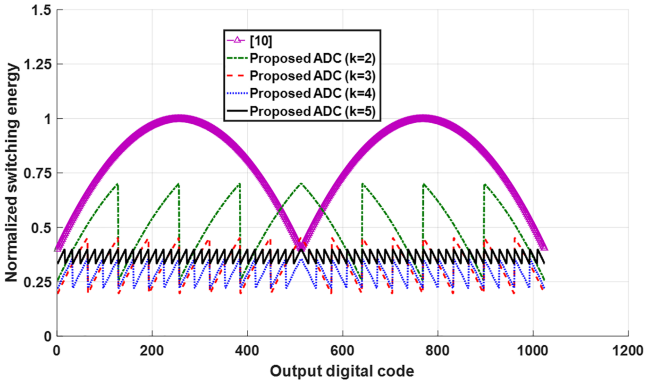

FIGURE 8 Normalized switching energy of 10-bit SAR ADCs versus the digital output codes with different values of k [Colour figure can be viewed at wileyonlinelibrary.com]

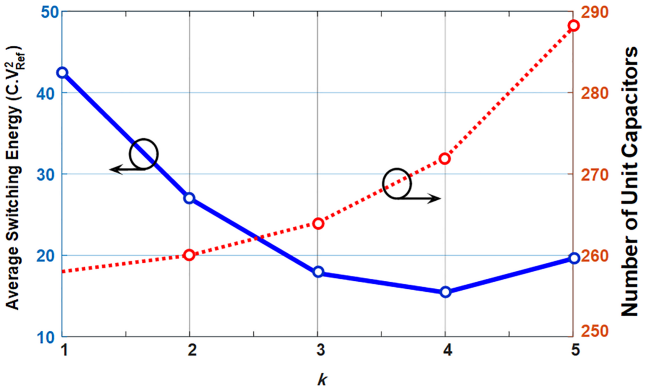

FIGURE 9 Simulated switching energy and the number of unit capacitors in the proposed 10-bit ADC versus k [Colour figure can be viewed at wileyonlinelibrary.com]

3.7 | Comparisons and discussions

The behavioral simulations of the proposed 10-bit fully differential SAR ADC using two previously reported DAC switching techniques were performed in MATLAB, and the results are summarized in Table 3 where the behavioral simulation results of several other ADCs are reported for the comparison purposes. The number of the required switches in DAC array is considered as a metric for logic complexity. The number of required DAC switches of some methods is given in Lui et al.[11] As it is seen, the proposed SAR ADC with DAC switching technique presented in Yuan and Lam[10] needs less DAC switching energy, area, and number of switches in comparison with high accuracy,[9] tri-level,[10] set and down,[11] capacitor splitting DAC,[12] and modified split-capacitor[21] schemes. Although the DAC switching energy in the common-mode voltage switching[13] and closed-loop charge recycling[15] is less than the proposed ADC, the number of switches and capacitor size is highly reduced in the proposed ADC. The DAC switching energy

TABLE 3 Comparison of several 10-bit SAR ADCs

Switching scheme	Average switching energy (CV^2_{Ref})	Energy saving (%)	Area reduction (%)	Number of switches (N-bit)[b]	Number of unit capacitors
Conventional[25]	1363.3	Reference	Reference	$4N + 8$	2048
Set and down[11]	255.5	81.26	50	$4(N - 1)$	1024
High accuracy[9]	85.08	93.759	75	$6N - 8$	512
Modified split-capacitor[18]	69.58	94.9	75	88[a]	512
Tri-level[10]	42.4	96.89	75	$6N - 8$	512
Capacitor splitting DAC scheme[12]	42.17	96.91	75	$8N$ -12	512
Common-mode voltage switching[13]	8.8	99.35	73.4	86[a]	544
Reference-insensitive[18]	7.8	99.43	50	60[a]	1024
Charge-sharing[16]	7.30	99.51	93.55	114[a]	132
Closed-loop charge recycling[15]	0	100	0.2	$2(N^2 - 3N + 6)$	2044
Energy-efficient[22]	0	100	87.9	744[a]	248
This work ($k = 2$) (applied in[10])	28.695	97.89	84.17	$3N + 5$	324[c]
This work ($k = 2$) (applied in[15])	0	100	46.28	$N^2 - 3N + 18$	1100[c]

[a]For 10-bit ADC.
[b]Without sampling switches.
[c]Without sampling capacitors.

and area reduction in Zhang et al. and Yousefi et al.[16,22] is more than that of the proposed ADC, but the number of required switches is highly reduced in the proposed ADC.

To realize high-resolution SAR ADCs such as 12 bit, k can be selected greater than 2 to reduce the DAC switching energy. However, the logic complexity is increased with k, and hence, there is a trade-off between the DAC switching energy, logic complexity, and power consumption with increasing k. It should be noted that most of the current DAC switching schemes can be utilized in the proposed SAR ADC. So, high accuracy and energy efficient DAC switching techniques and larger values of k can be utilized in the proposed SAR ADC to realize high-resolution ADCs as well. The proposed SAR ADC can also be used in SAR-assisted two-stage or multistage pipeline ADCs where 4- to 7-bits SAR ADCs are employed in the pipeline stages. In this case, $k = 2$ can be considered to realize low- to medium-resolution SAR sub-ADCs.

To alleviate the effect of DAC settling error in SAR ADCs, redundant decisions are utilized.[28] The proposed DAC switching technique can be utilized in SAR ADCs with redundant decisions as well. Figure 10A shows the structure of a 5-bit SAR with 1-bit redundancy, which has been presented in Wu et al.[28] In this ADC, the bit extraction is performed without the need for a third reference voltage. The redundancy performance is divided into first (1 bit), coarse (2 bit), and fine (3 bit) conversions. The scheme uses a single-ended procedure, which just switches one capacitor on one side of the DAC array after the first decision, and the capacitors on the other side remain unchanged until the last bit extraction.[28] Due to the use of two different procedures for extracting bits depending on the input range ($V_{in} > 0$ or $V_{in} < 0$), the logic circuit of this scheme is relatively complex.

As illustrated in Figure 10B, the proposed technique is employed in redundant scheme in Wu et al.[28] with $k = 0$. With the aims of (a) simplifying the logic circuit and thus reducing the power consumption and wiring of this part and (b) reducing the number of capacitors and as a result, reducing the number of switches, we chose $k = 0$. Therefore, by extracting the first MSB, no shift will be performed if $b_1 = 1$ or $V_{in} > 0$, but for $b_1 = 0$ or $V_{in} < 0$, the signal shift value is V_{Ref}. To do this, the bottom plate of the unit capacitor of the upper DAC is connected to gnd and V_{Ref} for $V_{in} > 0$ and

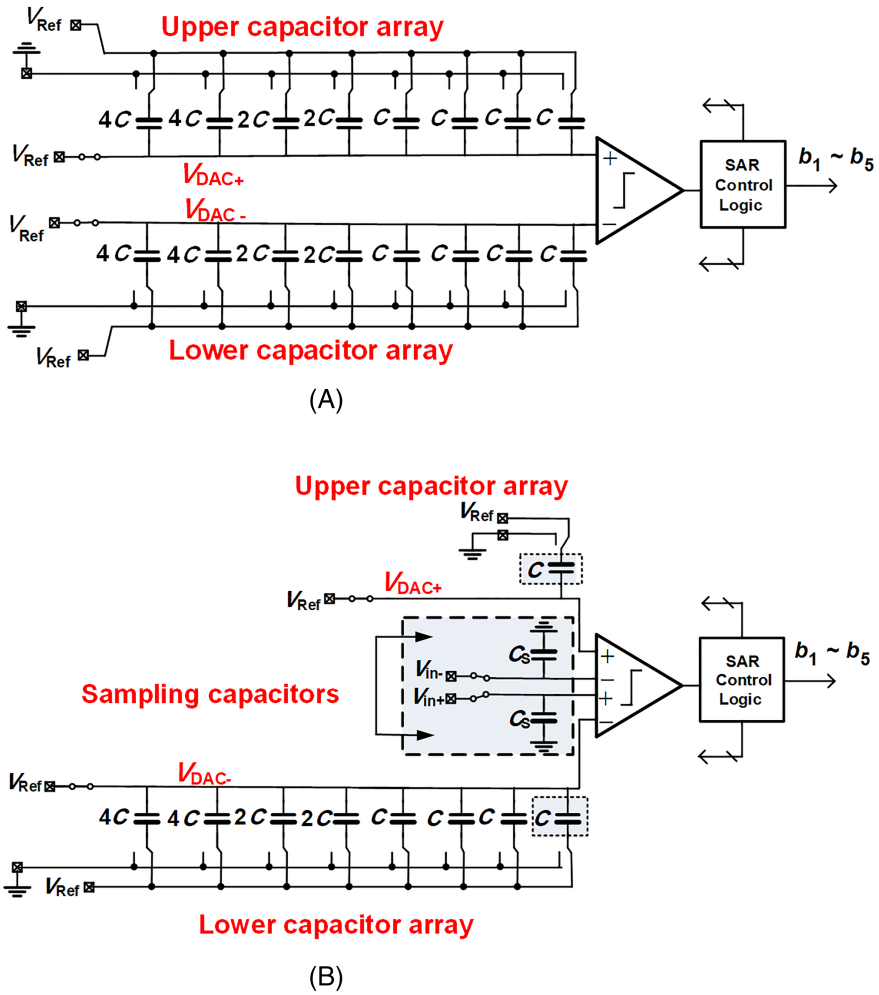

FIGURE 10 (A) Structure of a 5-bit SAR ADC with 1-bit redundancy in Wu et al.[28] and (B) the proposed ADC with $k = 0$ [Colour figure can be viewed at wileyonlinelibrary.com]

$V_{in} < 0$, respectively. After extracting the first MSB and the appropriate signal shift, the bit extraction process is exactly the same as the redundant scheme in Wu et al.[28]

4 | CONCLUSIONS

In this paper, a new structure for SAR ADCs has been presented to reduce the DAC switching energy, area, and number of the required switches. In this ADC, after a few most significant bits decision, the sampled differential input signal is shifted into two special regions according to the value of MSBs. Most of the previously reported energy efficient DAC switching schemes can be utilized in the proposed ADC to further reduce the DAC switching energy and area. The proposed technique has been applied to the conventional and two recent DAC switching techniques, and according to the analysis and simulation results, it results in significantly switching energy and area savings. In addition, the proposed ADC reduces the required number of DAC switches greater than the other methods. So, the proposed SAR ADC is proper for low power and low area applications.

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