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# A low-power four-stage amplifier for driving large capacitive loads

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## ABSTRACT

A four-stage amplifier with a new and efficient frequency compensation topology is presented in this paper. The new compensation scheme applies a Miller capacitor as the main negative feedback, a resistor and a capacitor in series as a load for one of the intermediate stages, and two feedforward paths. In order to design the amplifier and acquire circuit parameters, small signal analyses have been carried out to derive the signal transfer function and the pole-zero locations. The proposed amplifier was designed and implemented in a standard 90 nm CMOS process with two heavy capacitive loads of 500 pF and 1 nF. The simulation results show that when driving a 500 pF load, the amplifier has a gain-bandwidth product of 18 MHz consuming only 40.9 μW. With a 1 nF capacitive load, the proposed amplifier achieves 15.1 MHz gain-bandwidth product and dissipates 55.2 μW from a single 0.9 V power supply. Copyright © 2013 John Wiley & Sons, Ltd.

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KEY WORDS: multistage amplifiers; four-stage amplifier; frequency compensation; nested Miller compensation

## 1. INTRODUCTION

The operational amplifier is the core building block for analog and mixed-mode signal processing systems. As the channel length and the supply voltage for integrated circuits continue to scale down, multistage amplifiers are becoming more essential, especially for high precision purposes as they can provide high gain and large output swing with low supply voltages [1–4]. However, each stage adds at least a low-frequency pole resulting in the degraded stability which is an important amplifier design constraint. Recently, several frequency compensation topologies, most of which are based on nested Miller compensation (NMC) technique have been proposed [5–8].

For large capacitive loads, the NMC amplifier needs large compensation capacitors. These capacitors create a positive feedback loop which might lead to instability. To ensure stability, the transconductance of the last stage has to be large [9, 10]. Therefore, the NMC topology is not suitable for low-power large capacitive load amplifiers. To alleviate the drawbacks of the NMC technique, other compensation schemes such as multipath NMC (MNMC) [11] and NMC with feedforward and nulling resistor (NMCFNR) [12] were reported. In MNMC amplifier, a feedforward path is used to perform a pole-zero cancellation within the pass-band to improve the bandwidth. In NMCFNR topology, in addition to a feedforward path, a nulling resistor is added to ease the negative effect of the positive feedback loop on the stability of the amplifier.

For three-stage amplifiers with inverting intermediate stages, the reversed NMC (RNMC) frequency compensation scheme is an alternative option [13–16]. The operating principle of NMC

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and RNMC techniques are almost identical, but, in the latter, the inner Miller capacitor is not connected to the output node, and hence, it achieves an inherently larger bandwidth than the NMC one under equal conditions [14–16]. For this reason, several RNMC-based compensation topologies have been recently proposed such as RNMCFNR and reversed active feedback frequency compensation.

For recent low-voltage nanometer CMOS technologies, in order to achieve high dc gain and large output swing simultaneously, four-stage amplifiers are going to be popular. However, most of the frequency compensation schemes have been designed to ensure the stability in three-stage amplifiers. Obviously, the frequency compensation task for four-stage amplifiers is more complicated, due to the presence of additional low-frequency poles. Therefore, for nanometer CMOS four-stage amplifiers, novel and efficient compensation topologies have to be developed. In [7], a four-stage amplifier with nested $G_m$-C compensation topology (NGCC) has been reported which utilizes multi compensation capacitors with relatively large values to carry out the pole splitting task and compensate the frequency response. Large Miller capacitors, on the other hand, increase the silicon die area and introduce low-frequency right half plane zeros, and thus, degrade the amplifier phase response. In the four-stage amplifier reported in [17], the transconductances are large, and this moves the non-dominant poles to higher frequencies and improves the gain-bandwidth product. Clearly, this causes the amplifier to dissipate more power and makes it unsuitable for low-power applications such as battery-operated hand held devices.

From the above, it can be concluded that in the compensation techniques which are solely based on the pole splitting, the dominant pole is pushed to very low frequencies, and this results in a dramatically reduced bandwidth. In this paper, a new frequency compensation scheme for four-stage amplifiers is proposed. Since in the proposed amplifier, the Miller capacitors are small in value, the bandwidth is not much decreased, and the stability is guaranteed with two pole-zero cancellations. As a result, it achieves a higher gain-bandwidth product while ensuring the stability and preserving the low-power nature of the amplifier.

The paper is organized as follows. In Sect. 2, the structure of the proposed four-stage amplifier is presented. The small-signal analysis, the stability considerations, and a simple design procedure of the proposed amplifier are provided in Sect. 3. Section 4 presents the circuit level implementation of the amplifier. The simulation results are provided in Sect. 5, and finally, Sect. 6 concludes the paper.

## 2. STRUCTURE OF THE PROPOSED AMPLIFIER

The block diagram of the proposed four-stage amplifier is depicted in Figure 1. It employs four cascaded amplifying stages, where $g_{mi}$, $C_i$, and $R_i$ represent the transconductance, the lumped parasitic node capacitance, and output resistance of the $i^{th}$ stage, respectively. The main distinction of the presented topology from the ordinary NMC based multi capacitor amplifiers such as NGCC amplifier is that the inner Miller capacitors are eliminated. Alternatively, a capacitor is used in series with a resistor as the load in the third stage. This RC network generates a low-frequency left half

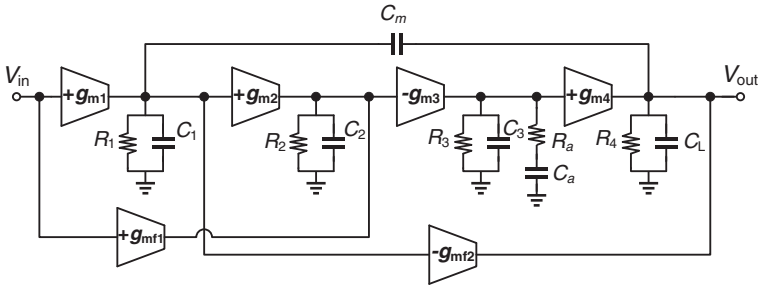


Figure 1. The block diagram of the proposed amplifier.



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plane (LHP) zero which contributes to an accurate low-frequency pole-zero cancellation. Also, a feedforward stage with a transconductance of $g_{mf1}$ is included from the input of the amplifier to the output node of the second stage to create another LHP zero and to perform the second pole-zero cancellation. In fact, there are different scenarios to place this feedforward stage between the nodes of the amplifier, but, the proposed path leads to a much less power dissipation. Another feedforward transconductance stage, $g_{mf2}$, is applied to improve the stability as well as the large signal performance. In the following sections, the above facts will be investigated by analysis of the proposed amplifier.

As mentioned, the idea of this topology is to compensate the negative phase shift of the poles with the positive phase shift due to LHP zeros. For low-power designs, since the transconductances are small, the non-dominant poles are not moved to very high frequencies and generating LHP zeros to cancel the non-dominant poles is inevitable. Recently, creating pole-zero pairs within the pass-band has been introduced as a reliable approach to design low-power high gain amplifiers with fast responses. This method, for instance, is demonstrated in the LDO regulator proposed in [18], in the two-stage no capacitor feedforward [19] amplifier as well as the three-stage MNMC and impedance adapting compensation [6] amplifiers.

## 3. THE AC RESPONSE AND STABILITY OF THE PROPOSED AMPLIFIER

Herein, the design methodology for the proposed amplifier is discussed. To investigate the ac response and stability, the open-loop signal transfer function of the proposed four-stage amplifier has been derived by considering the small signal model shown in Figure 2.

By neglecting the high frequency poles and zeros, the small-signal transfer function of the amplifier can be described by:

$$A_v(s) = A_{dc}\frac{1 + as + bs^2}{1 + cs + ds^2 + es^3 + fs^4} \tag{1}$$

where $A_{dc} = -g_{m1}g_{m2}g_{m3}g_{m4}R_1R_2R_3R_4$ is the dc gain of the amplifier.

In order to obtain simple and approximate expressions in the numerator and the denominator of the transfer function, the following assumptions are considered:

$$g_{mi}R_i >> 1, C_L >> C_m, C_a >> C_1, C_2, C_3 \tag{2}$$

Based on the assumptions described in (2), the coefficients in the signal transfer function are approximately given by:

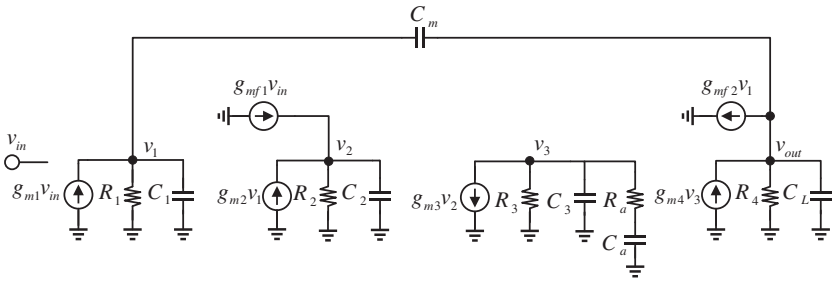


Figure 2. Small-signal model of the proposed amplifier.



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$$
\begin{aligned}
a &= \frac{g_{mf1}\, C_m}{g_{m2}\, g_{m1}} + R_a\, C_a \\
b &= \frac{g_{mf1}\, C_a\, R_a\, C_m}{g_{m2}\, g_{m1}} \\
c &= g_{m2}\, g_{m3}\, g_{m4}\, R_1\, R_2\, R_3\, R_4\, C_m \\
d &= g_{m2}\, g_{m3}\, g_{m4}\, R_1\, R_2\, R_3\, R_4\, C_m\, C_a\, R_a \\
e &= R_1\, R_4\, C_m\, C_a\, C_L(R_a + R_3) \\
f &= R_1\, R_4\, C_m\, C_a\, C_L(C_2\, R_2\, R_3 + C_3\, R_3\, R_a + C_2\, R_2\, R_a)
\end{aligned}
\tag{3}
$$

Using the expressions a, b, c, d, e, and f, the pole-zero locations can be obtained as follows:

$$\omega_{z1} = -\frac{1}{\frac{g_{mf1}\, C_m}{g_{m2}\, g_{m1}} + R_a\, C_a} \tag{4}$$

$$\omega_{z2} = -\frac{g_{mf1}\, C_m + g_{m2}\, g_{m1}\, R_a\, C_a}{g_{mf1}\, R_a\, C_a\, C_m} \tag{5}$$

$$\omega_{p1} = -\frac{1}{g_{m2}\, g_{m3}\, g_{m4}\, R_1\, R_2\, R_3\, R_4\, C_m} \tag{6}$$

$$\omega_{p2} = -\frac{1}{C_a\, R_a} \tag{7}$$

$$\omega_{p3} = -\frac{g_{m2}\, g_{m3}\, g_{m4}\, R_2\, R_3\, R_a}{C_L(R_a + R_3)} \tag{8}$$

$$\omega_{p4} = -\frac{(R_a + R_3)}{(C_2\, R_2\, R_3 + C_3\, R_3\, R_a + C_2\, R_2\, R_a)} \tag{9}$$

The strategy of the system design is to calculate the pole-zero locations of the open-loop signal transfer function, and to arrange them properly to optimize the performance of the amplifier such as the gain-bandwidth product and the phase margin. Since in an uncompensated four-stage amplifier, there are multiple poles located close to each other and below the unity gain frequency, the pole splitting task is needed to be applied [6]. As mentioned in Sect. 2, the main idea of the proposed frequency compensation scheme is two pole-zero cancellations in addition to a pole splitting performed by a small Miller capacitor. The multiplication of dc gain by dominant pole frequency, $\omega_{p1}$, yields the amplifier's gain-bandwidth product given by:

$$\omega_{GBW} \approx \omega_{p1} A_{dc} = \frac{g_{m1}}{C_m} \tag{10}$$

By comparing the zero frequency $\omega_{z1}$ with the pole frequency $\omega_{p2}$, it can be seen that for the condition described in (11), the first pole-zero cancellation is achieved.



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$$C_a R_a >> \frac{g_{mf1} C_m}{g_{m2} g_{m1}} \tag{11}$$

It is obvious that the larger values of the multiplication $C_aR_a$ results in a more accurate pole-zero cancellation. By choosing the proper value for $g_{mf1}$, the second zero $\omega_{z2}$ eliminates the third pole $\omega_{p3}$ in the small signal transfer function. By considering (5) and (8) and also the condition described in (11), the transconductance $g_{mf1}$ is obtained, as follows:

$$g_{mf1} = \frac{g_{m1} C_L (R_a + R_3)}{g_{m3} g_{m4} R_2 R_3 R_a C_m} \tag{12}$$

In order to make gmf1 insensitive to the variations of Ra, the value of resistor Ra has to be chosen much larger than R3. In this way, Ra can be cancelled out in (12) resulting in a more accurate pole-zero cancellation. Following the constraints described in (11) and (12) will result in two accurate pole-zero cancellations. It is worth mentioning that the imperfect pole-zero elimination affects the transient response of the amplifier and degrades the settling time [20]. However, by considering (4) and (7), it is apparent that for the condition described in (11) the frequencies of the first non-dominant pole $\omega_{p2}$ and the dominant zero $\omega_{z1}$ are almost equal and thus the effect of a low-frequency doublet in the transient response will be negligible [1]. In case of the second pole-zero pair, $\omega_{p3}$ and $\omega_{z2}$ are not dependent on the parasitic capacitances and can be located at higher frequencies by altering transconductances and compensation capacitances. Therefore, the second pole-zero cancellation will have a marginal effect on the settling time [6].

The third non-dominant pole, $\omega_{p4}$, determines the phase margin and the gain-bandwidth product. In order to have a sufficient phase margin, the gain-bandwidth product described in (10), should be limited to at least $2\sqrt{2}$ times lower than the third non-dominant pole frequency $\omega_{p4}$ [5]. Therefore, another design constraint is established as follows:

$$g_{m1} < \frac{C_m (R_a + R_3)}{2\sqrt{2}(C_2 R_2 R_3 + C_3 R_3 R_a + C_2 R_2 R_a)} \tag{13}$$

The stability of the amplifier will be ensured if the conditions in (11), (12), and (13) are well satisfied.

## 4. CIRCUIT IMPLEMENTATION

The circuit realization of the proposed amplifier is shown in Figure 3. A folded-cascode amplifier comprising of transistors $M_1$ to $M_9$ is used as the first stage. The feedforward transconductance $g_{mf1}$

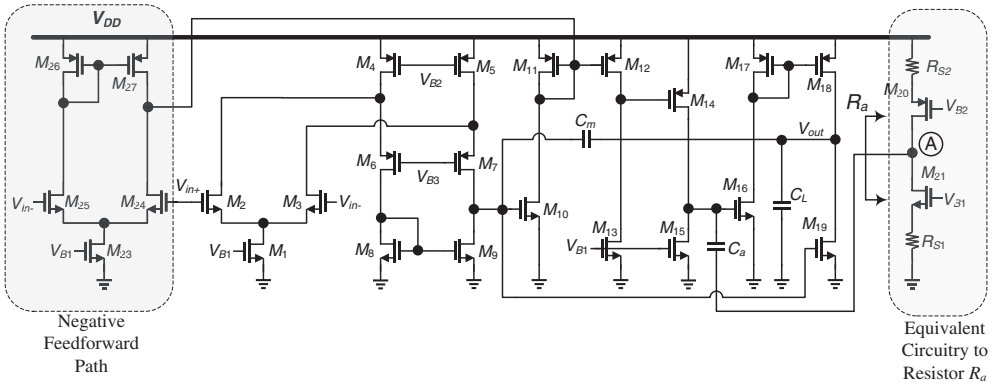


Figure 3. The circuit implementation of the proposed amplifier.



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is implemented by a differential pair consisting of transistors $M_{23}$ to $M_{27}$. The second stage is realized by a non-inverting gain stage which is comprised of transistors $M_{10}$ to $M_{13}$. Transistors $M_{14}$ and $M_{15}$ form the third stage. The last stage of the amplifier is realized by transistors $M_{16}$ to $M_{19}$ while the transconductance $g_{mf2}$ is implemented by transistor $M_{19}$.

As mentioned in the previous section, in order to perform a complete low-frequency pole-zero cancellation, the multiplication of $C_aR_a$ is needed to be high. It is evident that choosing large values for $C_a$ will decrease the slew rate and degrades the large signal performance. Furthermore, integrating large passive devices will increase the silicon die area, and thus, the fabrication cost. Here, to avoid these drawbacks, a small capacitor has been used as $C_a$ and a large resistor is used to keep a large value for the multiplication of $C_aR_a$. The large resistor $R_a$ (which may range from 1 MΩ to 2 MΩ) has been realized using an active circuit, consisting of transistors $M_{20}$ and $M_{21}$ plus two small resistors $R_{S1}$ and $R_{S2}$ as shown in Figure 3. The resistance $R_a$ is approximately equal to $\{(g_{m20}r_{ds20}R_{S2}) \parallel (g_{m21}r_{ds21}R_{S1})\}$ where $g_{m20}$ and $g_{m21}$ are the transconductances and $r_{ds20}$ and $r_{ds21}$ represent the drain-source resistances of transistors $M_{20}$ and $M_{21}$, respectively. The resistors $R_{S1}$ and $R_{S2}$ have been used to guarantee the thermal stability for the voltage of node A. The exclusion of these resistors causes the dc voltage of node A to vary widely versus the temperature variations and

Table I. Simulated circuit parameters.

| | | | | | |
|---|---|---|---|---|---|
| | | $C_L = 500$ pF | | | |
| $g_{m1}$ | 33 μA/V | $g_{mf1}$ | 92 μA/V | $R_{S1}$ | 50 kΩ |
| $g_{m2}$ | 39 μA/V | $g_{mf2}$ | 350 μA/V | $R_{S2}$ | 50 kΩ |
| $g_{m3}$ | 11 μA/V | $R_a$ | 1300 kΩ | $C_m$ | 0.28 pF |
| $g_{m4}$ | 350 μA/V | $C_a$ | 0.15 pF | $R_1$ | 5.14 MΩ |
| $R_2$ | 296 kΩ | $R_3$ | 415 kΩ | $R_4$ | 18.4 kΩ |
| $C_1$ | 1.17 fF | $C_2$ | 1.68 fF | $C_3$ | 2.27 fF |
| | | $C_L = 1000$ pF | | | |
| $g_{m1}$ | 33 μA/V | $g_{mf1}$ | 135 μA/V | $R_{s1}$ | 50 kΩ |
| $g_{m2}$ | 39 μA/V | $g_{mf2}$ | 570 μA/V | $R_{s2}$ | 50 kΩ |
| $g_{m3}$ | 11 μA/V | $R_a$ | 1300 kΩ | $C_m$ | 0.28 pF |
| $g_{m4}$ | 570 μA/V | $C_a$ | 0.15 pF | $R_1$ | 5.14 MΩ |
| $R_2$ | 296 kΩ | $R_3$ | 415 kΩ | $R_4$ | 10.5 kΩ |
| $C_1$ | 1.17 fF | $C_2$ | 1.68 fF | $C_3$ | 2.27 fF |

Table II. Device sizes used in the simulations.

| Parameter | $C_L = 500$ pF | $C_L = 1000$ pF |
|---|---|---|
| $(W/L)_1$ | 3 × 0.25μm/0.18μm | 3 × 0.25μm/0.18μm |
| $(W/L)_{2,3}$ | 3 × 0.25μm/0.18μm | 3 × 0.25μm/0.18μm |
| $(W/L)_{4,5}$ | 3 × 0.25μm/0.18μm | 3 × 0.25μm/0.18μm |
| $(W/L)_{6,7}$ | 3 × 0.25μm/0.18μm | 3 × 0.25μm/0.18μm |
| $(W/L)_{8,9}$ | 1 × 0.25μm/0.18μm | 1 × 0.25μm/0.18μm |
| $(W/L)_{10,13}$ | 1 × 0.25μm/0.09μm | 1 × 0.25μm/0.09μm |
| $(W/L)_{11,12}$ | 2 × 0.25μm/0.09μm | 2 × 0.25μm/0.09μm |
| $(W/L)_{14}$ | 2 × 0.25μm/0.09μm | 2 × 0.25μm/0.09μm |
| $(W/L)_{15}$ | 1 × 0.25μm/0.09μm | 1 × 0.25μm/0.09μm |
| $(W/L)_{16}$ | 2 × 0.5μm/0.09μm | 2 × 0.5μm/0.09μm |
| $(W/L)_{17}$ | 2 × 1μm/0.09μm | 2 × 1μm/0.09μm |
| $(W/L)_{18}$ | 6 × 1μm/0.09μm | 8 × 1μm/0.09μm |
| $(W/L)_{19}$ | 6 × 0.5μm/0.09μm | 8 × 0.5μm/0.09μm |
| $(W/L)_{20}$ | 3 × 0.25μm/2μm | 3 × 0.25μm/2μm |
| $(W/L)_{21}$ | 1 × 0.25μm/2μm | 1 × 0.25μm/2μm |
| $(W/L)_{23}$ | 7 × 1μm/0.09μm | 9 × 1μm/0.09μm |
| $(W/L)_{24,25}$ | 8 × 1μm/0.09μm | 10 × 1μm/0.09μm |
| $(W/L)_{26,27}$ | 16 × 1μm/0.09μm | 20 × 1μm/0.09μm |



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process corner cases, and thus, the small-signal parameters of the transistors $M_{20}$ and $M_{21}$ may change considerably. As a result, the location of the associated poles and zeros is altered, and this affects the amplifier's frequency response.

In order to further increase the gain-bandwidth product, the parasitic capacitances at output nodes of each stage should be small. In Figure 1, it is clear that the parasitic capacitance of the feedforward stage $g_{mf1}$ is added to the capacitance of the output node of the second stage. Therefore, the pole associated with this node will be pushed towards the origin and will decrease the gain-bandwidth product. To avoid this, the positive feedforward path $g_{mf1}$ is not directly connected to the output node of the second stage. Instead, as shown in Figure 3, a negative feedforward stage consisting of transistors $M_{23}$ to $M_{27}$ is connected to the gate of the current mirror transistors $M_{11}$ and $M_{12}$, and this structure acts as the positive feedforward path with the transconductance of $g_{mf1}$.

Table III. The simulated performance summary.

| | Value | | | | | |
|---|---|---|---|---|---|---|
| | TT @ 27 °C | | FF @ −40 °C | | SS @ 85 °C | |
| Parameter | $C_L = 500$ pF | $C_L = 1000$ pF | $C_L = 500$ pF | $C_L = 1000$ pF | $C_L = 500$ pF | $C_L = 1000$ pF |
| DC gain (dB) | 92.6 | 92.1 | 88.9 | 88.1 | 93.8 | 93.4 |
| GBW (MHz) | 18 | 15.1 | 18.5 | 15.6 | 15.4 | 12.9 |
| Phase margin (degree) | 74.3 | 75 | 71.9 | 72.5 | 76.4 | 77.5 |
| Power (μW) | 40.9 | 55.2 | 47 | 63.3 | 37.4 | 50.5 |
| Slew rate ($SR^+/SR^-$) (V/μs) | 1.28/2.23 | 0.85/1.71 | 1.79/2.91 | 1.19/2.21 | 0.89/1.62 | 0.59/1.18 |
| 1% Settling time ($t_s^+/t_s^-$) (ns) | 680/403 | 870/433 | 469/309 | 608/334 | 1020/502 | 1348/603 |

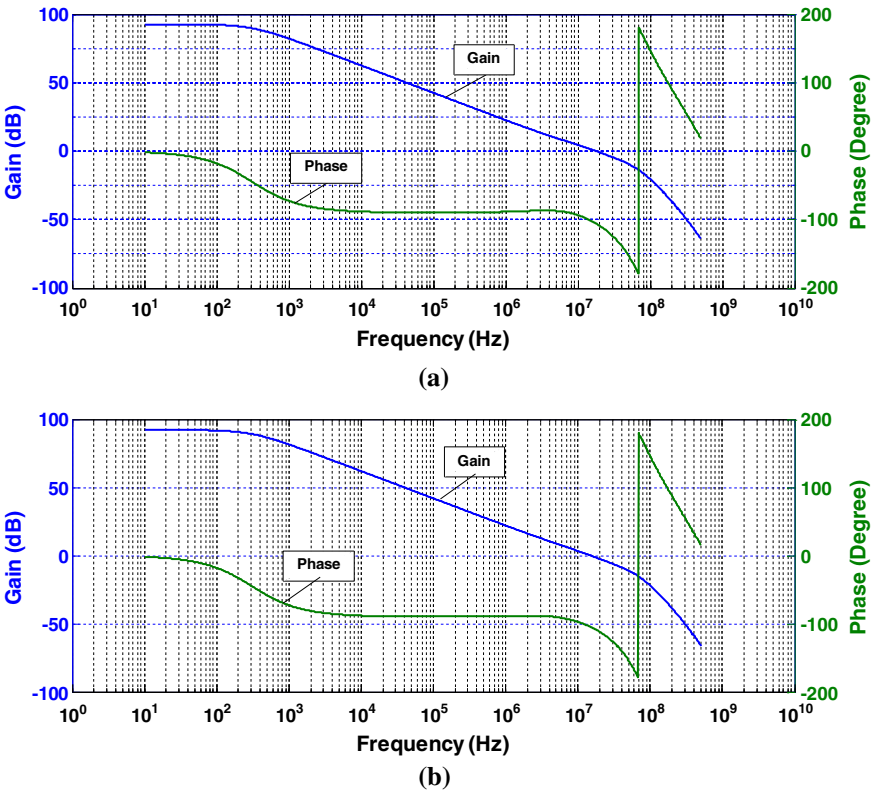


Figure 4. Simulated open-loop frequency response: a) $C_L = 500$ pF and b) $C_L = 1000$ pF.



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## 5. SIMULATION RESULTS

The proposed four-stage amplifier has been designed and simulated in a standard 90 nm CMOS process using HSPICE. The amplifier uses a single 0.9 V power supply, drives a 500 pF load capacitance, and achieves a gain-bandwidth product of about 18 MHz while dissipating only 40.9 μW power. For a larger loading capacitance of 1000 pF, the amplifier has a gain-bandwidth product of 15.1 MHz and consumes 55.2 μW of power. The simulated transconductance of each stage and the values of resistors and capacitors are summarized in Table I.

The aspect ratio of transistors is reported in Table II, and Table III shows the simulation results for different corner cases with a temperature variation spanning from −40°C to 85°C. The simulated open-loop frequency response is shown in Figure 4. Also, Figure 5 shows the large signal transient response to a 350-mV input step.

In order to prove the feasibility of the presented amplifier and to show that the pole-zero cancellations are almost insensitive to the device mismatches [21], circuit level Monte-Carlo simulations have been carried out. The distributions for the gain-bandwidth product and the phase margin over 500 iterations are shown in Figure 6. It can be seen that the performance of the amplifier is not changed considerably against process variations. The proposed topology is compared with some previously published multistage amplifiers using four figures of merit, $FOM_S$, $FOM_L$, $IFOM_S$, and $IFOM_L$, described by:

$$FOM_S = \frac{\omega_{GBW} \times C_L}{\text{Power}} \tag{14}$$

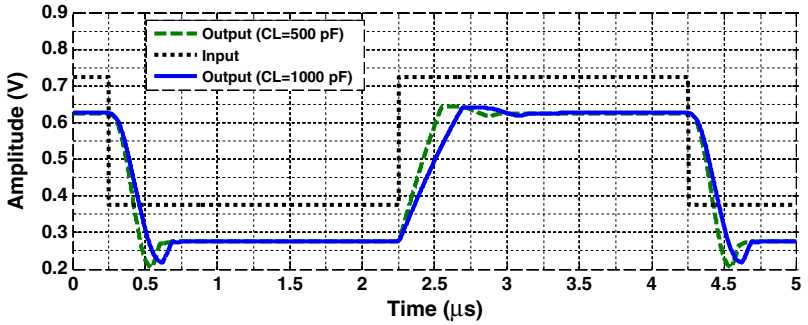


Figure 5. Simulated transient response.

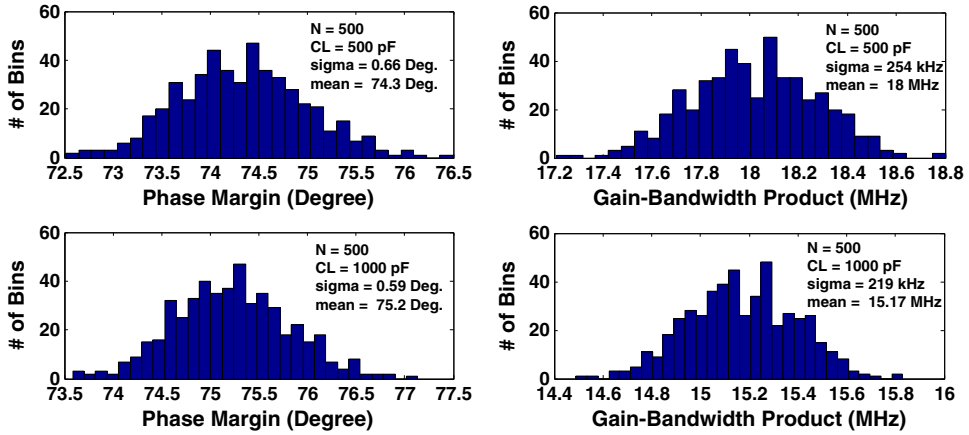


Figure 6. Monte-Carlo simulation results of the gain-bandwidth product and phase margin.



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Table IV. Comparison of the different multistage amplifiers.

| Reference | $V_{DD}$ (V) | $I_{DD}$ (mA) | $C_L$ (pF) | GBW (MHz) | SR (V/μs) | $FOM_S$ (MHz×pF/mW) | $FOM_L$ (V/μs×pF/mW) | $IFOM_S$ (MHz×pF/mA) | $IFOM_L$ (V/μs×pF/mA) | $FOM_A$ | CMOS technology | Compensation capacitance (pF) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| [6] | 1.5 | 0.02 | 150 | 4.4 | 1.8 | 22000 | 9000 | 33000 | 13500 | 2.84 | 0.35 μm | 1.6 |
| [7][a] | 2 | 0.34 | 20 | 0.61 | 2.5 | 18 | 74 | 36 | 148 | N.A. | 2 μm | N.A. |
| [8][b] | 1.5 | 0.16 | 500 | 27.27 | 0.84 | 57531 | 1782 | 85218 | 2640 | 13.68 | 0.18 μm | 0.7 |
| [17][ba] | 1 | 1.4 | 500 | 40.2 | 17.52 | 14357 | 6257 | 14357 | 6257 | 1.28 | 0.12 μm | 17.6 |
| [22][b] | 2 | 0.07 | 500 | 1.2 | 0.8 | 4286 | 2857 | 8572 | 5714 | N.A. | 0.35 μm | 12.5 |
| [9] | 1.5 | 0.03 | 150 | 2.85 | 1.035 | 9500 | 3450 | 14250 | 5175 | 1.24 | 0.35 μm | 2.02 |
| [23][b] | 1.5 | 0.115 | 500 | 12.9 | 2.13 | 37283 | 6156 | 55925 | 9234 | 5.65 | 0.35 μm | 1 |
| [24][b] | 1.5 | 0.014 | 150 | 1.8 | 0.7 | 12857 | 5000 | 19286 | 7500 | 2.3 | 0.35 μm | 2 |
| [5] | 2 | 0.13 | 800 | 3.6 | 1.7 | 22154 | 5231 | 22154 | 10461 | 2.68 | 0.35 μm | 2.2 |
| This work[ba] | 0.9 | 0.045 | 500 | 18 | 1.75 | 220049 | 21393 | 200000 | 19444 | 16.95 | 90 nm | 0.43 |
| This work[ba] | 0.9 | 0.061 | 1000 | 15.1 | 1.28 | 273551 | 23188 | 247541 | 20983 | 19 | 90 nm | 0.43 |

[a]Four-stage amplifier.
[b]Simulation results.



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$$FOM_L = \frac{SR \times C_L}{\text{Power}} \tag{15}$$

$$IFOM_S = \frac{\omega_{GBW} \times C_L}{I_{\text{dd}}} \tag{16}$$

$$IFOM_L = \frac{SR \times C_L}{I_{\text{dd}}} \tag{17}$$

Although the two figures of merit described in (14) and (15) are more commonly used, they depend on the supply voltage, and both the gain-bandwidth product and the slew rate depend upon the quiescent current flowing in the relevant transistors. Therefore, to have a more reasonable comparison, two other figures of merit defined by (16) and (17) are used. All the above figures of merit are related to the current drawn from the supply voltage, and thus they are dependent upon the particular amplifier structure and the utilized process. Here, in order to have a more general comparison, another figure of merit described in (18) is also used [10,16]:

$$FOM_A = \frac{\omega_{GBW} \times \mathrm{C_L}}{g_{m1} + g_{m2} + g_{m3} + g_{m4} + g_{m,comp}} \tag{17}$$

where gm,comp is the sum of compensation network transconductances. The results are summarized in Table IV. As is seen, the proposed amplifier outperforms all of the previously reported amplifiers and has high practicality for low-voltage and low-power applications.

## 6. CONCLUSIONS

A four-stage amplifier with a novel frequency compensation scheme was proposed. The compensation topology is based on both pole splitting and pole-zero cancellations, and as was proved, this leads to a better performance while consuming lower power than most of the previously reported works. Also, this amplifier requires small amounts of capacitance for the frequency compensation task. Extensive simulations have been carried out to prove the robustness of the proposed amplifier. Finally, comparing the simulation results with some latest published works based on five figures of merit shows that the overall performance of the proposed amplifier is considerably improved. As an example, the average FOM is about 14 times larger than that reported in [17] which is a four-stage amplifier and uses an almost similar technology. Therefore, the proposed amplifier is well-suited for low-voltage and low-power nanometer applications.

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