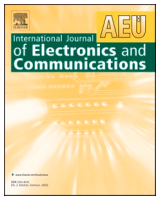
Int. J. Electron. Commun. (AEÜ) 201 (2025) 155976

Contents lists available at ScienceDirect

International Journal of Electronics and Communications

journal homepage: www.elsevier.com/locate/aeue



Regular paper

A closed-loop neural recording analog front-end with low noise and automatic gain control amplifiers

Mohammadamin Mohtashamnia, Mohammad Yavari *

Integrated Circuits Design Laboratory, Department of Electrical Engineering, Amirkabir University of Technology (Tehran Polytechnic), 424 Hafez Ave., P.O. 15875-4413, Tehran 15914, Iran

ARTICLE INFO

Keywords:
Closed-loop neural recording
Low-noise amplifier
Low-power amplifier
Stimulation artifacts
Automatic gain control
CMOS integrated circuits

ABSTRACT

This paper presents a novel analog front-end including both an analog circuit and an analog-to-digital converter (ADC) for closed-loop neural recording. The analog part contains a low-noise amplifier (LNA), an automatic gain control amplifier (AGCA), and a voltage buffer. For noise and power performance optimization, a novel LNA structure is introduced. The proposed LNA employs two current mirror amplifiers, both incorporating class-AB output stages. Additionally, the first stage utilizes source-degenerated current mirrors. Using the AGCA allows for dynamic adjustment of the voltage gain during periods without artifacts, which reduces the precision requirements of the ADC. This improves overall system efficiency by optimizing signal amplification while minimizing the ADC's workload. A 10-bit successive approximation register (SAR) ADC is incorporated to digitize the amplified signals. To judge the operation of the suggested circuit, extensive circuit level simulations were conducted using 180 nm TSMC CMOS technology within the Cadence environment. The circuit operates from a 1.8 V power supply and at 37 °C, consuming 9 μW of power while processing signals with a 10 kHz bandwidth. It reaches a dynamic range of 81.83 dB and a maximum signal-to-noise and distortion ratio (SNDR) of 58.40 dB, demonstrating competitive performance when compared to existing solutions in the field.

1. Introduction

Nowadays, many individuals around the world are facing health issues like paralysis, Alzheimer's, and other neural disorders. Some specialists have tried using drug therapies or surgery to address these conditions; however, in some patients these approaches are not very effective. In such cases, neural stimulation can be beneficial [1]. Neural stimulation modulates brain activity by delivering controlled electrical pulses to targeted regions. Conventional therapies depend on continuous, pre-programmed stimulation, which, while effective, may lead to adverse side effects [2] and diminish in usefulness over time due to brain plasticity and other factors. To address this, neuroscientists have introduced closed-loop stimulation, where stimulation factors are adjusted immediately based on neural signal feedback. This guarantees that stimulation occurs only in critical situations and at the appropriate strength, minimizing the risks associated with open-loop systems while maximizing healing outcomes. The feedback mechanism also allows stimulation to adapt to brain changes, ensuring lasting treatment effectiveness. Additionally, closed-loop systems serve as valuable tools for studying brain function. In the near future, neuromodulation systems will demand the capability to support hundreds of recording channels for better efficiency.

Fig. 1 illustrates a sample closed-loop neural recording system. The cerebrospinal fluid (CSF) high conductivity and coupling between electrode pathways and recording locations can result in large stimulation signals at the recording sites. These artifacts at the recording sites exhibit an average amplitude up to approximately 300 mV_p in common mode and 50 mV_p in differential mode [3].

Local field potentials (LFPs) span the frequency range from 1 to 200 Hz with a peak amplitude of approximately 1 mV_p, while action potentials (APs) cover a range from 200 Hz to 10 kHz with a peak amplitude of 100 μV_p. [3,4]. Thermal noise and biological backgrounds picked up by the electrodes are about 10 μV_{rms} [5].

The characteristics of the electrode must also be considered. As shown in Fig. 2, a simple RC circuit models the electrode. R_s represents the series resistance of the metal connection, while R_{el} and C_{el} represent the metal-electrolyte interface, and their values differ significantly based on the electrode's target bandwidth, manufacturer specifications, and surface properties. Wet electrodes are unsuitable for long-term use due to their reliance on gel. In contrast, dry electrodes have been utilized

* Corresponding author.
E-mail address: myavari@aut.ac.ir (M. Yavari).

https://doi.org/10.1016/j.aeue.2025.155976
Received 15 April 2025; Accepted 31 July 2025
Available online 7 August 2025

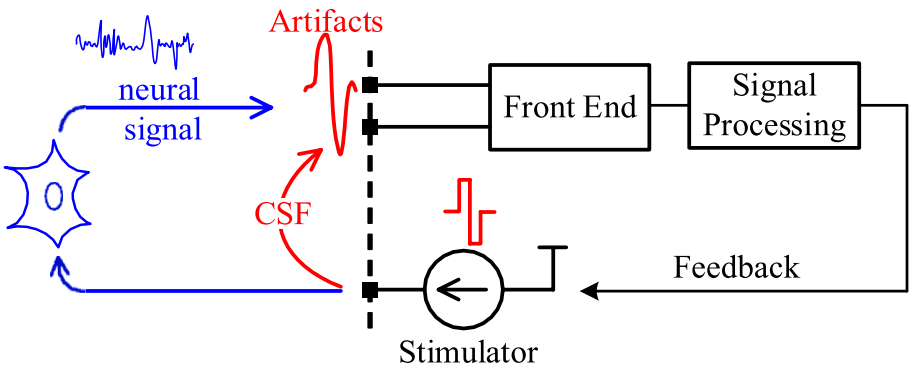


Fig. 1. A closed-loop neural recording system block diagram [3].

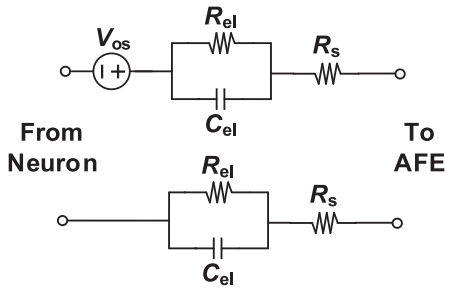


Fig. 2. Equivalent circuit of typical neural-recording electrodes.

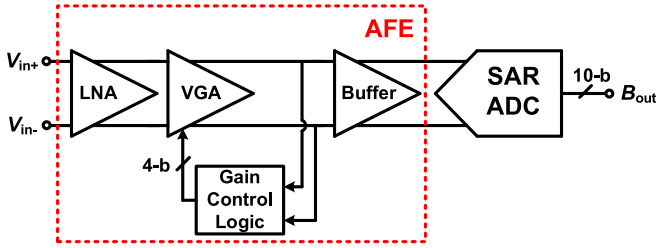


Fig. 3. Overall structure of the proposed analog front-end and ADC.

as an alternative to wet electrodes because of user comfort and continuous neural recording. However, one challenge is the high impedance of dry electrodes [6].

Another issue is the electrode offset voltage. This voltage is caused by electrochemical effects at the electrode-tissue interface. For differential recordings using similar electrodes, the amplitude of the offset voltage can range up to 50 mV_p [7]. The offset in the electrode can induce DC currents due to the interface circuit's limited DC impedance. If these currents persist, they can harm the surrounding tissue over time.

As mentioned already, A key difficulty in closed-loop neural signal recording is the presence of artifacts at the recording sites. If not properly addressed, these artifacts can easily saturate the circuit and disrupt the recording process. As noted in [8], gain reduction is an effective method for preventing the neural recorder from saturation. However, a very low gain presents problems for designing the analog-to-digital converter (ADC). Due to the presence of amplified artifacts along with neural signals, a high effective number of bits (ENOB) and signal-to-noise and distortion ratio (SNDR) are needed for the ADC to support a wide range of input signals.

In [9–14], neural signals were digitized without any amplification. In [14], a continuous-time delta-sigma modulator (CTDSM) was used for digitizing neural signals, incorporating a modified integrator based on an instrumentation amplifier (IA). This design improves input impedance, common-mode rejection ratio (CMRR), and linearity. Additionally, the current reuse of the modulator's feedback digital-to-analog converter (DAC) to bias the integrator reduces the power consumption significantly. In [15], a neural recording amplifier was integrated with a monotonic successive approximation register (SAR) ADC and an error-feedback (EF) noise-shaping path to create an EF NS-SAR ADC. By reusing the amplifier, the system achieved process-voltage-temperature (PVT) robustness, enhanced gain, and reduced thermal noise. These two methods (low-gain amplification and direct conversion) are not power-efficient when artifacts are not present, considering the use of high-precision ADCs.

Due to the periodic nature of stimulation artifacts, an effective anti-artifact approach is to turn off the input of the recording circuit during neural stimulation. This technique is known as blanking [16–19]. In these structures, the input switches are controlled by a flag signal when an artifact is detected at the recording site. As a result, the artifacts cannot pass through. However, the blanking technique results in the loss of information related to the stimulation. Similar to blanking, the soft reset technique is also used to avoid encountering artifacts [20,21]. This method prevents circuit saturation by controlling the low cut-off frequency and consequently the gain of the neural amplifier. For a capacitively coupled amplifier, the high-pass cut-off frequency is adjusted by controlling a pseudo-resistance in the DC-feedback loop. Since artifacts are periodically generated by the stimulation current and the stimulation duration is much shorter than the entire period of signal acquisition, it is better to amplify the neural signal with high gain when artifacts are absent to improve circuit power efficiency. This method for dealing with artifacts has been employed in [22], which utilizes continuous-time zoom ADC and employs a two-step conversion. The output data from the first step is passed to the digital auto-ranging (DAR) block. DAR calculates the slope of the input signal and adjusts the gain accordingly. In this way, the saturation of the front-end circuit is prevented at the expense of increasing complexity. The use of programmable gain amplifiers (PGAs) and reconfigurable structures is common in applications that require band selection, as demonstrated in [23]. This technique is also effective for handling signals with varying amplitudes, as shown in [24]. In such approaches, when a stimulation artifact is detected, the voltage gain of the analog front-end is reduced. Therefore, one of the most critical aspects is controlling the switches in a way that prevents amplifier saturation during the artifact period.

In this paper, an analog front-end circuit is presented to convert neural signals into the digital domain. The analog front-end includes a low-noise amplifier (LNA), an automatic gain control amplifier (AGCA) which contains a variable gain amplifier (VGA) along with a gain control logic circuit, and a voltage buffer. After amplification, the signal undergoes digitization by the ADC. The subsequent sections of this paper are organized as follows. Section 2 provides an introduction to the structure of the proposed circuit and gives details of each part. Simulation results are gathered in Section 3, and the paper concludes in Section 4.

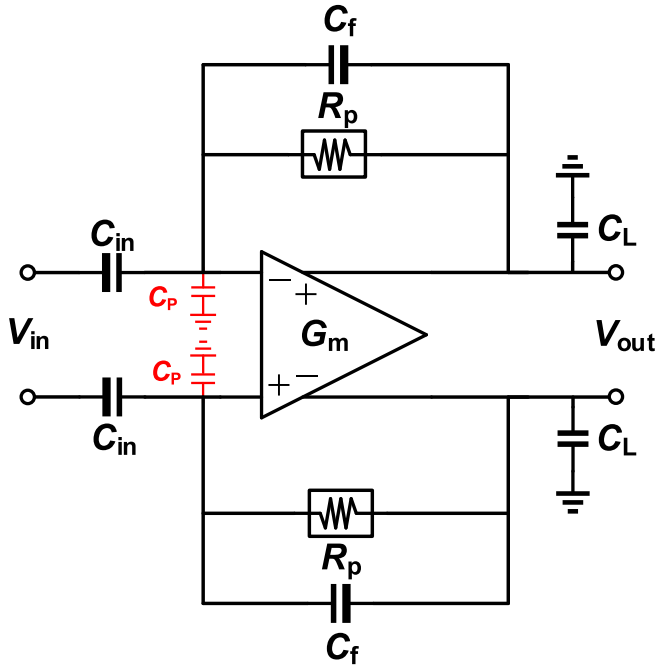


Fig. 4. Conventional capacitive-feedback amplifier.

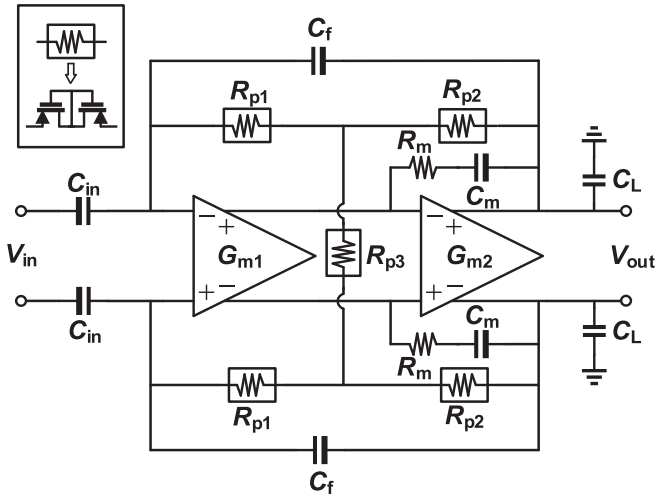


Fig. 5. Proposed structure for the low-noise amplifier.

2. The proposed analog front-end and ADC

2.1. Overall structure

The proposed analog front-end circuit for closed-loop signal recording is shown in Fig. 3. To manage stimulation artifacts, an automatic gain control technique is employed. Since controlling the bandwidth, stability, and noise performance of a variable-gain amplifier is challenging, a low-noise amplifier with a constant gain is used before this stage. This is to ensure that it generates minimal noise itself while significantly reducing the noise of subsequent stages. Additionally, since the analog circuit must drive the capacitive load of the ADC, it is preferable to place an analog buffer stage after the variable-gain amplifier to enhance the driving power of the front-end analog circuit. Finally, an analog-to-digital converter is included.

2.2. Low noise amplifier

The primary sources of noise within the bandwidth of neural signals are flicker and thermal noise. Increasing the transistor dimensions, particularly the input pair transistors, is one of the approaches to reduce flicker noise [25]. Chopping technique is one effective method for reducing noise and improving the quality of recorded signals in neural signal recording systems. This technique minimizes low-frequency noise and offset by phase-shifting the input signal. Chopping has been used to improve linearity and reduce noise in neural signal recording systems in [3,9,10,26]. However, this technique also has drawbacks, including reduced input impedance and increased power consumption. To address these challenges, certain methods need to be employed. In [27,28], positive feedback is exploited to enhance the input impedance of the circuit, but this method is not effective in circuits with bandpass characteristics and does not enhance the input impedance at frequencies near DC, making it unsuitable for this application. Additionally, in [29], an auxiliary path for pre-charging the input capacitors is used, with the increased input impedance achieved by lowering the current supplied by the input. In [30], a current feedback amplifier, rather than a capacitive feedback amplifier, is employed alongside a feed-forward path to significantly increase the input impedance. But, tuning the voltage gain in this architecture presents a challenge. Moreover, these methods also result in increased input noise and power dissipation. An alternative technique for reducing circuit noise is the source degeneration technique as used in [31,32]. In this method, the simple current mirrors are replaced with a source-degenerated cascode current mirrors. By appropriately selecting the degeneration resistors, the noise produced by the degenerated current mirror, primarily from the resistors, can be significantly reduced compared to the MOS transistor noise at the same current.

In recent years, many amplifiers for neural signals have been introduced, among which the capacitive-feedback structure is one of the most popular [29,31,33,34]. Fig. 4 shows the general schematic of this structure. In this structure, R_p is a pseudo-resistor and is employed to establish DC feedback. Additionally, these resistances play a crucial role in determining the high-pass frequency. The gain in this structure is fixed by the input to the feedback capacitors ratio. Other characteristics of this amplifier (low and high cut-off frequencies, and input-referred noise) are as follows:

$$f_L = \frac{1}{2\pi R_p C_f} \tag{1}$$

$$f_H = \frac{C_f G_m}{2\pi C_{in} C_L} \tag{2}$$

$$\overline{V_{n.in}^2}(f) = \overline{V_{n.OTA}^2}(f)\left(\frac{C_{in}+C_f+C_P}{C_{in}}\right)^2 + 2\overline{V_{n.Rp}^2}(f)\left(\frac{C_f}{C_{in}}\frac{f_L}{f}\right)^2 \tag{3}$$

where $V_{n,OTA}^2$ and $V_{n,Rp}^2$ represent the input-referred noise of the operational transconductance amplifier (OTA) and the noise contribution of the pseudo resistor, respectively. The parasitic input capacitor of the amplifier (C_P) should be as small as possible. Additionally, this stage must tolerate common-mode artifacts at the input, requiring a wide input common-mode range. Therefore, a suitable architecture, such as a rail-to-rail, folded-cascode, or current mirror OTA, should be used to ensure proper performance. Furthermore, the desired amplifier should have a high output swing. Given the need for both high gain and a wide output swing, a two-stage structure is necessary. In [35], a novel method for DC feedback and biasing the input pairs is proposed, which significantly reduces the low cut-off frequency and improves linearity. However, it is sensitive to OTA offset, which may degrade the amplifier's performance. In [36], to address the nonlinearity of pseudo-resistors, a very-low transconductance OTA is employed as a replacement. However, the limited input range of the VLT OTA poses a challenge for

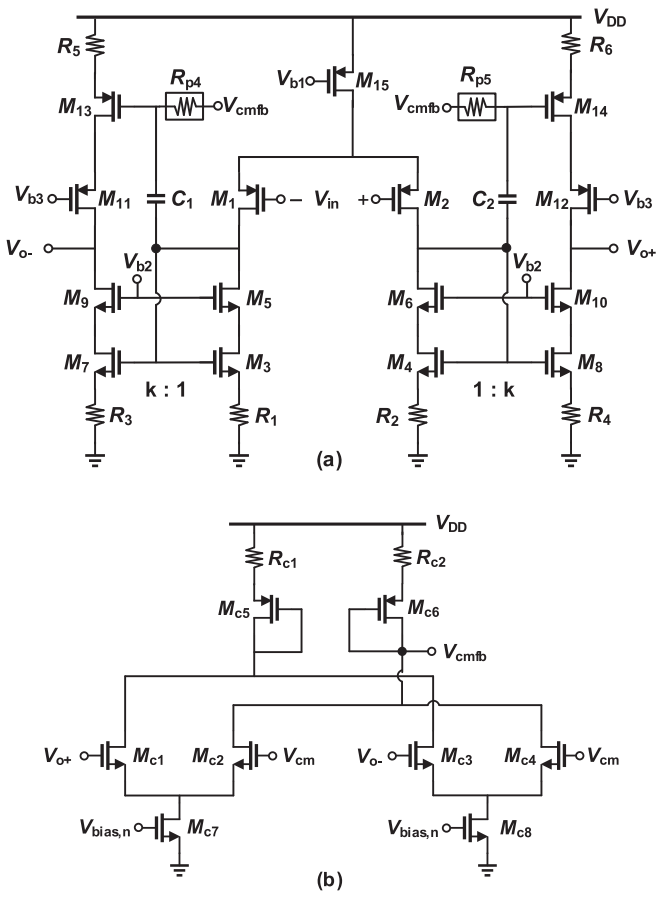


Fig. 6. (a) First stage of low-noise amplifier and (b) its CMFB amplifier.

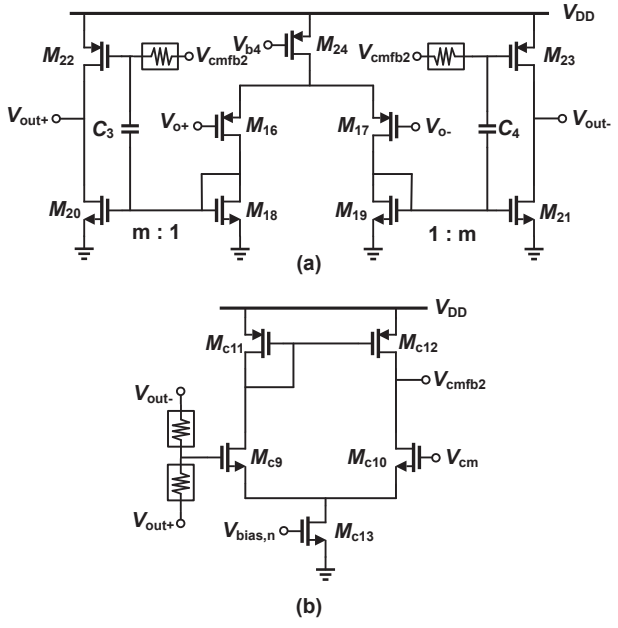


Fig. 7. (a) Second stage of the low-noise amplifier and (b) its CMFB amplifier.

designers.

Additionally, considering relation (3) and the gain relationship, achieving a relatively high gain requires a large input capacitor. In [37],

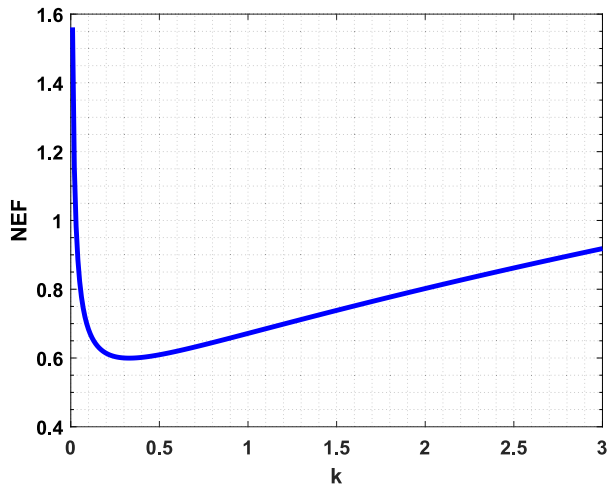


Fig. 8. Calculated NEF for different values of *k*.

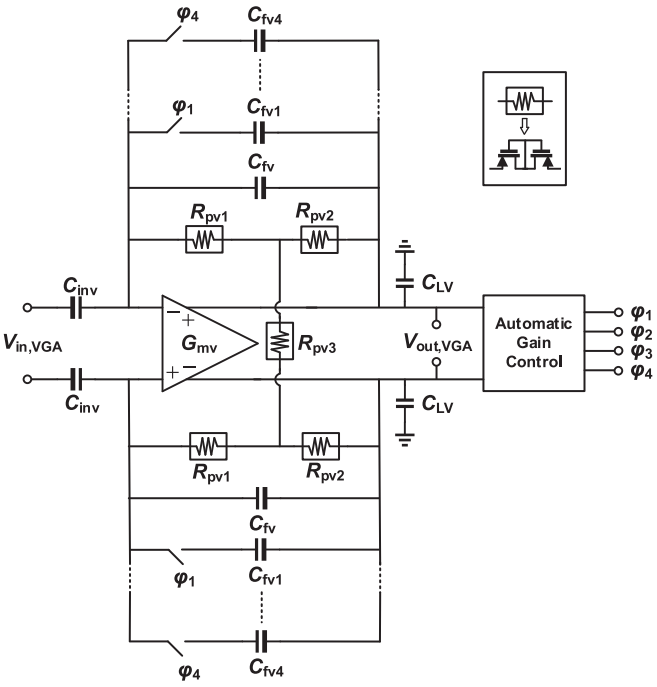


Fig. 9. Structure of the variable-gain amplifier and automatic gain control.

this is achieved without requiring extensive die area by using an attenuator in the feedback path. However, in closed-loop systems, this technique is unnecessary.

T-network capacitors have been used in [38] to reduce input capacitance and save area. Similarly, in [39], a T-network is employed in the DC feedback path to lower the high-pass corner frequency. However, this approach may compromise stability due to the presence of positive feedback.

The proposed structure for the LNA is depicted in Fig. 5. In this structure, instead of using pseudo-resistors in the conventional manner, a novel method is employed to establish DC feedback. In this method, the pseudo-resistor R_{p1} senses only a portion of the OTA's total gain, resulting in a larger Miller resistance at the OTA's input. This significantly reduces the low cut-off frequency. In this structure, the positive

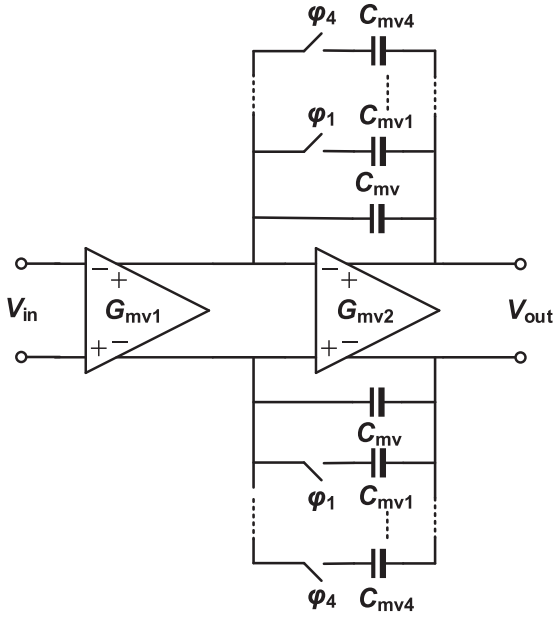


Fig. 10. Structure of the two-stage OTA used in the variable gain amplifier.

feedback path consists of R_{p2} and R_{p3}, while the negative feedback path includes only R_{p2}. As a result, the positive feedback is always weaker than the negative feedback, reducing stability concerns. For a more precise analysis, the low-frequency pole is calculated as follows:

$$f_L = \frac{1}{2\pi C_f\left(\left(R_{p1}+R_{p2}\right)+\frac{2R_{p2}R_{p1}}{R_{p3}}\right)} \tag{4}$$

In the structure shown in Fig. 5, if $R_{p1} = R_{p2} = A \times R_{p3}$, the low cut-off frequency can be obtained as:

$$f_L = \frac{1}{2\pi C_f R_{p1} \times 2(1+A)} = \frac{f_{L0}}{(1+A)} \tag{5}$$

According to relation (5) the low cut-off frequency is $(A + 1)$ times smaller when R_{p3} is present compared to when R_{p3} is absent (i.e., $R_{p3} = \infty$). The input-referred noise in this structure can be calculated as:

$$\overline{V_{n.in}^2}(f) = \overline{V_{n,OTA}^2}(f)\left(\frac{C_{in}+C_f+C_P}{C_{in}}\right)^2 + \frac{2}{(A+1)^2}\left(\overline{V_{n.Rp1}^2}(f)(2A+1)^2 + \overline{V_{n.Rp2}^2}(f) + A^2\overline{V_{n.Rp3}^2}(f)\right)\left(\frac{C_f}{C_{in}}\frac{f_{L0}}{f}\right)^2 \tag{6}$$

where, $V_{n,OTA}^2$ and $V_{n,Rp1\text{-}3}^2$ represent the input-referred noise of OTA and the noise contribution of the corresponding pseudo resistors, respectively. "A" denotes the ratio of $R_{p1,2}$ to R_{p3}. Therefore, by using this DC feedback method, the high-pass cut-off frequency can be reduced without the need for large capacitors. However, according to relation (6), increasing "A" in the T-network within the DC feedback path can approximately increase the input-referred noise power density by up to 4× (for $A \to \infty$). Nevertheless, due to the low-pass behavior of the pseudo-resistor noise, a suitable selection of f_{L0} can mitigate this effect. Additionally, reducing the capacitor size while maintaining a constant voltage gain –as described by relation (6)– increases the input-referred noise (IRN). Therefore, a trade-off between noise, gain, and area must be carefully considered.

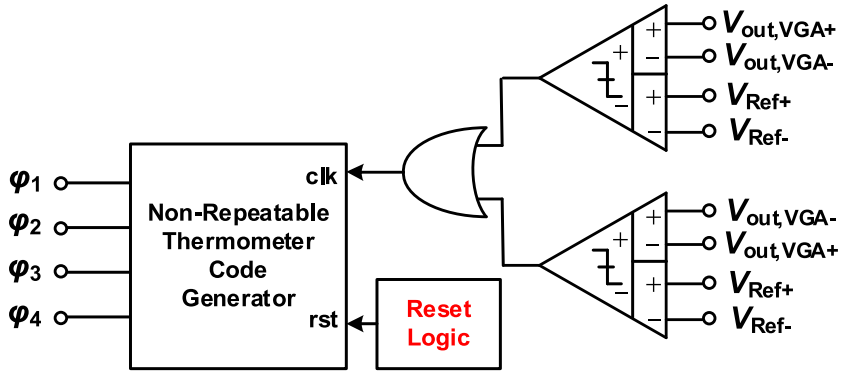


Fig. 11. The gain control circuit in the automatic gain control amplifier.

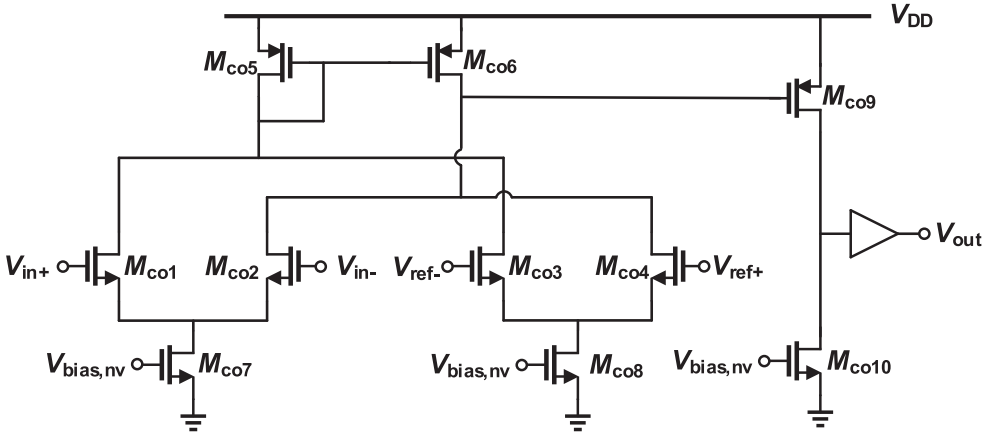


Fig. 12. The static comparator in the automatic gain control amplifier.

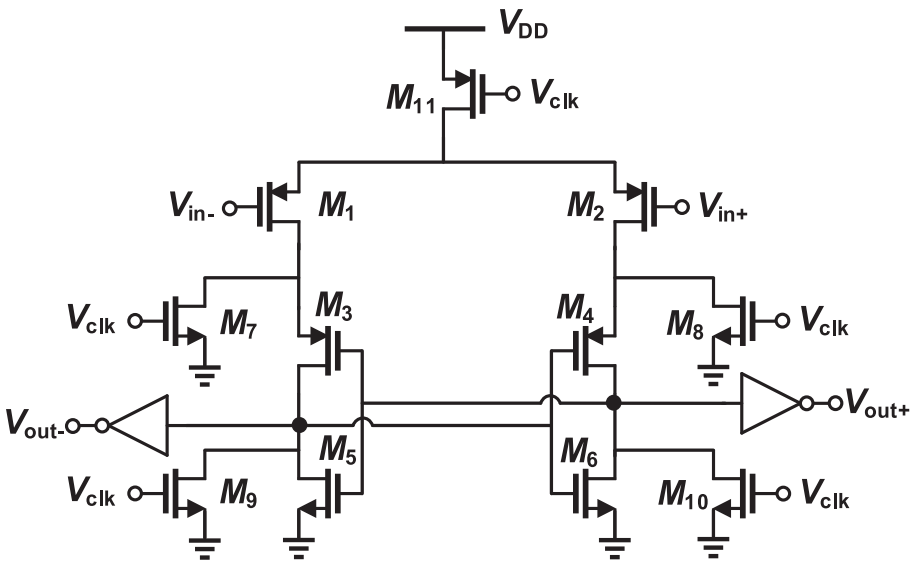


Fig. 13. The strong-arm latch comparator.

Table 1
Simulated device parameters.

Transistor	Size (M × W/L)	Transistor	Size (M × W/L) or Value
$M_{1,2}$	20 × 30.0 μm/0.5 μm	$M_{c7,8}$	1 × 8.0 μm/10.0 μm
$M_{3,4}$	5 × 4.0 μm/4.0 μm	$M_{c9,10}$	1 × 10.0 μm/1.0 μm
$M_{5,6}$	5 × 1.5 μm/4.0 μm	$M_{c11,12}$	1 × 1.5 μm/0.5 μm
$M_{7,8}$	2 × 4.0 μm/4.0 μm	M_{c13}	1 × 7.5 μm/10.0 μm
$M_{9,10}$	2 × 1.5 μm/4.0 μm	C_{in}	9.6 pF
$M_{11,12}$	1 × 10.0 μm/2.0 μm	C_f	0.6 pF
$M_{13,14}$	5 × 20.0 μm/0.5 μm	C_m	10.8 pF
M_{15}	1 × 4.0 μm/20.0 μm	R_m	0.6 MΩ
$M_{16,17}$	1 × 8.0 μm/2.0 μm	$R_{1,2}$	1 MΩ
$M_{18,19}$	1 × 3.0 μm/1.0 μm	$R_{3,4}$	2.5 MΩ
$M_{20,21}$	5 × 3.0 μm/1.0 μm	$R_{5,6}$	0.25 MΩ
$M_{22,23}$	3 × 5.0 μm/1.0 μm	$R_{c1,2}$	1 MΩ
M_{24}	1 × 1.1 μm/20.0 μm	$C_{1,2}$	2 pF
$M_{c1\text{-}4}$	1 × 5.0 μm/0.5 μm	$C_{3,4}$	2 pF
$M_{c5,6}$	5 × 5.0 μm/0.5 μm	A	2.5

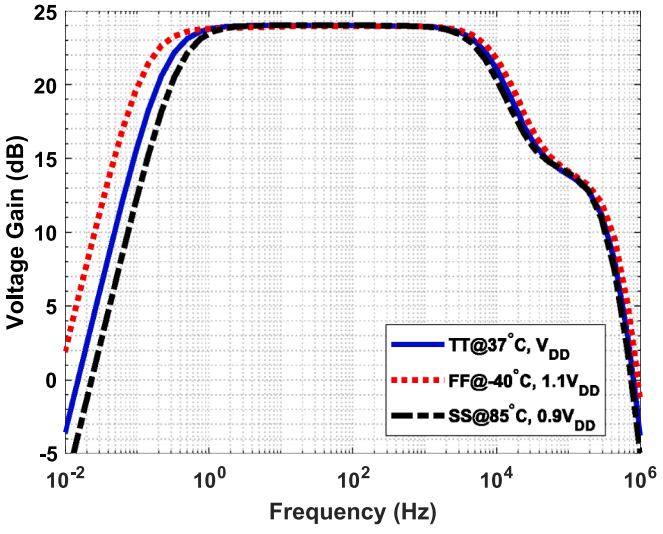


Fig. 14. The proposed low-noise amplifier frequency response.

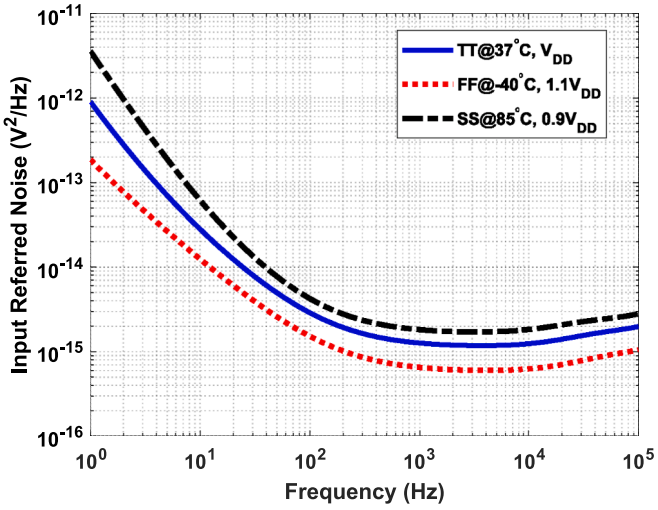


Fig. 15. Input-referred noise PSD of the low-noise amplifier.

The DC output voltage for this configuration is given by:

$$V_{out}(@DC) \approx \frac{R_{p2}+R_{p3}}{R_{p3}}\left(V_{os1}+\frac{V_{os2}}{G_{m1}R_{o1}}\right) \quad (7)$$

where V_{os1} and V_{os2} are the input-referred offset voltages of the first and second stages, respectively, and G_{m1} and R_{o1} are the transconductance and output resistance of the first stage. This equation indicates that increasing R_{p3} improves the output offset performance. However, a larger R_{p3} also raises the high-pass corner frequency, introducing a trade-off between output offset and low-frequency response.

When choosing the first-stage structure, inverter-based OTAs, such as those used in [3], or telescopic OTAs, as in [34], provide high power and noise efficiency. However, they are not effective at mitigating common-mode artifacts. Thus, circuits to remove the common-mode input signal, as in [29], are necessary, increasing power consumption and circuit noise. Fig. 6 illustrates the schematic of the proposed LNA's first stage

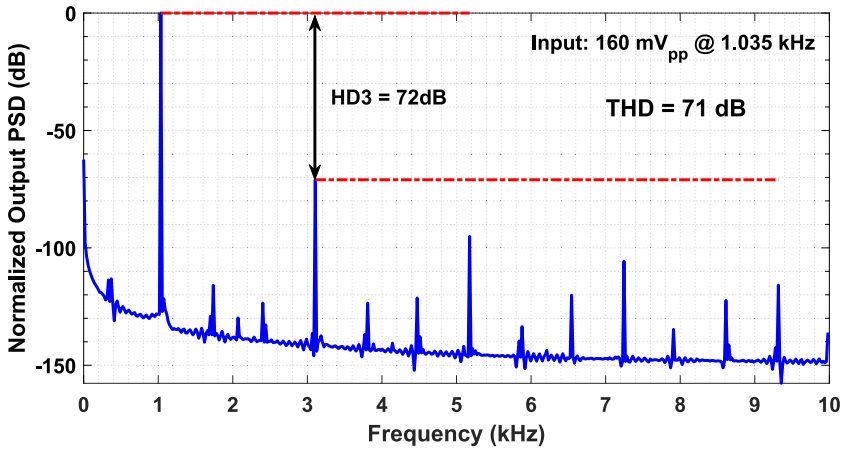


Fig. 16. The suggested LNA harmonic distortion for a 160 mV_{pp} input signal at 1.03515625 kHz.

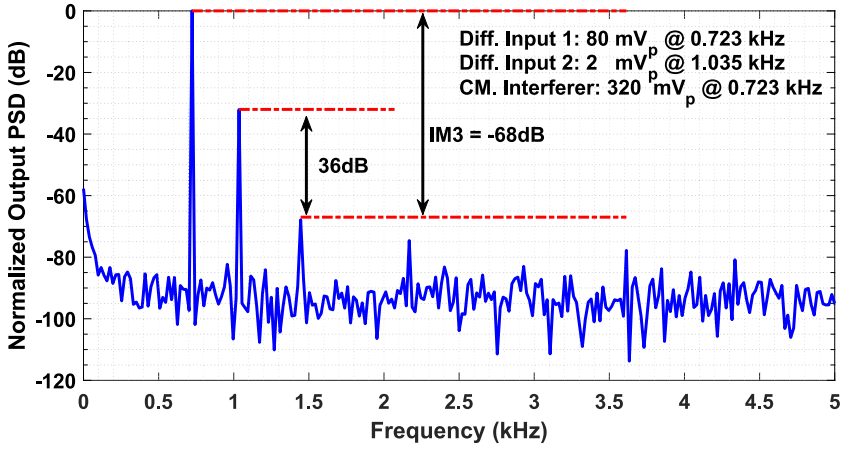


Fig. 17. Output PSD of the suggested LNA in two-tone test.

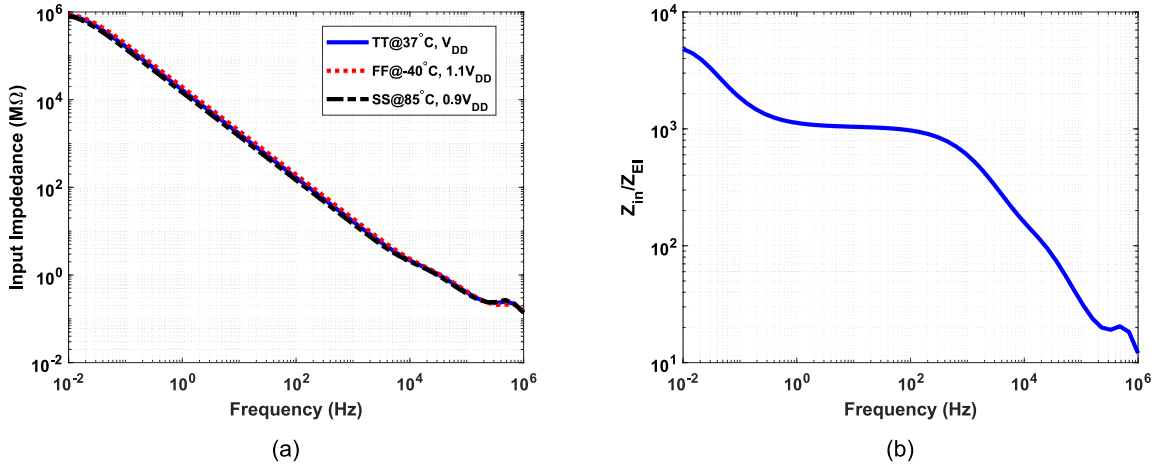


Fig. 18. (a) Input impedance of the proposed LNA and (b) its ratio to the electrode impedance.

and common-mode feedback (CMFB) circuit. A fully-differential current-mirror amplifier, implemented by transistors M_1–M_{15}, is selected for its wide input common-mode range. Source degeneration resistors (R_1–R_6) are used with transistors $M_{3,4}$, $M_{7,8}$, and $M_{13,14}$ to minimize flicker and thermal noises, balancing noise and input range. The class-AB output stage is achieved through high-pass path formed by the RC network ($C_{1,2}$ and $R_{p4,p5}$). All transistors operate in the weak-inversion (sub-threshold) region for power efficiency [40]. The CMFB circuit determines the common-mode output voltage. To ensure proper operation under different process-voltage-temperature conditions, a suitable biasing circuit is crucial. In the proposed LNA, a simple constant current biasing circuit is employed. This circuit incorporates wide-swing

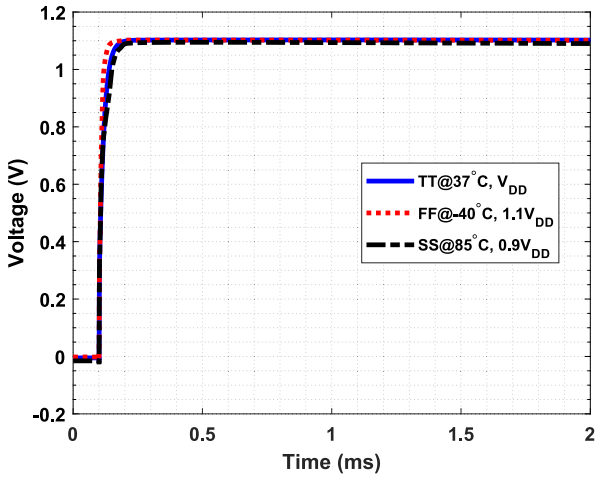


Fig. 19. Step response of the proposed low-noise amplifier.

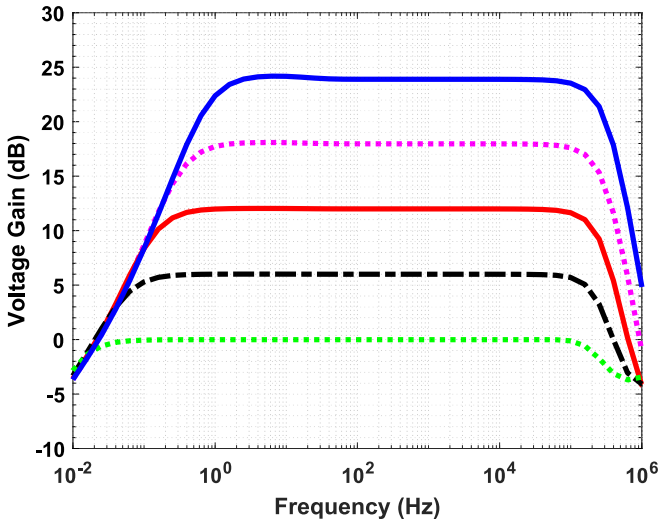


Fig. 20. The variable gain amplifier frequency response in different gain states.

Table 2
Performance summary of the simulated LNA under different PVT conditions.

Parameter	TT @ 37 °C, V_{DD}	FF @ −40 °C, $1.1V_{DD}$	SS @ 85 °C, $0.9V_{DD}$
Mid-Band Gain (dB)	23.93	23.92	23.92
Bandwidth (Hz)	0.24–10.55 k	0.13–13.04 k	0.37–8.87 k
Total Current (μA)	1.90	1.82	1.99
Input Equivalent Noise (μV_{rms})	LFP: 1.40 AP: 3.46	LFP: 0.87 AP: 2.47	LFP: 2.26 AP: 4.18
NEF	LFP: 5.09 AP: 1.80	LFP: 4.12 AP: 1.67	LFP: 7.28 AP: 1.92
PEF	LFP: 46.63 AP: 5.81	LFP: 33.94 AP: 5.58	LFP: 84.83 AP: 5.92
THD (dB)	−71.01	−78.78	−75.91
Dynamic Range (dB)	LFP: 92.12 AP: 84.27	LFP: 96.26 AP: 87.20	LFP: 87.97 AP: 82.63

cascode current mirrors, which enables large output swing, ensuring stable performance across various conditions.

Fig. 7 shows the second stage of the suggested LNA and its CMFB circuit. For this stage, a current-mirror amplifier without cascode transistors is selected to achieve the required large output swing. Since the noise from this stage is attenuated by the preceding stage's gain, source degeneration is unnecessary, though a class-AB output stage is used for power efficiency. Unlike the first stage, this CMFB circuit needs additional gain to increase the CMFB loop gain and regulate the common-mode voltage at the output nodes, due to the absence of cascode transistors. A constant current circuit is also employed for biasing

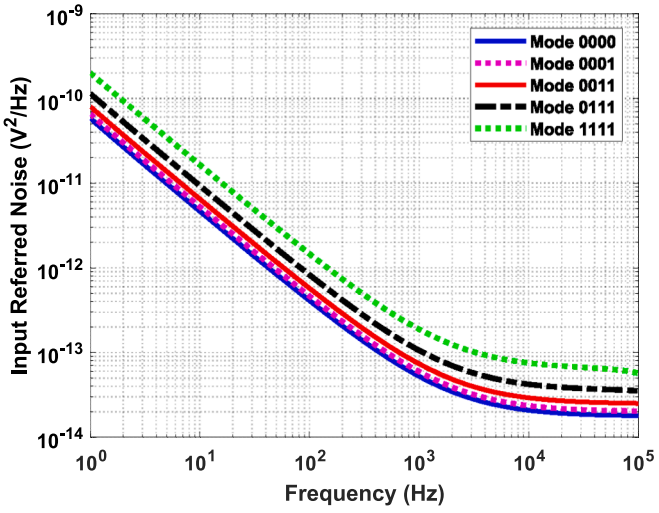


Fig. 21. Input-referred noise PSD of the variable gain amplifier.

Table 3
Comparison of the suggested low-noise amplifier performance with some recent works.

Ref.	JSSC'17 [3]	JSSC'17 [29]	AICSP'18 [33]	SSCL'19 [30]	JSSC'19 [36]	AICSP'19 [35]	AICSP'20 [31]	CSSP'22 [27]	This Work
Supply Voltage (V)	1.2	1.2	1.8	1.2	1.8	0.6	1.8	1.8	1.8
Process	40 nm	40 nm	180 nm	180 nm	180 nm	180 nm	180 nm	180 nm	180 nm
Power (μW)	2	2.8	4.07	2.6	3.24	0.72	1.53	3.64	3.42
Bandwidth (Hz)	0.2–5 k	0.12–5 k	0.3–4.4 k	0.5–5 k	0.35–5.4 k	0.12–5 k	5.69–5.45 k	0.1–5.1 k	0.24–10.55 k
Mid-band gain (dB)	26	25.7	39.75	41–59	40	39.2	40.02	26.04	23.93
Z_{in} (Ω)	300 M @DC	1.6 G @DC	N/A	3 G @DC	440 M	N/A	N/A	1.8 G @10 Hz	331 M @50 Hz
Input Equivalent Noise (μV_{rms})	AP: 7 LFP: 2	AP: 5.3 LFP: 1.8	3.19	AP: 3.2 LFP: 2.0	AP: 2.14 LFP: 0.65	4.98	3.27	AP: 2.86 LFP: 0.63	AP: 3.46 LFP: 1.40
Noise Efficiency Factor	AP: 4.9 LFP: 7	AP: 4.4 LFP: 7.4	2.78	AP: 3.2 LFP: 9.9	AP: 1.56 LFP: 2.37	2.13	1.58	AP: 2.3 LFP: 2.5	AP: 1.80 LFP: 5.09
Power Efficiency Factor	AP: 28.8 LFP: 58.8	AP: 23.2 LFP: 65.7	13.9	N/A	AP: 4.38 LFP: 11.1	2.71	4.5	AP: 9.52 LFP: 11.3	AP: 5.81 LFP: 46.6
THD	−74 dB @40 mV_{pp},1 kHz, input	−76 dB @80 mV_{pp},1 kHz, input	−40 dB @14.9 mV_{pp}, input	−35.6 dB @1 mV_{pp},1 kHz, input	−61 dB @5 mV_{pp}, 1 kHz input	−75 dB @1 mV_{pp}, 1 kHz, input	−40 dB @1.2 V_{pp}, output	−71.9 dB @40 mV_{pp}, 1 kHz, input	−71.01 dB @160 mV_{pp}, 1.03 kHz, input
Meas./Sim.	Meas.	Meas.	Meas.	Meas.	Meas.	Sim.	Sim.	Sim.	Sim.

the second stage amplifier.

2.2.1. Small-signal transconductance and DC gain

To calculate the amplifier gain, determining the output resistance and transconductance of each stage is required. The small-signal transconductance of the first stage, G_{m1}, is given by:

$$G_{m1} = g_{m2}\left(\frac{1}{g_{m4}} + R_2\right)\left(\frac{g_{m8}}{1+g_{m8}R_4} + \frac{g_{m14}}{1+g_{m14}R_6}\right) \tag{8}$$

Assuming the following conditions (which are necessary to reduce the circuit noise), the simplified relationship for G_{m1} is obtained as

$$g_{m4}R_2 = g_{m8}R_4 >> 1, \quad g_{m14}R_6 >> 1 \tag{9}$$

$$(R_2/R_6) = p\,, \quad (R_2/R_4) = k \;\Rightarrow\; G_{m1} \approx g_{m2}(k+p) \tag{10}$$

The second stage transconductance and the first and second stage output resistances are also calculated as follows:

$$G_{m2} = \frac{g_{m16}}{g_{m18}}\left(g_{m20} + g_{m22}\right) \tag{11}$$

$$R_{out,1} \approx g_{m10}g_{m8}r_{ds10}r_{ds8}R_4 \| g_{m12}g_{m14}r_{ds12}r_{ds14}R_6 \tag{12}$$

$$R_{out,2} = r_{ds20} \| r_{ds22} \tag{13}$$

And finally, the DC open-loop gain of the proposed OTA is calculated using the following relation:

$$A_{dc} = G_{m1}G_{m2}R_{out,1}R_{out,2} \tag{14}$$

2.2.2. Noise performance

To analyze the noise of the amplifier, several key points must be considered. First, since flicker noise analysis offers limited value for design optimization, only thermal noise has been analyzed in this work. Second, the noise from transistors with degenerated sources can be neglected. Additionally, considering that the second stage noise is referred to the input with a large gain, its noise contribution can also be disregarded. Furthermore, the noise from cascode and tail transistors can be ignored as well [25]. With these assumptions, the output thermal noise current is given by

$$\begin{aligned}
\overline{I_{n,th,out}^2} &= 2\overline{I_{n,th,M2}^2} \times \left(\frac{1}{g_{m4}} + R_2\right)^2 \left(\frac{g_{m8}}{1+g_{m8}R_4} + \frac{g_{m14}}{1+g_{m14}R_6}\right)^2 \\
&+ 2\overline{I_{n,th,M4}^2}\left(\frac{1}{1+g_{m4}R_2}\right)^2 \left(\frac{1}{g_{m4}} + R_2\right)^2 \left(\frac{g_{m8}}{1+g_{m8}R_4} + \frac{g_{m14}}{1+g_{m14}R_6}\right)^2 \\
&+ 2\overline{I_{n,th,M8}^2} \times \left(\frac{1}{1+g_{m8}R_4}\right)^2 + 2\overline{I_{n,th,M14}^2}\left(\frac{1}{1+g_{m14}R_6}\right)^2 \\
&+ 2\overline{I_{n,R2}^2}\left(\frac{g_{m4}R_2}{1+g_{m8}R_4}\right)^2 \left(\frac{1}{g_{m4}} + R_2\right)^2 \left(\frac{g_{m8}}{1+g_{m8}R_4} + \frac{g_{m14}}{1+g_{m14}R_6}\right)^2 \\
&+ 2\overline{I_{n,R4}^2}\left(\frac{g_{m8}R_4}{1+g_{m8}R_4}\right)^2 + 2\overline{I_{n,R6}^2}\left(\frac{g_{m14}R_6}{1+g_{m14}R_6}\right)^2
\end{aligned} \tag{15}$$

where $I_{n,th,Mi}^2$, $I_{n,Ri}^2$ are the thermal noise of the corresponding transistors and resistors. By assuming $B = g_{m4}R_2 = g_{m8}R_4 \gg 1$, $g_{m14}R_6 \gg 1$, the simplified input-referred thermal noise is given by:

$$\overline{V_{n,th,in}^2} = 4k_bT\frac{\zeta^2 V_T}{I_{D2}}\left(\left(1 + \left(\frac{1}{B}\right)^2 + \left(\frac{1}{B}\right)^2\frac{1}{2k}\right) + \frac{4V_T}{R_2 I_{D2}}\left(0.5 + \frac{1}{4k}\right)\right) \tag{16}$$

where k_b represents Boltzmann's constant, T denotes the absolute temperature, and V_T stands for the thermal voltage. To fairly compare low-noise amplifiers, two indices have been introduced: the Noise Efficiency Factor (NEF) and the Power Efficiency Factor (PEF). Their definitions, as

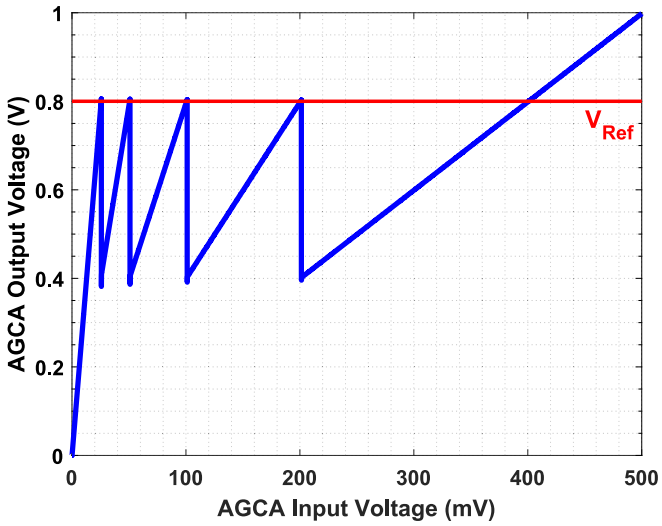


Fig. 22. Transfer characteristic curve of the automatic gain control amplifier.

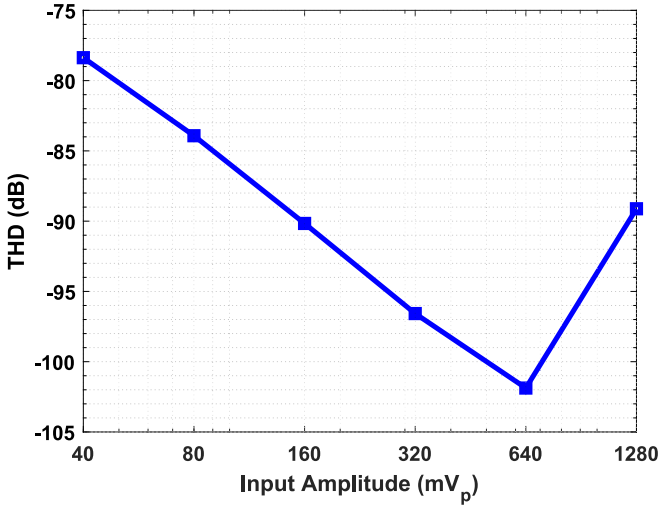


Fig. 23. THD of variable gain amplifier versus the input amplitude.

Table 4
Frequency performance of the simulated VGA under typical condition.

Parameter					
	0000	0001	0011	0111	1111
V_{DD} (V)	1.8				
Temperature (°C)	37				
Total Current (μA)	1.034				
Mid-Band Gain (dB)	23.89	17.97	11.99	6.00	−0.01
Bandwidth (Hz)	0.7–271.9 k	0.3–266.0 k	0.12–260.4 k	0.04–262.6 k	0.01–387.0 k
Input-EquivalentNoise (μV_{rms})	LFP: 15.8 AP: 17.6	LFP: 16.8 AP: 18.7	LFP: 18.7 AP: 20.8	LFP: 22.4 AP: 25.0	LFP: 29.8 AP: 33.3

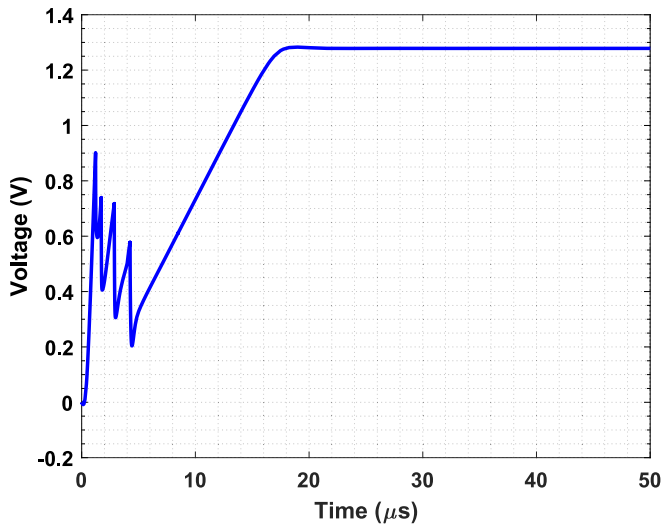


Fig. 24. Step response of the automatic gain control amplifier.

provided in [41] and [42], are given by the following relations:

$$NEF = V_{ni,tot,rms}\sqrt{\frac{2I_{tot}}{\pi \times V_T \times 4k_bT \times BW}} \tag{17}$$

$$PEF = NEF^2 \times V_{DD} \tag{18}$$

By rewriting the NEF relation for the first stage of the low-noise amplifier, the relation becomes:

$$NEF = \sqrt{4\zeta^2(k+1)\left(\left(1+\left(\frac{1}{B}\right)^2\left(1+\frac{1}{2k}\right)\right)+\frac{4V_T}{R_2I_{D2}}\left(0.5+\frac{1}{4k}\right)\right)\frac{1}{\pi}} \tag{19}$$

Considering $\zeta = 1.5$, B = 6, $V_T = 27$ mV, and a voltage drop across the resistor of 200 mV, the NEF versus k plot is shown in Fig. 8. According to this plot, the optimal value of k is about 0.35 while a value of 0.4 is chosen in this work.

2.3. Automatic gain control amplifier

This section of the circuit is responsible for reducing the gain in the presence of artifacts to prevent the circuit from saturating. Fig. 9 shows the proposed automatic gain control amplifier, while the inner schematic of the OTA (G_{mv}) is illustrated in Fig. 10. This block is designed to deliver a moderate gain with high accuracy and a large output swing. As seen in Fig. 10, a two-stage amplifier is required to achieve these requirements. A notable issue in this structure is that reducing the gain increases the bandwidth. Furthermore, the load capacitance of the amplifier also increases, which means the second pole decreases and the risk of instability arises. Therefore, in this structure, compensation must be adjusted simultaneously with the voltage gain. One way to shift the second pole is by altering the transconductance via changes in the amplifier's bias current, as described in [40]. However, in this paper, the compensation is adjusted by varying the Miller capacitance, as shown in Fig. 10, which helps maintain stability.

Table 5
Time-domain simulation results of automatic gain control amplifier.

Parameter	TT @ 37 °C, V_{DD}	FF @ −40 °C, $1.1V_{DD}$	SS @ 85 °C, $0.9V_{DD}$
Total Current (μA)	1.44	1.81	1.33
Max. THD (dB)	−78.37	−76.00	−77.41

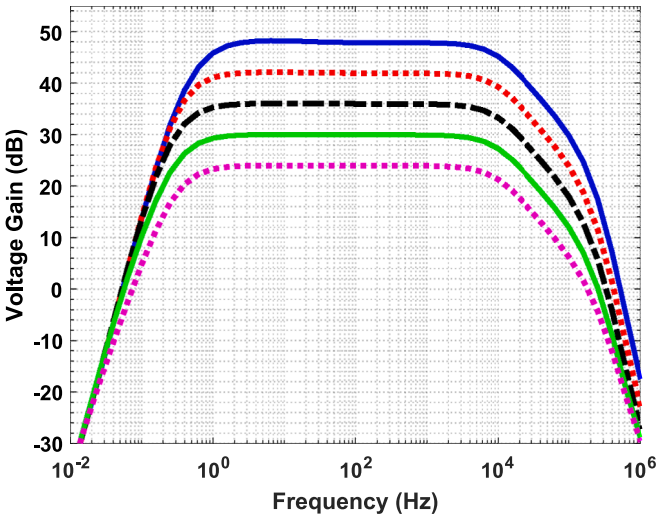


Fig. 25. The analog front-end frequency response.

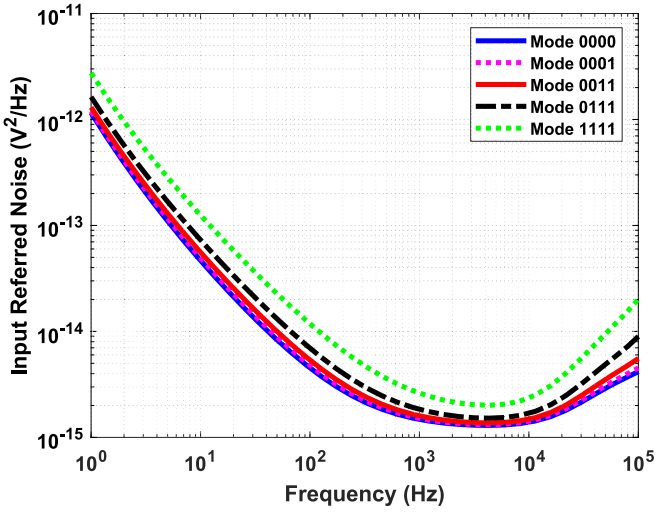


Fig. 26. Input-referred noise PSD of the analog front-end.

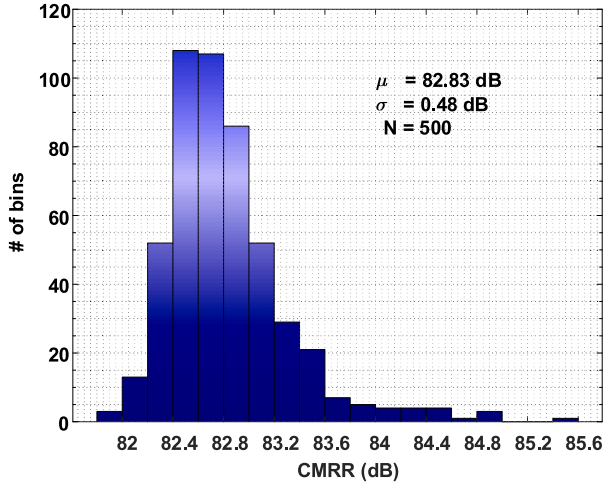


Fig. 27. Statistical distribution of CMRR.

The first stage of the OTA (G_{mv1}) is similar to the design in Fig. 6, except that the degeneration resistors are removed from the main circuits, CMFB amplifier, and biasing circuit, as noise performance is less

Table 6
Frequency performance simulation results of the analog front-end under typical condition.

Parameter	Mode				
	0000	0001	0011	0111	1111
V_{DD} (V)	1.8				
Temperature (°C)	37				
Mid-Band Gain (dB)	47.79	41.86	35.89	29.89	23.89
Bandwidth (Hz)	0.86–10.15 k	0.49–10.15 k	0.48–10.16 k	0.46–10.17 k	0.46–10.17 k
Input-Equivalent Noise (μV_{rms})	LFP: 1.73	LFP: 1.78	LFP: 1.88	LFP: 2.13	LFP: 2.78
	AP: 3.68	AP: 3.71	AP: 3.80	AP: 4.05	AP: 4.76

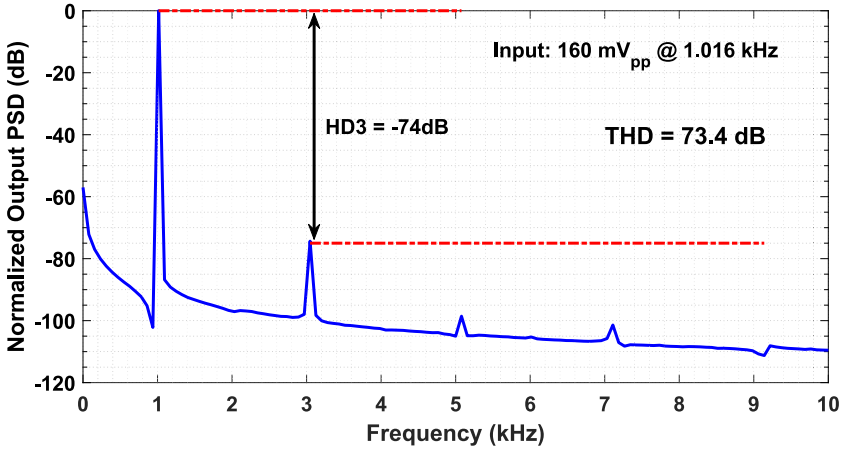


Fig. 28. Harmonic distortion of the suggested analog front-end.

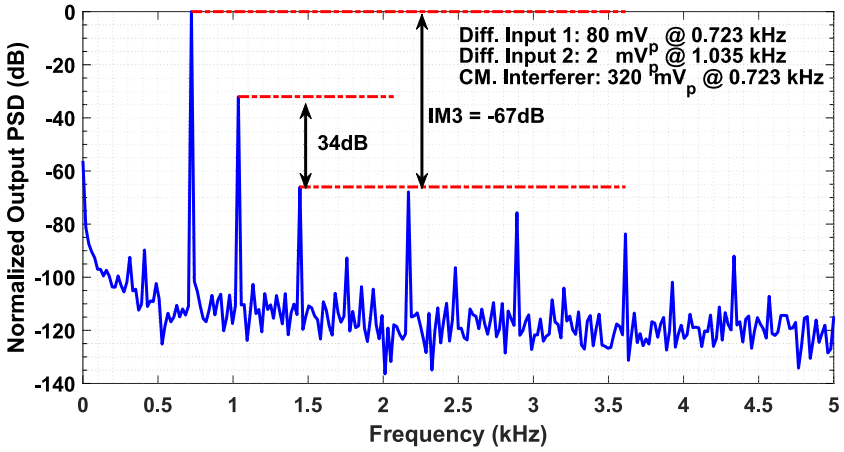


Fig. 29. Output spectrum of the suggested analog front-end in two-tone test.

critical than in the LNA's first stage. However, the second stage structure of the OTA (G_{mv2}) is identical to the design shown in Fig. 7.

An important part of this amplifier is the automatic gain control circuit. This structure must monitor the amplifier's output signal and adjust the gain if the voltage level exceeds a certain threshold. Therefore, a comparator is needed. Dynamic comparators consume less power, but because they perform the comparison operation in synchronization with the input clock, they have higher latency. Therefore, it is better to use static comparators for this application. Fig. 11 and Fig. 12 show the structure of the gain control circuit and the comparator circuit with differential voltage inputs.

The gain control circuit operates as follows. After a reset pulse, the circuit is in the state 0000 (referring to the signals $\varphi_4\varphi_3\varphi_2\varphi_1$). This means that after the reset, only capacitor C_{fv} is in the feedback loop, and its gain is at the maximum level. When $V_{out,VGA}$ exceeds the voltage V_{ref}, the output of the comparators goes to 1. This pulse is applied to the circuit in Fig. 11, causing the circuit state to change from 0000 to 0001. The capacitor C_{fv1} is introduced into the feedback path, halving the gain and bringing the output below V_{ref}. The next time $V_{out,VGA}$ exceeds V_{ref}, the same events occur, and the circuit state changes from 0001 to 0011. These events continue in this manner until the circuit reaches the state 1111. Beyond this state, the comparator outputs no longer change the circuit state. At this point, a reset signal must be present to return the circuit to the high gain state after the artifact has passed, allowing neural signals to be recorded with high accuracy.

It is important to note that the input-referred noise of this block and the voltage buffer is attenuated by the square of the voltage gain of the LNA. As a result, their impact on the overall noise performance of the

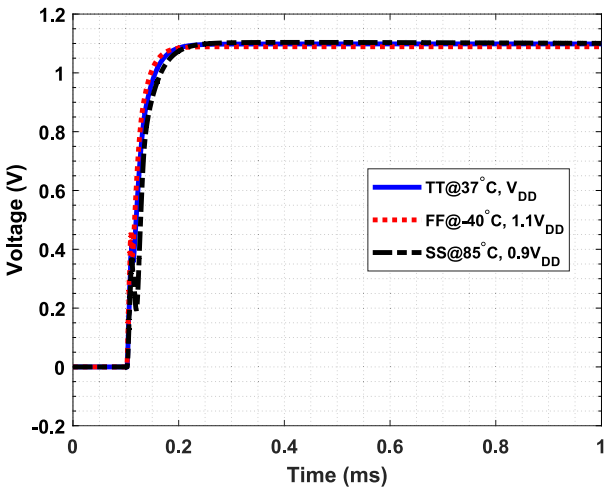


Fig. 30. Step response of the suggested analog front-end.

Table 7
Time-domain simulation results of analog front-end.

Parameter	TT @ 37 °C, V_{DD}	FF @ −40 °C, $1.1V_{DD}$	SS @ 85 °C, $0.9V_{DD}$
Total Current (μA)	3.88	4.24	3.82
Max. THD (dB)	−73.44	−75.33	−72.75

analog front-end is minimal. Therefore, for the sake of simplicity, their noise analysis has been omitted.

2.4. Voltage buffer

At the end of the analog section of the circuit, there is a voltage buffer responsible for driving the input capacitors of the ADC. A notable point is that these capacitors are connected to the buffer output only during sampling and are disconnected at other times. Consequently, during non-sampling periods, the output pole of the buffer shifts to upper frequencies. If this pole is dominant, there is a risk of instability, but if it is the second pole, it enhances circuit stability. Therefore, a two-stage buffer design is preferable. Additionally, since this stage does not provide a gain greater than one, cascode transistors at the output are unnecessary. So, in the OTA, the first and second stages are simple current mirror amplifiers with class AB output branches.

2.5. Analog-to-digital converter (ADC)

Finally, the amplified signal from the analog front-end is converted to digital data by an ADC. For medium accuracy, low-speed, and low-power applications, SAR ADCs are an appropriate choice. In this work, the switching method introduced in [43] is used. The advantage of this switching method is that the ADC's output code is almost independent of the mid-level reference voltage, except for the LSB (least significant bit). Additionally, the input common-mode voltage of the comparator remains nearly constant. These improvements are achieved with low-complexity SAR logic. The comparator uses a strong-arm latch structure as depicted in Fig. 13.

3. Circuit level simulation results

In this section, the simulation results of the proposed circuit, implemented in Cadence software using 180 nm TSMC CMOS technology, with a supply voltage of 1.8 V, and at a temperature of 37 °C, are presented. These results include simulations of various parts of the front-end individually, the complete analog front-end, and the overall system simulation. Additionally, the circuit's performance will be examined under PVT variations. Although the environment around the implants is close to body temperature, to evaluate the circuit's performance under extreme conditions, simulations were conducted across a wide temperature range, from −40 to 85 degrees Celsius.

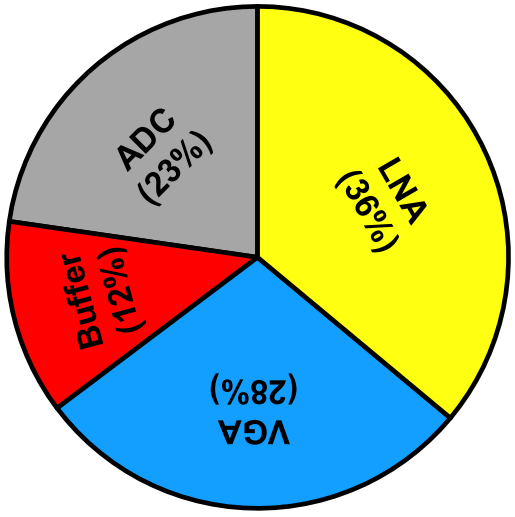


Fig. 32. Distribution of power consumption between different blocks.

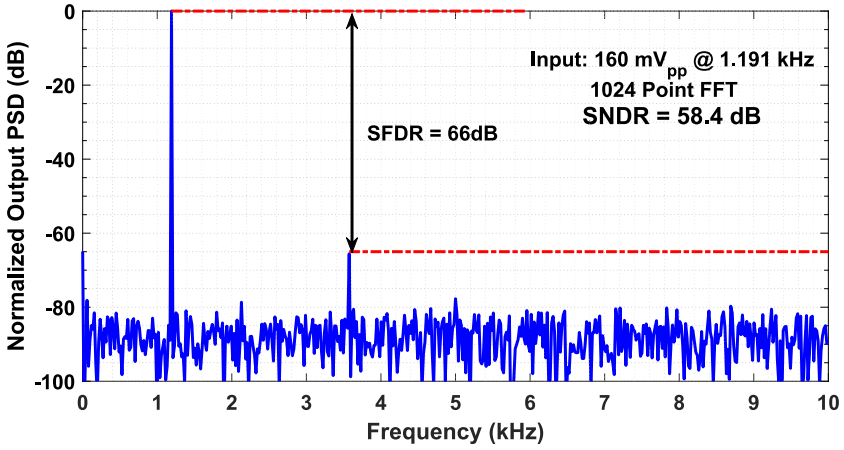


Fig. 31. Normalized output spectrum of the front-end.

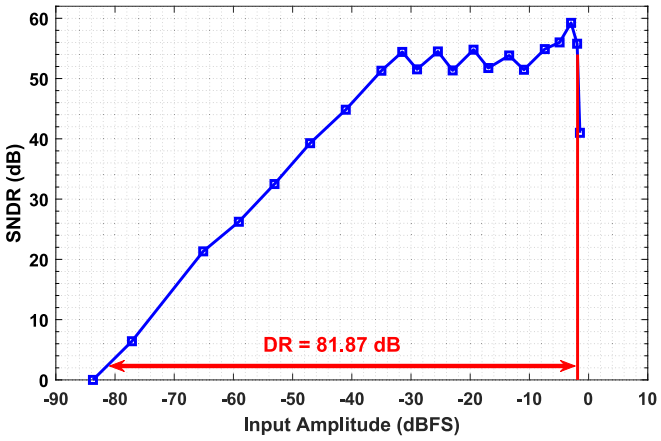


Fig. 33. Simulated SNDR with varying the input amplitude.

3.1. The proposed low-noise amplifier

In the simulations related to the low-noise amplifier, an electrical model of the electrodes, as depicted in Fig. 2, is used at the input. Additionally, the aspect ratio (W/L) of transistors, and the sizes of resistors and capacitors in Figs. 5–7 are mentioned in Table 1. The voltage gain is set to 16 (24 dB) to prevent saturation when artifacts are present. Additional details on the amplifier's other characteristics are discussed in the introduction.

Firstly, the frequency transfer function of the circuit across different technology corners, considering supply voltage and temperature variations, is depicted in Fig. 14. The amplifier's mid-band gain is 23.93 dB, with a bandwidth ranging from 0.24 Hz to 10.55 kHz. Fig. 15 presents the input-referred noise power spectral density (PSD) across different corners. The integrated input-referred noise amounts to 1.40 μV_{rms} in the LFP band and 3.46 μV_{rms} in the AP band. A notable observation in Fig. 15 is that the input-referred noise PSD rises at high frequencies. This occurs because some noise sources still have relatively high gain paths, while the signal gain has dropped, resulting in increased input-referred noise at out-of-band frequencies.

To assess the noise impact of the T-network within the DC feedback loop, simulations were performed on the LNA after replacing the T-network with a conventional DC feedback structure. In these simulations, the low cut-off frequency and the input-referred noise of the LNA were 0.66 Hz and 3.39 μV_{rms}, respectively. This demonstrates that the T-network effectively reduces the low cutoff frequency while introducing only a negligible increase in input-referred noise.

To evaluate the low-noise amplifier's linearity, a sinusoidal signal with an 80 mV_p amplitude and a frequency of 1.03515625 kHz was applied to the input. A 1024-point fast Fourier transform (FFT) was then performed on the output. The normalized output PSD is shown in Fig. 16. The simulated total harmonic distortion (THD) of the amplifier was −71.01 dB, as illustrated in Fig. 16. Additionally, to evaluate the proposed amplifier's operation in the presence of artifacts, a simulation with two inputs was conducted. A signal with a frequency of 0.72265625 kHz and differential amplitude of 80 mV_p, along with a common-mode amplitude of 320 mV_p, and a differential signal of 2 mV_p at 1.03515625 kHz, was applied to the circuit. The result of this simulation is shown in Fig. 17. As depicted, the low-noise amplifier tolerates these artifact signals well, with minimal intermodulation distortion.

The amplifier input impedance is also an important aspect. The frequency simulation results of the input impedance under various conditions are shown in Fig. 18(a). This behavior is predictable due to the capacitive nature of its input impedance. Fig. 18(b) shows the ratio of the input impedance magnitude of the circuit to the impedance of the electrode. Within the amplifier's bandwidth, this ratio is always above 150, indicating that the proposed low-noise amplifier performs well in terms of input impedance.

To assess the circuit's stability, the step response was evaluated when a 70 mV_p input was applied. The output waveform under different corners is shown in Fig. 19. As seen in the figure, the circuit demonstrates adequate stability.

Table 2 summarizes the results of the proposed low-noise amplifier simulation under various PVT conditions. Table 3 compares the performance of the low-noise amplifier with previous works. According to Table 3, the proposed LNA, while maintaining low noise in the LFP and AP signal bands and acceptable linearity, consumes an appropriate amount of power, making it suitable for use as the first stage in analog circuits for neural signal recording. Moreover, due to the absence of chopper techniques, there is no concern regarding the input impedance of the amplifier.

3.2. The proposed gain control amplifier

First, the amplifier is simulated without the gain control circuit to obtain the frequency characteristics of the circuit, such as the frequency response and noise performance. The frequency transfer function of the amplifier in different gain states is shown in Fig. 20. In each state change, the gain is halved, equivalent to an approximate reduction of 6

Table 8
Comparison of the proposed front-end performance with some of recent works.

Ref.	TBCAS'16 [44]	TBCAS'17 [24]	JSSC'18 [8]	JSSC,19 [14]	JSSC,21 [45]	JSSC,22 [22]	TBCAS'23 [15]	JSSC'23 [13]	This Work
Topology	AFE + ADC	AFE + ADC	CCIA + CT-DSM	CT-DSM	LNA + VGA + SAR ADC	LNA + VGA+CT-Zoom-DSM	AFE −Embedded NSSAR	NSSAR nested DSM	LNA + VGA + SAR ADC
Supply Voltage (V)	1.8,0.9	1.2	1.2	1.8	1,3	1.2,0.8	1.2	1.3,0.8	1.8
Process	180 nm	130 nm	40 nm	180 nm	180 nm	180 nm	180 nm	65 nm	180 nm
Power (μW)	9.5	2.43	7.3	23	4.3	9.8/13.6	4.3	5.2	9.0
Bandwidth (Hz)	0.3–7 k	192–7.4 k	0.1–5 k	1–5 k	200–9 k	1–5 k	1–5 k	1–500	0.24–10 k
Peak SNDR (dB)	56	47.5	78	78	53.5	70.1	71.5	94.5	58.40
Dynamic Range (dB)	59	65.5*	81	90	N.A.	99.5	72	95.8	81.9
FOM_s (dB)	147.7	160.2	169.4	173.4	N.A.	185.2	162.7	175.6	172.4
Peak Input (mV_{pp})	10	1200	200	208	700	76	150	600	180
Input Impedance (Ω)	∞ @ DC	5.4 M @ 1 kHz	1.52 G @ DC	1.06 G @ 250 Hz	∞ @ DC	∞ @ DC	133 M @ 300	208 M @ DC	331 M @ 50 Hz
Meas./Sim.	Meas.	Meas.	Meas.	Meas.	Meas.	Meas.	Meas.	Meas.	Sim.

* Estimation

dB. The next simulation pertains to the input noise of the amplifier. Although the noise of this stage does not significantly affect the total noise, it should not be excessively large. The input-equivalent noise power of this amplifier is shown in Fig. 21. As expected, and according to relation (3), the input-equivalent noise increases as the feedback capacitor becomes larger. Table 4 shows the performance of the VGA without the gain control circuit in typical condition.

To evaluate the other characteristics of the variable gain amplifier circuit, time-domain simulations need to be performed in the presence of the gain control circuit. The first step is to assess the performance of the control circuit. For this purpose, a ramp signal is applied to the input of the automatic gain control amplifier, and its output is observed in Fig. 22. In the circuit, a reference voltage of 800 mV is defined for changing the gain. As shown, shortly after the differential output of the circuit crosses the threshold voltage, the control circuit reduces the gain. However, once the circuit reaches unity gain, further crossing of the output voltage over the reference voltage does not change the gain.

Next, to evaluate the linearity of the amplifier, several sinusoidal signals are applied to the circuit. Fig. 23 shows the THD of the output signals versus the input amplitude. According to the figure, for an input amplitude of 1.28 V, the output signal maintains acceptable THD. Finally, to assess the stability of the circuit, a pulse with a rise time of 5 μs is applied to the input. This simulation, shown in Fig. 24, demonstrates that the gain control circuit operates effectively at high speeds and that the amplifier circuit maintains good stability. The sawtooth behavior at the beginning of Fig. 24 is due to variations in the amplifier's gain, resulting in a decrease in output voltage. Given the presence of five different states, four sudden changes in the output voltage were predictable. The specifications of the automatic gain control amplifier are summarized in Table 5.

3.3. The analog front-end

Similar to the simulations of the AGCA, the frequency simulation of the analog front-end is conducted without considering the gain control circuit. Fig. 25 illustrates the frequency response of the analog circuit with different gains. Additionally, the results of the noise simulation of the analog circuit are plotted in Fig. 26. To evaluate the Common-Mode Rejection Ratio (CMRR), a Monte Carlo simulation with 500 iterations, considering process variations and device mismatches, has been performed. The average CMRR of the proposed analog circuit at 50 Hz is 82.83 dB, and the histogram of this simulation is shown in Fig. 27. A summary of the frequency specification of the analog circuit is provided in Table 6.

Furthermore, by applying a sinusoidal input signal at a frequency of 1.26953125 kHz and observing the output spectrum, the THD of the analog front-end is calculated (Fig. 28). In addition, a two-tone test was conducted to assess intermodulation. In this test, a differential signal with a frequency of 0.72265625 kHz and an amplitude of 80 mV_p, along with a common-mode amplitude of 320 mV_p, and a differential signal with an amplitude of 2 mV_p at a frequency of 1.03515625 kHz, were applied to the circuit. The result of this simulation is shown in Fig. 29. As can be seen, the intermodulation distortion is minimal and does not significantly affect the circuit's linearity. To assess the stability of the circuit, a pulse was applied to its input and the step response is shown in Fig. 30. The summary of the analog front-end's specifications, extracted from time-domain simulations, is provided in Table 7.

3.4. The analog front-end and ADC

First, the output spectrum for an input signal with an amplitude of 80 mV_p at a frequency of 1.03515625 kHz is shown in Fig. 31. According to the figure, the Spurious-Free Dynamic Range (SFDR) is 65.57 dB. This indicates that the power of harmonics generated by the analog circuit is much lower than the quantization noise of the ADC. The maximum SNDR and ENOB of this interface circuit are 58.40 dB and 9.41 bits, respectively. Under these conditions (TT corner, body temperature, and 1.8 V supply voltage), the current consumption of the interface circuit is 5.01 μA, leading to a power consumption of 9.018 μW, which is acceptable given the circuit's bandwidth.

The power consumption percentage of each section of the circuit is shown in Fig. 32. As expected, the low-noise amplifier (LNA) consumes the highest share of power. Additionally, to calculate the dynamic range, the SNDR of the digitized output signal is plotted against the input signal power, as shown in Fig. 33. The dynamic range of the interface circuit is 81.87 dB. Table 8 provides a comparison between the proposed interface circuit and previous works in the field of closed-loop neural signal recording. For a fair comparison, the Schreier's figure of merit (FOM) has been used, which is defined by the following equation:

$$FOM_s(dB) = DR(dB) + 10\log\left(\frac{BW(Hz)}{Power(W)}\right) \tag{20}$$

This FOM incorporates dynamic range, power consumption, and bandwidth, three critical parameters for a closed-loop neural recording system, which are often in trade-off and together reflect the efficiency of the proposed architecture. However, we acknowledge that the Schreier's FOM is not the only important metric. Other specifications, such as operating under 10 μW power, maximum tolerable input signal, and a sufficiently wideband frequency response, are also essential for a practical closed-loop analog front-end design. According to this table, the proposed analog front-end circuit strikes a fine balance between power efficiency, signal integrity, and bandwidth, demonstrating its suitability for advanced closed-loop neural signal recording systems. With its low power consumption of 9.0 μW, the design stands out in the context of modern power-sensitive applications, such as portable or implantable devices for neural interfacing.

However, every work has room for improvement, and this study is no exception. In this design, a suitable, but not optimal, SAR ADC with a simple switching scheme was used. Therefore, adopting a more advanced SAR architecture or even a delta-sigma ADC could enhance overall efficiency. Moreover, this paper presents a single-channel circuit, but in a multi-channel AFE, techniques such as time-division multiplexing could reduce the effective power consumption per channel. Another possible improvement lies in designing a more efficient gain control circuit that adjusts the voltage gain after the stimulation artifacts disappears.

4. Conclusion

This work proposes an interface circuit for closed-loop neural recording systems. The main challenge in designing this circuit for such applications is the presence of large-amplitude artifacts, which can easily saturate the circuit. In this work, a gain control technique is employed to prevent amplifier saturation. Additionally, since the first stage plays a crucial role in the noise performance of the circuit, a low-noise amplifier using a current-mirror OTA is used at the input of the interface circuit. To reduce noise in this stage, source-degeneration technique is used instead of chopper technique, and to enhance power efficiency, a class-AB output stage is utilized. Moreover, by modifying the DC feedback structure, the low cut-off frequency of the circuit is lowered. The subsequent stages include a variable-gain amplifier and gain control circuit, which dynamically adjust the circuit's gain based on the input amplitude. To drive the ADC capacitors, a voltage buffer with adequate bandwidth is placed at the output of the VGA. Finally, an ADC with appropriate switching methods converts the amplified signal into digital data.

The LNA, with a power consumption of 3.42 μW and an input-referred noise of 1.40 and 3.46 μV_{rms} in the LFP and AP signal bands, respectively, and a THD of less than −70 dB for input amplitudes up to 80 mV_p, shows satisfactory performance. The VGA can effectively reduce the gain of the interface circuit at high speeds, preventing its

saturation. The entire interface circuit, with a power consumption of 9 μW and a dynamic range greater than 80 dB, and a maximum SNDR of 58.40 dB, can successfully convert neural signals from the analog to the digital domain with high quality.

CRediT authorship contribution statement

Mohammadamin Mohtashamnia: Writing – review & editing, Writing – original draft, Validation, Software, Resources, Methodology, Investigation, Formal analysis, Data curation, Conceptualization. **Mohammad Yavari:** Writing – review & editing, Visualization, Validation, Supervision, Project administration, Investigation, Funding acquisition, Conceptualization.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

No data was used for the research described in the article.

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