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A low-power low-noise neural recording amplifier with an improved recycling telescopic-cascode OTA

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ABSTRACT

In this paper, a fully-differential low-power low-noise neural recording amplifier with a novel recycling telescopic-cascode (RTC) operational transconductance amplifier (OTA) is presented. In the proposed RTC OTA, the current recycling and cross-coupled transistors with local positive feedback are utilized to significantly improve the OTA's parameters like small-signal DC gain and unity-gain bandwidth. The gain enhancement also improves the linearity in the closed-loop structure. Extensive analytical calculations and simulation results using TSMC 0.18-μm CMOS process are provided to examine the usefulness of the proposed OTA. The simulated neural recording amplifier achieves 3.55 μV_{rms} input-referred noise over 1 Hz-10 kHz bandwidth with 3.03 and 1.22 noise efficiency factor for local field potential (LFP) and action potential (AP) bands, respectively. The total harmonic distortion (THD) is −41.7 dB for a 1 mV_{pp}, 1 kHz sinusoidal input signal. The total power consumption is 1.70 μW from a single 1.8-V power supply.

1. Introduction

Recent advances in the internet of things (IoT) and the need for more neural monitoring of some patients with Parkinson's disease and fainting or changes in brain function caused by anxiety about this monitoring, have made the idea of using implantable bio-chips in the body which are for permanent monitoring, more noticeable for the professionals [1,2]. Favorite signals in neural recording are classified into two action potential (AP) and local field potential (LFP) categories. As shown in Fig. 1, the frequency range of LFP signals is from 1 Hz to 200 Hz with a maximum amplitude of 1 mV and the APs' frequency range is from 200 Hz to 10 kHz with a maximum amplitude of 100 μV [2,3]. The main challenges in designing implantable neural recording systems are small silicon area and low power consumption because they increase the battery life and prevent the loss of living tissues. Besides, low input-referred noise (IRN), high power supply rejection ratio (PSRR) and common-mode rejection ratio (CMRR), and considerable input impedance are also needed [4].

To reduce the power consumption, circuit noise, and area, several techniques have been utilized in previous works. In [5], the source degeneration technique has been applied to a double recycling folded-cascode amplifier to reduce the input-referred noise. But it also reduces the output swing and voltage gain. In [6–9], chopper amplifiers have been used with positive feedback in order to achieve noise requirements and also to compensate low input impedance of chopper amplifiers. However, these amplifiers require clock and extra circuits that increase the power consumption and complexity of the amplifier [10]. The open-loop instrumentation amplifier (IA) in [11] has small noise efficiency factor (NEF) and large CMRR and PSRR. But open-loop structures in comparison with closed-loop ones have more sensitivity to the process, voltage, and temperature (PVT) variations and degraded linearity. In [12] and [13], the proposed amplifier is single-ended resulting in low linearity and small CMRR and PSRR. In [14], the fully-differential amplifier consists of an IA and a programmable gain amplifier (PGA). Due to the asymmetry in the IA structure, the linearity of the amplifier is drastically reduced.

Recently, some methods have been suggested to improve the performance of the conventional folded-cascode amplifier. In [15], by splitting the input transistors and producing a new signal path, the current-source transistors in the conventional folded-cascode amplifier are also utilized in the signal amplification path. This improved amplifier, named the recycling folded-cascode amplifier, actually comprises two parallel conventional folded-cascode and current-mirror operational transconductance amplifiers (OTAs) and improves both small-signal and large-signal parameters of the OTA compared to the conventional folded-cascode amplifier. In [16], an improved fully-

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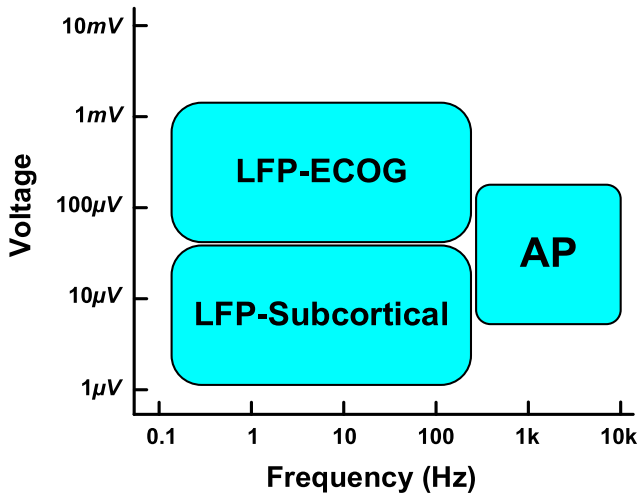

Fig. 1. Frequency range and amplitude of neural signals [2].

differential OTA with a class AB operation is presented which uses the recycling technique in both NMOS and PMOS current-source transistors in the traditional folded-cascode OTA. Indeed, by using these techniques, a three-path amplifier consisting of one folded-cascode and two current-mirror OTAs with a class AB operation is realized which significantly improves both large-signal and small-signal parameters in comparison with the conventional and recycling folded-cascode OTAs. The class AB operation is realized by utilizing a flipped-voltage follower (FVF) cell in input transistors.

In [17], a super class AB scheme of the recycling folded-cascode OTA is proposed by utilizing an adaptive biasing circuit for the input differential pair to provide the dynamic current boosting. Using the recycling technique and positive-feedback cross-coupled transistors, a single-stage three-path OTA is presented in [18] to substantially improve the dc frequency gain, unity-gain bandwidth, and slew rate for switched-capacitors circuits. The local positive feedback technique has been also utilized in a non-recycling folded-cascode OTA in [19] to improve the dc gain. In [20] by using the class-AB input stage which includes the cross-coupled FVFs and also using a non-linear current recycling output stage, the unity-gain bandwidth and the maximum output current have been improved. In [21], the thermal noise is reduced by using transconductance boosting and self-biasing without any extra power consumption. Also, for improved gain and transconductance, multi-stage amplifiers are used in [22].

In this paper, a low-noise amplifier (LNA) with capacitive feedback is presented for neural recording applications. An improved fully-differential recycling telescopic-cascode OTA is proposed to realize the neural recording amplifier. In comparison with the folded-cascode OTA, the telescopic-cascode amplifier achieves higher dc gain and unity-gain bandwidth and lower input-referred noise with lower power consumption. So, the current recycling technique and cross-coupled transistors with local positive feedback are utilized in the conventional telescopic-cascode OTA to significantly improve both large-signal and small-signal characteristics.

The remainder of the article is prepared as follows. In Section 2, the overall architecture of the neural recording amplifier and its important specifications are presented. The structure and analysis of the proposed recycling fully-differential telescopic-cascode OTA are presented in Section 3 along with a detailed comparison with the conventional telescopic-cascode OTA. The circuit level simulation results are presented in Section 4 and Section 5 concludes the paper.

2. Neural recording amplifier structure

The architecture of the neural recording amplifier employing

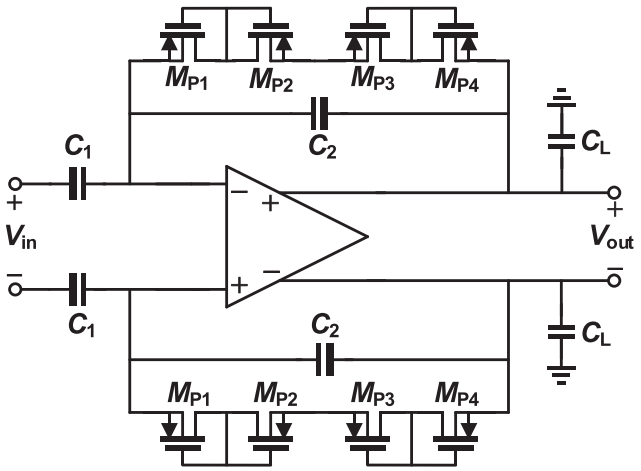

Fig. 2. Capacitive feedback neural recording amplifier.

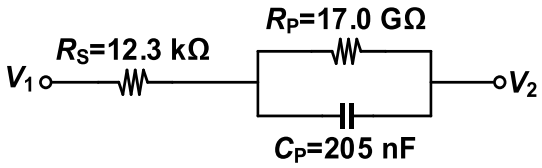

Fig. 3. Electrical model of electrodes [24].

capacitive feedback is illustrated in Fig. 2 [23]. Transistors M_{P1}-M_{P4} are utilized to realize a pseudo resistor named R_2 whose value is about several hundreds of GΩ [5]. In this section, the main specifications of the LNA are briefly reviewed such as the transfer function, input-referred noise, and input impedance.

2.1. Transfer function

The relationship between the output and input voltages in Fig. 2 is given by [23]:

$$\frac{V_{out}}{V_{in}}(s)=\frac{C_1}{C_2}\times\frac{1-s\left(\frac{C_2}{G_m}\right)}{\left(1+\frac{1}{sR_2C_2}\right)\left(1+s\frac{C_LC_1}{G_mC_2}\right)}=A_M\frac{1-\frac{s}{\omega_z}}{\left(1+\frac{\omega_{pL}}{s}\right)\left(1+\frac{s}{\omega_{pH}}\right)} \tag{1}$$

According to relation (1), the low cutoff frequency (f_L) is set by R_2 and C_2, and the mid-band gain is determined by C_1/C_2 ratio. Finally, the high cutoff frequency (f_H) is the ratio of OTA unity gain frequency and mid-band gain. Also, there is a right-half-plane zero (f_z), but by using the appropriate value of capacitors and OTA transconductance, this zero can be large enough to have little effect on the amplifier performance. For this purpose, the value of capacitors should be selected as [23]:

$$C_2 << \sqrt{C_1C_L} \tag{2}$$

2.2. Input impedance

By considering the Miller effect of capacitor C_2, the differential input impedance of the neural recording amplifier is obtained as:

$$\begin{aligned} Z_{input} &= 2\left(\frac{1}{j\omega C_1}+\frac{1}{j\omega(1-A_{dc})C_2}\middle\|\frac{1}{j\omega C_{in}}\right) \\ &\Rightarrow (1-A_{dc})C_2 >> C_{in}, C_1 \Rightarrow Z_{input}\approx\frac{2}{j\omega C_1} \end{aligned} \tag{3}$$

where C_{in} is the amplifier input parasitic capacitance. Relation (3) indicates that with high gain and small amplifier input parasitic capacitor, the input impedance at the mid-band frequencies is only dependent on

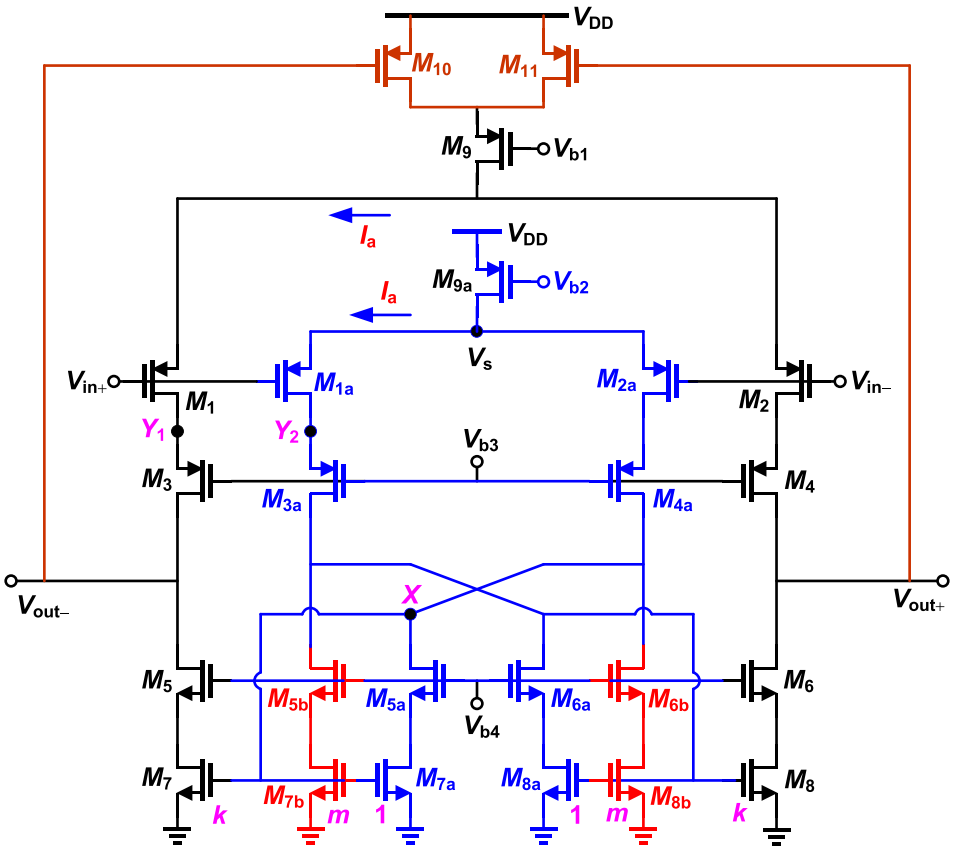

Fig. 4. Proposed single-stage recycling telescopic-cascode OTA.

C_1. For the proposed application that we need power efficiency, certain mid-band gain, and low cutoff frequency, the input impedance must be extremely greater than the electrode impedance. Fig. 3 illustrates the typical electrical model of the electrodes [24]. For example, in 10 kHz input signal frequency, the impedance of the electrode is about 12.4 kΩ. Thus, the amplifier input impedance must be >236 kΩ at 10 kHz so that the voltage drop across the electrode is less than 5% of the input signal. Therefore, we are to use an input capacitor with an amount lower than 70 pF. Also, it is necessary for the amplifier to have extremely high input impedance at DC in order to avoid damaging the living tissues. This is achieved by using the capacitive feedback amplifier.

2.3. Input-referred noise

In the neural recording amplifier shown in Fig. 2, the main noise sources are the input-referred noise of the OTA and the thermal noise of the pseudo resistors. So, the input-referred noise (IRN) of the neural amplifier shown in Fig. 2 is given by [10]:

$$\overline{V_{ni,Amp}^2} = \left(\frac{C_1 + C_2 + C_{in}}{C_1}\right)^2 \left(\overline{V_{ni,OTA}^2} + \overline{V_{nR2}^2}\right) \tag{4}$$

where $V_{ni,OTA}$ is the OTA's IRN and V_{nR2} is the noise of the pseudo resistors which can be negligible [23].

According to relation (4), the ratio of C_1 and C_2 capacitors has a large effect on LNA input-referred noise. Therefore, the LNA needs to have relatively large input capacitors. But this issue reduces the input impedance, although it results in large closed-loop gain. Another important point that should be considered is the amount of background noise raised by the electrodes which is about 10 μV_{rms} [2]. So, the total input-referred noise of the neural recording amplifier should be lower than this amount.

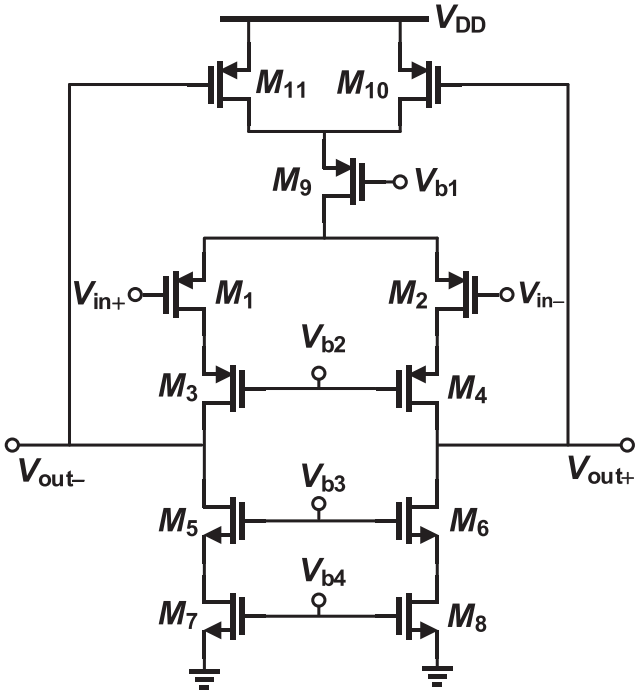

Fig. 5. Traditional telescopic-cascode OTA.

3. Proposed recycling telescopic-cascode OTA

In this section, the structure of the proposed recycling telescopic-cascode OTA is described. Then the analysis of OTA characteristics is

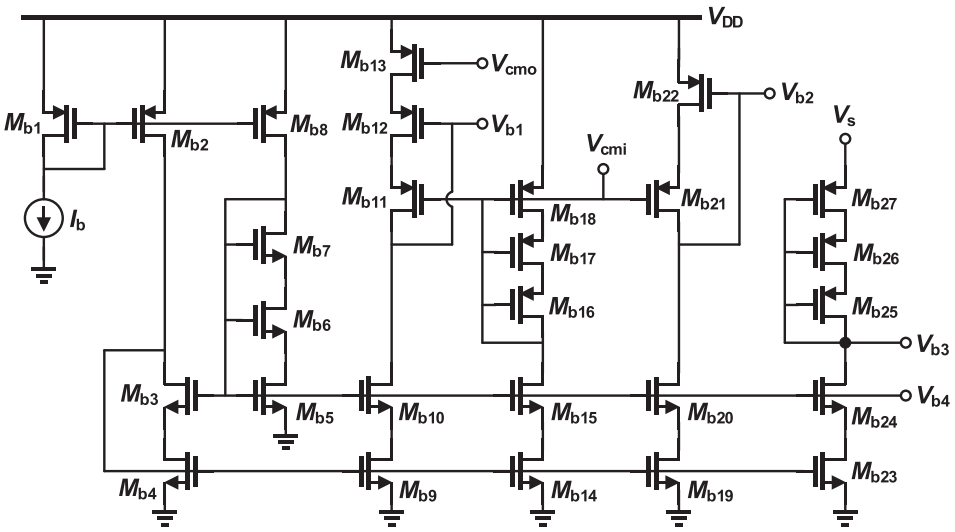

Fig. 6. Biasing circuit of the proposed recycling telescopic-cascode OTA.

presented. Finally, a careful comparison between the conventional telescopic-cascode OTA and the proposed one is provided.

3.1. Proposed OTA architecture

Fig. 4 depicts the structure of the proposed recycling telescopic-cascode OTA. The transistors M_1-M_9 are corresponding transistors in the traditional telescopic OTA which is also shown in Fig. 5 [25]. The input transistors are chosen PMOS rather than NMOS due to lower flicker noise [18], and they are divided into M_1, M_{1a}, M_2 and M_{2a} in order to realize the current recycling technique and also to reduce the bias current of output transistors, and hence, enhance the output resistance. Transistors M_7, M_{7a}, M_8 and M_{8a} are divided to make a two-path amplifier. M_{5a} and M_{6a} transistors are used to form the wide-swing cascode current mirrors to improve the matching in active current mirrors. Transistors M_{5b}, M_{6b}, M_{7b}, and M_{8b} are used in a cross-coupled structure instead of the current mirror scheme in order to build a local positive feedback circuit at the gates of M_7 and M_8 transistors [18]. Also, the current mirror ratios are denoted by k and m in Fig. 4.

The common-mode (CM) voltage of output nodes cannot be defined by using a single tail current source at the source of input transistors since in this case, the gain of the common-mode feedback (CMFB) loop will be almost zero owing to having two separate CMFB paths with similar gains but opposite sign. Therefore, two separate tail current sources are employed at the source of input transistors in order to define the CM voltage at the output nodes through the negative CMFB loop which is realized by the main telescopic amplifier. M_{10} and M_{11} similar transistors are used at the source of M_9 tail current source to implement the CMFB circuit. Transistors M_{10} and M_{11} are biased in deep triode region resulting in a resistance at the source of M_9 transistor which is equal to:

$$\begin{aligned} R_P &= R_{on10}||R_{on11} \\ &= \frac{1}{\mu_p C_{ox}(W/L)_{10,11}\left(2V_{DD} - V_{out+} - V_{out-} - 2\left|V_{TH10,11}\right|\right)} \end{aligned} \tag{5}$$

where μ_p is the mobility of holes, C_{ox} is the oxide capacitance per unit area, and $(W/L)_{10,11}$ and $|V_{TH10,11}|$ are the aspect ratio and threshold voltage of M_{10} and M_{11} transistors. The operation of the CMFB circuit is as follows. When the CM voltage of output nodes is increased, the equivalent on-resistance of M_{10} and M_{11} transistors is also increased resulting in more voltage drop across these transistors. Therefore, the bias current of M_9 tail current source is decreased. On the other hand, the bias current of M_5-M_8 transistors is defined by M_{9a} tail current source and the aspect ratio of current mirror transistors which is almost constant during the common-mode operation. Hence, the drain current of M_3 and M_4 transistors becomes less than that of M_5 and M_6 transistors. Therefore, the CM voltage of output nodes should be reduced due to the channel length modulation effect of MOS transistors in order to satisfy the current Kirchhoff's law at the output nodes. So, there is a negative CMFB loop to define the output CM voltages. A similar phenomenon is happened when the CM voltage of output nodes becomes less than the desired value of V_{cmo}. During the differential signal amplification, R_P is constant and the CM voltage at the output nodes is not changed.

The biasing voltages V_{b1}-V_{b4} and input CM voltage are provided by a constant current biasing circuit with an ideal current source (I_b) which is shown in Fig. 6 where V_{cmo} is the intended output CM voltage which is usually set to $V_{DD}/2$. Wide-swing cascode current mirrors are used to improve the matching between biasing and main transistors without the swing reduction at the output of the main OTA. To reduce the sensitivity of the output CM voltage to the device parameters and the value of V_{b1}, the drain current of transistor M_9 tracks the constant bias current of M_{b12} transistor and V_{cmo}. So, by neglecting the channel length modulation and considering $[(W/L)_{10} + (W/L)_{11}]/(W/L)_{b13} = I_{D9}/I_{D,b13}$, I_{D9} becomes equal to $(W/L)_9/(W/L)_{b12}I_{D,b12}$ only if the output CM voltage is V_{cmo}. Therefore, the output CM voltage is set to V_{cmo} without needing any resistors to sense the CM level of the output nodes.

To reduce the power consumption and input-referred noise, the transconductance and channel width and length of the input transistors is maximized making the input transistors to be biased in the sub-threshold region. By this technique, the mismatch between the input transistors is also reduced and common-mode parameters such as CMRR and PSRR are improved and the input-referred offset voltage is reduced.

By doing a simple DC analysis, the following relation between the current mirror ratios is obtained indicating that k and m are dependent on each other.

$$\begin{cases} I_{D1} = I_{D7} = k\left(\dfrac{1}{1+m}\right)I_{D1a} \\ I_{D1} = I_{D1a} \end{cases} \Rightarrow \; k = m + 1 \tag{6}$$

In the following, a detailed small-signal and noise analysis of the proposed OTA is provided.

3.2. Small-signal DC gain and transconductance

The small-signal transconductance (G_m) of the proposed RTC OTA is examined by finding the ratio between differential output short-circuit

current and the input signal, as in the following equations.

$$\begin{aligned} & i_{sc,out+} - i_{sc,out-} = i_{d1} + i_{d7} - i_{d2} - i_{d8} = 2(i_{d1} + i_{d7}) \\ & = 2i_{d1} - 2g_{m7}\frac{1}{(1-m)g_{m7a}}i_{d2a} \\ & = 2g_{m1}\frac{v_{in}}{2} - 2\frac{k}{1-m}g_{m2a}\left(-\frac{v_{in}}{2}\right) \\ & = \left(1+\frac{1+m}{1-m}\right)g_{m1}v_{in} \end{aligned} \tag{7}$$

which results in:

$$G_{m,RTC} = \left(\frac{2}{1-m}\right)g_{m1} \tag{8}$$

where g_{m1} is the small-signal transconductance of the transistor M_1. Therefore, the DC gain of the proposed OTA is given by:

$$\begin{aligned} A_{dc,RTC} &= G_{m,RTC}R_{out} \\ &\approx \left(\frac{2}{1-m}\right)g_{m1} \times (g_{m3}r_{ds3}r_{ds1} \| g_{m5}r_{ds5}r_{ds7}) \end{aligned} \tag{9}$$

where r_{dsi} is the small-signal drain-source resistance of the corresponding transistors. Assuming a dominant pole at the output node, the unity-gain bandwidth of the proposed RCT OTA is given by:

$$\omega_{t,RTC} \simeq \frac{G_{m,RTC}}{C_L} \simeq \left(\frac{2}{1-m}\right)\frac{g_{m1}}{C_L} \tag{10}$$

3.3. Frequency response

Firstly, we need to calculate the transfer function of RTC OTA. According to Fig. 4, only four nodes, X, Y_1, Y_2 and output, have been considered in the signal paths. By assuming that Y_1 and Y_2 poles are equal, neglecting other nodes, and assigning a pole to each node in the signal path, we have:

$$\begin{aligned} A_v(s) &= \frac{A_1}{(1+s/\omega_{out})(1+s/\omega_y)} + \frac{A_2}{(1+s/\omega_y)(1+s/\omega_x)(1+s/\omega_{out})} \\ &= A_{dc}\frac{(1+s/\omega_z)}{(1+s/\omega_x)(1+s/\omega_y)(1+s/\omega_{out})} \end{aligned} \tag{11}$$

where

$$\begin{aligned} & A_1 = g_{m1}R_{out}, \quad A_2 = \left(\frac{1+m}{1-m}\right)g_{m1}R_{out}, \quad A_{dc} = A_1 + A_2 \\ & \omega_{out} = \frac{1}{R_{out}C_L}, \quad \omega_x = (1-m)\frac{g_{m7}}{C_X}, \quad \omega_y = \frac{g_{m3}}{C_Y}, \quad \omega_z = \frac{2g_{m7}}{C_X} \end{aligned} \tag{12}$$

where C_L, C_X and C_Y are the equivalent capacitance at the output, X and Y nodes, respectively. So the proposed RTC OTA has three poles and one zero at the left half-plane. It is clear that by increasing m, the second pole (ω_x) is decreased resulting in degraded stability. So, there is a compromise between stability and unity-gain bandwidth and DC gain. So, in this paper, $m = 1/3$ and $k = 4/3$ are considered. Another way to improve the stability is to increase g_{m7}, which brings the second pole to a higher frequency.

3.4. Noise analysis

In the noise analysis, input transistors (M_1, M_{1a}, M_2 and M_{2a}) and current mirror transistors (M_7, M_{7a}, M_{7b}, M_8, M_{8a} and M_{8b}) have the most contribution, and the effects of other transistors can be ignored. The OTA input-referred noise has two thermal and flicker noise terms. The input-referred thermal noise power spectral density (PSD) of the proposed RTC OTA is obtained as:

$$\overline{V_{n,in,th}^2} = \frac{8kT\gamma}{g_{m1}}\left(\frac{1}{2}(m^2+1) + \frac{3}{4}\frac{g_{m7}}{g_{m1}}(1-m)^2\right) \tag{13}$$

where T is the absolute temperature, k is the Boltzmann's constant, γ is the excess noise factor, and g_{mi} is the small-signal transconductance of the corresponding transistor. Also, the input-referred PSD due to the flicker noise contribution in the proposed OTA is given by:

$$\begin{aligned} \overline{V_{n,in,1/f}^2} &= \frac{K_{FP}}{2C_{ox}(WL)_1 f}(m^2+1) \\ &+ \frac{K_{FN}}{2C_{ox}(WL)_7 f}\frac{g_{m7}^2}{g_{m1}^2}(1-m)^2\left(1+\frac{(WL)_7}{(WL)_{7a}}+\frac{(WL)_7}{(WL)_{7b}}\right) \end{aligned} \tag{14}$$

where K_{FN} and K_{FP} are the process dependent flicker noise parameters for NMOS and PMOS transistors, respectively. C_{ox} is the gate oxide capacitor per unit area. Since the transistors are biased in the sub-threshold region, the g_{m1}/g_{m7} ratio is as follows:

$$\frac{g_{m1}}{g_{m7}} \approx \frac{\frac{I_{D1}}{\zeta V_T}}{\frac{I_{D7}}{\zeta V_T}} \approx \frac{I_{D1}}{I_{D7}} \simeq 1 \tag{15}$$

where V_T is the thermal voltage that is approximately equal to 26.7 mV at the absolute temperature of 310 K (37°Celsius which is the normal body temperature) and ζ is a non-ideality factor. Considering relations (13–15), the PSD of total input-referred noise of the proposed RTC OTA is obtained as follows:

$$\begin{aligned} \overline{V_{ni,RTC}^2} &= \frac{2kT\gamma}{g_{m1}}(5m^2 - 6m + 5) \\ &+ \frac{K_{FP}}{2C_{ox}(WL)_1 f}(m^2+1) \\ &+ \frac{K_{FN}}{2C_{ox}(WL)_7 f}(1-m)^2\left(1 + k\frac{L_7^2}{L_{7a}^2} + \frac{k}{m}\frac{L_7^2}{L_{7b}^2}\right) \end{aligned} \tag{16}$$

3.5. Comparison with conventional Telescopic-Cascode OTA

In this sub-section, the proposed RTC OTA is compared with the traditional one. To make the comparison more tangible, $m = 1/3$ and $k = 4/3$ are considered. Also, for a fair comparison, the same aspect ratio in input transistors and total current consumption are used. So, the following relationship is established.

$$g_{m1,RTC} = \frac{1}{2}g_{m1,TC} \tag{17}$$

Firstly, the relation between small-signal transconductance of OTAs is determined as follows:

$$G_{m,TC} = g_{m1,TC} \tag{18}$$

$$\frac{G_{m,RTC}}{G_{m,TC}} = \frac{1}{1-1/3} = 1.5 \tag{19}$$

where $G_{m,RTC}$ and $G_{m,TC}$ are the total transconductance of the proposed and traditional OTAs, respectively.

By assuming the same intrinsic gain ($g_{mi}r_{dsi}$) for corresponding transistors in the proposed OTA and traditional one, the dc gain relation is equal to:

$$\frac{A_{dc,RTC}}{A_{dc,TC}} = \frac{G_{m,RTC}}{G_{m,TC}} \times \frac{R_{out,RTC}}{R_{out,TC}} \approx \left(\frac{1}{1-m}\right) \times 2 \approx 3 \tag{20}$$

Nonetheless, the phase margin is degraded because the proposed OTA has more non-dominant poles. Besides, we have increased the channel length of the transistors in order to reduce the flicker noise making the second pole to be smaller and resulting in more degraded phase margin.

The PSD of total input-referred noise of the traditional telescopic-

Table 1
Aspect ratio of transistors in the simulated OTAs.

Parameter	Proposed Recycling Telescopic-Cascode OTA	Conventional Telescopic-Cascode OTA
$(W/L)_{1,2}$	20 × 30.0 μm/0.5 μm	40 × 30.0 μm/0.5 μm
$(W/L)_{1a,2a}$	20 × 30.0 μm/0.5 μm	—
$(W/L)_{3,4}$	10 × 20.0 μm/2.0 μm	20 × 20.0 μm/2.0 μm
$(W/L)_{3a,4a}$	10 × 20.0 μm/2.0 μm	—
$(W/L)_{5,6}$	1 × 20.0 μm/2.0 μm	2 × 20.0 μm/2.0 μm
$(W/L)_{5a,6a}$	1 × 15.0 μm/2.0 μm	—
$(W/L)_{5b,6b}$	1 × 5.0 μm/2.0 μm	—
$(W/L)_{7,8}$	1 × 60.0 μm/10.0 μm	2 × 60.0 μm/10.0 μm
$(W/L)_{7a,8a}$	1 × 45.0 μm/10.0 μm	—
$(W/L)_{7b,8b}$	1 × 15.0 μm/10.0 μm	—
$(W/L)_{9}$	1 × 1.0 μm/0.5 μm	1 × 2.0 μm/0.5 μm
$(W/L)_{9a}$	1 × 1.0 μm/0.5 μm	—
$(W/L)_{10,11}$	1 × 1.7 μm/0.5 μm	1 × 3.0 μm/0.5 μm

cascode (TC) OTA is calculated as:

$$\overline{V_{ni,TC}^2} = \frac{8kT\gamma}{g_{m1}}\left(1+\frac{g_{m7}}{g_{m1}}\right) + 2\frac{K_{FP}}{C_{ox}W_1L_1f}\left(1+\frac{K_{FN}}{K_{FP}}\frac{W_1L_1}{W_7L_7}\left(\frac{g_{m7}}{g_{m1}}\right)^2\right) \quad (21)$$

where the first term is the thermal noise contribution and the second one is the flicker noise contribution. According to the relation (15), it is simplified as follows:

$$\overline{V_{ni,TC}^2} = \frac{16kT\gamma}{g_{m1}} + \frac{2K_{FP}}{C_{ox}W_1L_1f}\left(1+\frac{K_{FN}}{K_{FP}}\frac{W_1L_1}{W_7L_7}\right) \quad (22)$$

Finally, the relation between the thermal noise PSD of the proposed and conventional TC OTAs is obtained as the following:

$$\frac{\overline{V_{ni,th,RTC}^2}}{\overline{V_{ni,th,TC}^2}} = \frac{1}{4}\left(m^3+2m^2-4m+2+m^{-1}\right) = 0.98 \quad (23)$$

This shows approximately no thermal noise reduction. About the flicker noise PSD of the input transistors, the relation is achieved as:

$$\frac{\overline{V_{ni1,RTC,1/f}^2}}{\overline{V_{ni1,TC,1/f}^2}} = \frac{1+m^2}{2} = 0.56 \quad (24)$$

Also, the flicker noise PSD ratio of the current mirror transistors is given by:

$$\frac{\overline{V_{ni2,RTC,1/f}^2}}{\overline{V_{ni2,TC,1/f}^2}} = \frac{1}{2}(1-m)^2\left(3+m+\frac{1}{m}\right) = 1.4 \quad (25)$$

According to relations (24) and (25), in comparison with the conventional TC OTA, the input-referred flicker noise of input transistors is reduced while that of the current mirror transistors is increased in the proposed OTA. Therefore, the overall input-referred flicker noise depends on the contribution ratio of input and current mirror transistors.

4. Circuit-level simulation results

In this section, firstly, the relations obtained in Section 3 are verified by simulating both of the proposed RCT OTA and traditional TC OTA in HSPICE using TSMC 0.18-μm CMOS process. Then, the simulation results of neural recording amplifier using the proposed RTC OTA are presented. Due to the amplifier application, all of the simulations are done in body temperature (37 °C).

4.1. Proposed RTC and TC OTA comparison

The operational transconductance amplifiers shown in Fig. 4 and Fig. 5 were designed for low-power applications with a 1.8 V power supply. The simulated transistor sizes of the main amplifiers are mentioned in Table 1. It is worth mentioning that a similar biasing circuit shown in Fig. 6 is utilized in the conventional TC OTA. The channel length of transistors is chosen large enough to achieve low input-referred flicker noise. As motioned already, the transistors are biased in the sub-threshold region to maximize the amplifier transconductance.

The open-loop voltage gain frequency response is illustrated in Fig. 7 indicating that DC gain in the proposed RTC and TC OTAs is about 103.2 and 93.4 dB, respectively. Hence, the DC gain of the proposed OTA is about 9.8 dB larger than the conventional telescopic-cascode OTA. The simulated phase margin of the proposed RTC OTA and conventional TC OTA are 35.1° and 57.3°, respectively. As mentioned before, the phase margin of the proposed OTA is smaller than that of the conventional TC OTA because it has more non-dominant poles and zeros. In addition, the second pole in the proposed OTA is smaller owing to using large transistors to reduce the input-referred flicker noise. Nonetheless, in the

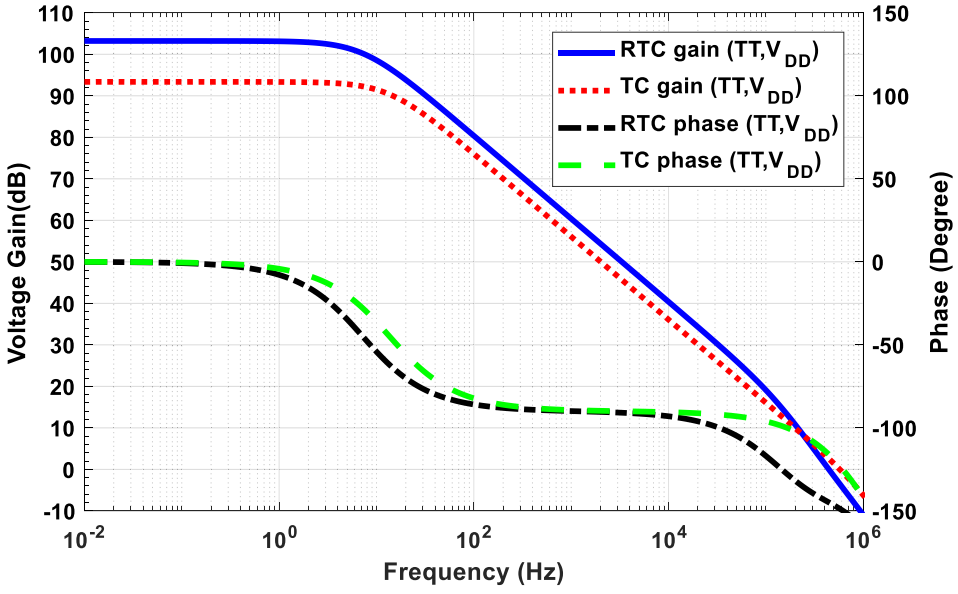

Fig. 7. Open-loop frequency response of the proposed RTC and conventional TC OTAs in typical conditions.

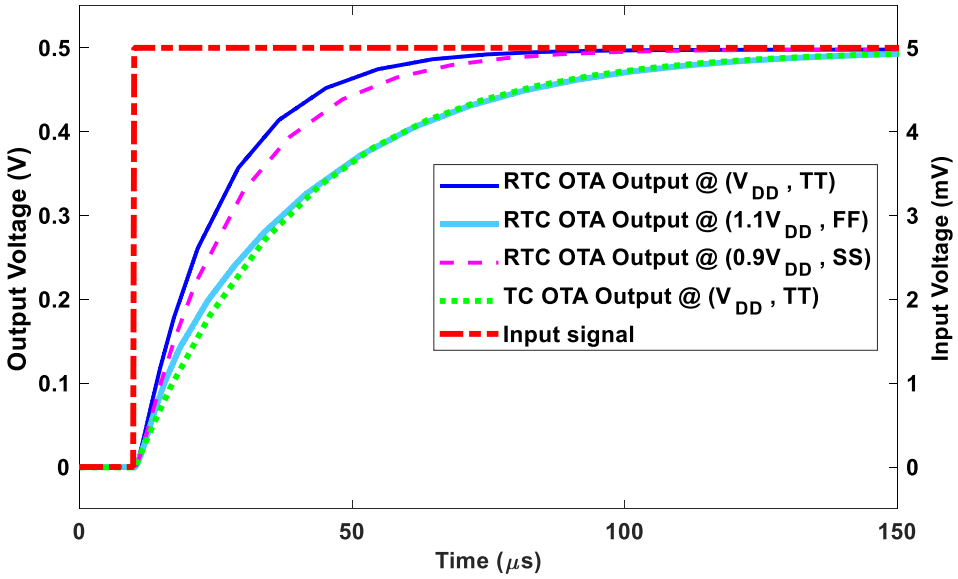

Fig. 8. Closed-loop transient response of the proposed and conventional OTAs with 0.01 feedback factor in different process corners and V_{DD} variations.

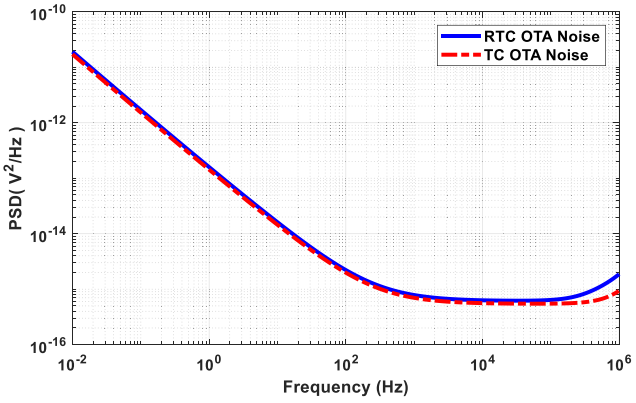

Fig. 9. Input-referred noise PSD of conventional TC and proposed RTC OTAs.

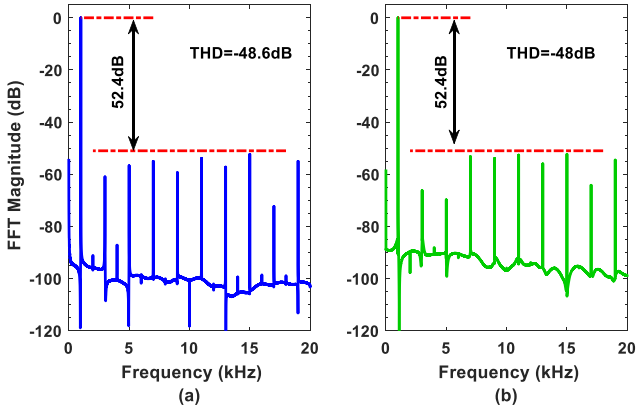

Fig. 10. Output PSD with a sinusoidal input signal with 1 kHz, 20 mV_{pp} in the (a) proposed RTC and (b) traditional TC OTAs.

simulated neural recording amplifier, the feedback factor is 0.01 to achieve a 40 dB closed-loop voltage gain. Therefore, there is any instability issue with such simulated open-loop phase margins. Actually, the closed-loop phase margin with a 0.01 feedback factor is about 86.8° and 89.7° for the RTC and TC OTAs, respectively.

Table 2
Simulation results summary of the proposed RTC and conventional TC OTAs across process and voltage variations.

Parameter	Proposed RTC OTA			Conventional TC OTA		
	TT @ V_{DD}	FF @1.1 V_{DD}	SS @ 0.9 V_{DD}	TT @ V_{DD}	FF @1.1 V_{DD}	SS @ 0.9 V_{DD}
Power consumption	1.674 µW	1.687 µW	1.683 µW	1.686 µW	1.639 µW	1.626 µW
DC gain	103.2 dB	98.5 dB	102.8 dB	93.4 dB	88.7 dB	90.2 dB
Gain × Bandwidth @ frequency ≤ 20 kHz	1.044 MHz	1.108 MHz	1.026 MHz	0.62 MHz	0.641 MHz	0.604 MHz
Phase margin	35.1°	33.7°	36.5°	57.3°	53.8°	60.1°
THD @ (10 mV_{pp},1 kHz input)	−43.5 dB	−42.6 dB	−44.5 dB	−42.3 dB	−41.2 dB	−42.2 dB
Input-referred noise (0.1 – 20 kHz)	3.77 μV_{rms}	4.37 μV_{rms}	3.92 μV_{rms}	3.56 μV_{rms}	4.17 μV_{rms}	3.75 μV_{rms}
FoM* (kHz × pF/µW)	1559.1	1642.0	1524.1	917.9	977.7	928.7
Power supply voltage	1.8 V					
Load capacitor	2.5 pF					
Technology	0.18 µm 1P6M TSMC					

* FoM = GBW × C_L/Power.

The transient simulation is done in a capacitive feedback configuration. The input and feedback capacitors are 50 pF and 0.5 pF, respectively, to have a 40 dB closed-loop gain. An input step of 5 mV differential height was applied and the output voltage is shown in Fig. 8. As it is obvious from Fig. 8, in the intended application, the proposed RTC OTA has no instability issue and it is faster than TC OTA.

The simulated input-referred noise PSD of both OTAs is shown in Fig. 9. The achieved input-referred noise in the RTC and TC OTAs is about 3.77 μV_{rms} and 3.56 μV_{rms}, respectively. It is obvious that changes in OTA noises are not noticeable. The main contributors to the total integrated noise in the proposed RTC OTA are input transistors and M_7, M_8, M_{7a}, M_{8a}, M_{7b}, M_{8b} transistors since their source terminal is not degenerated. For total harmonic distortion (THD) calculation, a sinusoidal input signal with 1 kHz frequency and 10 mV_p amplitude has been

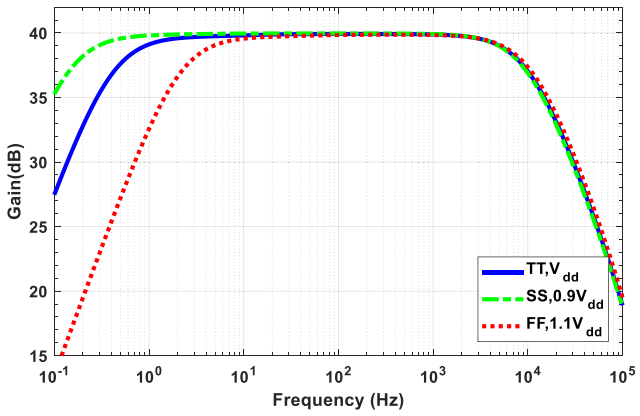

Fig. 11. Closed-loop frequency response of the proposed neural recording amplifier at 37 °C.

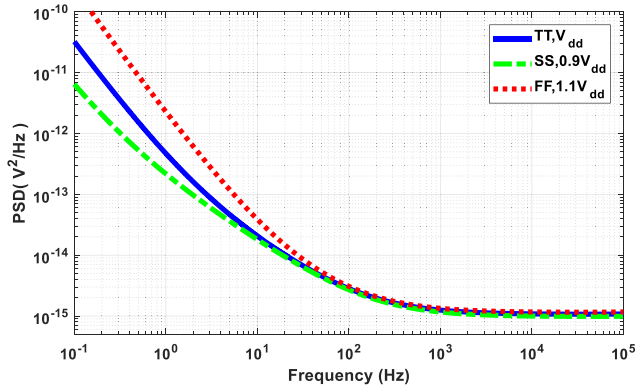

Fig. 12. Noise PSD of the proposed neural recording amplifier at 37 °C.

applied to the simulated OTAs in a closed-loop structure with a feedback factor equal to 0.01. The resulted output spectrums are illustrated in Fig. 10. The THD in the proposed RTC OTA is −43.5 dB and in TC OTA, it is −42.3 dB.

To provide a clear view, the simulation results of both OTAs are summarized in Table 2. As it is seen, analytical calculations could predict the characteristics of the proposed amplifier as well. However, the unity-gain bandwidth is not predicted very well since the size of current mirror transistors is large and carries small current that results in large parasitic capacitance and resistance at node *X*. Hence, the second pole is moved to lower frequencies making the unity-gain bandwidth of the proposed OTA to be smaller than that of the traditional TC OTA. But, if the proposed OTA is designed for a typical application without flicker noise concern, it is easy to achieve a larger unity-gain bandwidth compared to the conventional TC OTA as well.

4.2. Neural recording amplifier

The proposed neural recording amplifier depicted in Fig. 2 is designed and simulated with $C_L = 2$ pF, $C_1 = 50$ pF and $C_2 = 0.5$ pF to achieve a 40 dB closed-loop gain within 1 Hz to 10 kHz bandwidth. The capacitors are implemented by metal-insulator-metal (MIM) capacitors. The proposed OTA which has been designed in the previous sub-section is used as the core of the neural recording amplifier.

The frequency response of LNA in different process corners and power supply variations is depicted in Fig. 11. The mid-band gain is about 39.92 dB in the frequency band of 0.41 Hz–10.3 kHz which covers the frequency range of both neural LFP and AP signals as well. The low cut-off frequency shift across the process and voltage variations is the result of capacitors and pseudo resistors changes. According to the simulation results, the feedback capacitor variation range is from 439 fF in FF process corner to 595 fF in SS process corner. The feedback resistor variation range is from 1.1 TΩ in FF process condition to 12 TΩ in SS process condition. So, the dominant effect on the low cut-off frequency change belongs to the feedback resistor variation.

The simulated input-referred noise PSD in process corners and power supply variations is depicted in Fig. 12. The integrated input-referred noise of the LNA is 1.18 μV_{rms} in 1 Hz to 200 Hz bandwidth (LFP frequency band) and it is 3.34 μV_{rms} for AP frequency band (200 Hz–10 kHz). The noise efficiency factor (NEF) is a criterion for the noise-to-power trade-off which is defined as [26]:

$$NEF = V_{ni,rms}\sqrt{\frac{2I_{tot}}{\pi \times V_T \times 4kT \times BW}} \tag{26}$$

where $V_{ni,rms}$ is the input-referred noise, I_{tot} is the total current including the bias circuit, BW is the LNA bandwidth, T is the absolute temperature, and k is the Boltzmann's constant. The achieved NEF for the proposed LNA is 3.03 and 1.22 in LFP and AP frequency bands, respectively. Another benchmark for noise efficiency is the power efficiency factor (PEF) which considers the supply voltage in addition to the total current which is defined by [27]:

$$PEF = NEF^2 \times V_{DD} \tag{27}$$

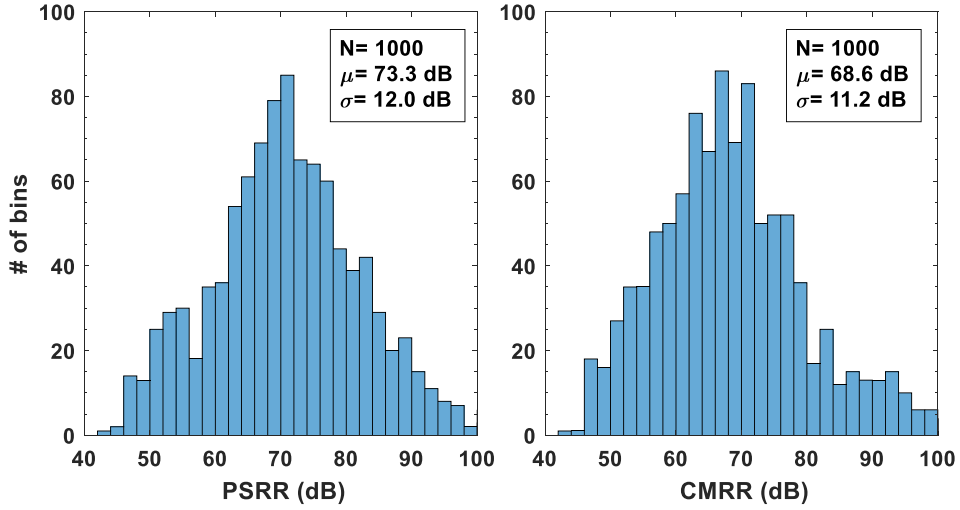

Fig. 13. Statistics distribution of CMRR and PSRR in Monte Carlo simulations with 1000 runs.

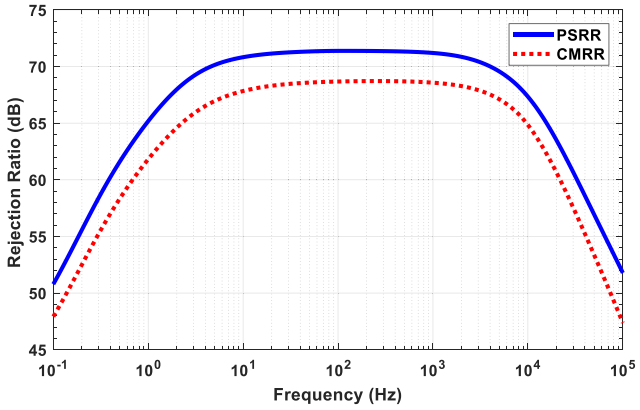

Fig. 14. Mean value of CMRR and PSRR in Monte Carlo simulations of the proposed LNA with 1000 runs versus the frequency.

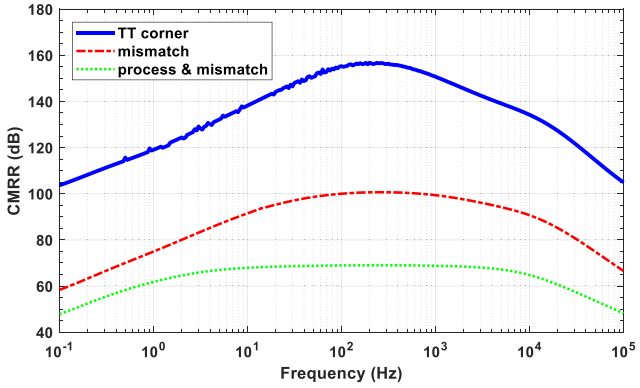

Fig. 15. Mean value of CMRR in Monte Carlo simulations with considering only device mismatches and both device mismatches and process variations.

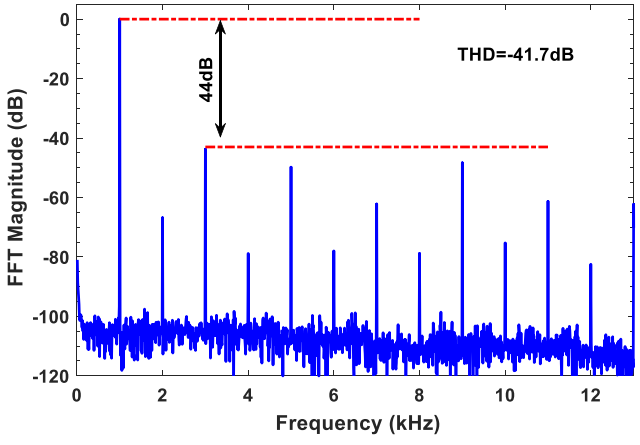

Fig. 16. THD of the LNA for a 1 mV_{pp},1 kHz sinusoidal input signal.

The achieved PEF for the proposed LNA in LFP and AP frequency ranges is about 16.58 and 2.69, respectively.

Fig. 13 shows the Monte Carlo simulation results of CMRR and PSRR at 50 Hz frequency with 1000 runs where both device mismatches and process variations have been considered according to Monte Carlo models of device components in the utilized 180 nm TSMC CMOS process. The achieved LNA CMRR and PSRR at 50 Hz frequency are 68.6 dB and 73.3 dB, respectively. In Fig. 14, the mean value of CMRR and PSRR in Monte Carlo simulation results has been illustrated versus the input signal frequency. To understand the limiting factor, an extra simulation

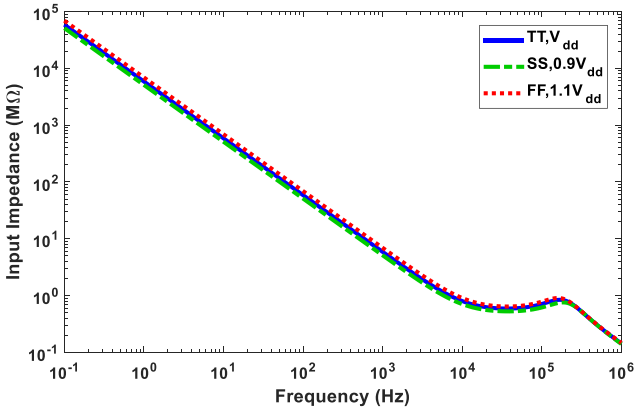

Fig. 17. The LNA input impedance versus frequency in power supply voltage variations and process corner cases.

Table 3
The LNA simulation results in different process corners and V_{DD} variations.

Parameter	TT @ V_{DD} = 1.8 V	FF @ V_{DD} = 2.0 V	SS @ V_{DD} = 1.6 V
Power consumption (μW)	1.70	1.69	1.75
Mid-band gain (dB)	39.92	39.86	39.96
Bandwidth (Hz)	0.41–10.3 k	2.1–11.3 k	0.14–10.2 k
IRN (μV_{rms} @ 1 Hz–10 kHz)	3.55	3.90	3.39
NEF	1.28	1.36	1.30
PEF	2.97	3.69	2.70
Input impedance (MΩ) @ 50 Hz	117.4	138.1	102.1
Technology	1P6M TSMC 0.18 μm CMOS		

for CMRR has been done and the CMRR frequency response has been plotted in typical conditions and also by considering only device mismatches and both device mismatches and process variations in Fig. 15. As it is seen, the effect of device mismatches is dominant.

The THD is measured in a Monte Carlo simulation with 100 runs when the input signal is 1 mV_{pp} and 1 kHz sinusoidal and both device mismatches and process variations have been considered. The PSD of the average output signal is shown in Fig. 16. At these conditions, the achieved THD of the proposed LNA is − 41.7 dB. Fig. 17 illustrates the simulated input impedance of LNA in different process corners and variations of the power supply voltage. The input impedance in typical conditions is 117.4 MΩ at 50 Hz.

A summary of the simulation results in power supply variations and different process corner cases is provided in Table 3. According to Table 3, the performance of the proposed neural recording amplifier is almost robust in process and power supply voltage variations. In Table 4, the proposed neural recording amplifier is compared with several recent similar works. According to Table 4, the performance of the proposed neural recording amplifier can be compared with the best reported similar works in current literature. This work has a good NEF in comparison with others which shows its merit in noise performance. Also, the ratio between bandwidth and power shows that it is one of the best works in power efficiency. Besides, others specifications such as CMRR, PSRR, and the input impedance are good enough for an implantable neural recording application.

5. Conclusion

In this paper, a low-power amplifier with a capacitive feedback structure is presented for neural recording systems. By using the local positive feedback network in the proposed recycling telescopic-cascode OTA, the open-loop gain and closed-loop linearity are enhanced without

Table 4
Performance comparison of the proposed neural recording amplifier with several recent similar works with BW $\geq$ 5 kHz.

Ref.	JSSC'17 [2]	ISCAS'17 [11]	JSSC'17 [8]	AEUE'18 [4]	AICSP'18 [12]	AICSP'18 [13]	JSSC'18 [28]	SSCL'19 [6]	JSSC'19 [7]	AICSP'19 [10]	AICSP'20 [5]	CSSP'22 [9]	MEJ'22 [29]	This Work
Process	40 nm	0.18 μm	40 nm	65 nm	65 nm	0.18 μm	0.18 μm	0.18 μm	0.18 μm	0.18 μm	0.18 μm	0.18 μm	0.18 μm	0.18 μm
V_{DD} (V)	1.2	1.8	1.2	1	1	1.8	0.9	1.2	1.8	0.6	1.8	1.8	1	1.8
Power (μW)	2	32.7	2.8	1.12	0.6	4.07	0.23	2.6	3.24	0.72	1.53	3.64	3.6	1.70
Signals	AP + LFP	AP + LFP	AP + LFP	AP + LFP	AP	AP + LFP	AP + LFP	AP + LFP	AP + LFP	AP + LFP	AP + LFP	AP + LFP	AP + LFP	AP + LFP
Mid-band gain (dB)	26	30–40	25.7	40	30	39.75	25.4	41–59	40	39.2	40.02	26.04	45–55	39.92
Bandwidth (Hz)	0.2–5 k	0.05–11 k	0.01–10 k	0.66–5 k	220–17 k	0.3–4.4 k	4–10 k	0.5–5 k	0.35–5.4 k	0.12–5 k	5.69–5.45 k	0.1–5.1 k	0.8–8.2 k	0.41–10.3 k
Input-referred noise (μV_{rms})	LFP. 2 AP. 7	1.34	LFP. 1.8 AP. 5.3	8.1 (1–5 k)	7.81@ (10–1 M) Hz	3.19	6.7	LFP. 2.0 AP. 3.2	LFP. 0.65 AP. 2.14	4.98	3.27	LFP. 0.63 AP. 2.86	2.1	LFP. 1.18 AP. 3.34
NEF	LFP. 7 AP. 4.9	1.92	LFP. 7.4 AP. 4.4	4.62	N/A	2.78	1.26	LFP. 9.9 AP. 3.2	LFP. 2.37 AP. 1.56	2.13	1.58	LFP. 2.5 AP. 2.3	1.7	LFP. 3.03 AP. 1.22
PEF	LFP. 58.8 AP. 28.8	6.63	LFP. 65.7 AP. 23.2	21.34	N/A	13.9	1.43	N/A	LFP. 11.1 AP. 4.38	2.71	4.5	LFP. 11.25 AP. 9.52	2.89	LFP. 16.58 AP. 2.69
CMRR (dB)	N/A	84	78	124	65	76 @50 Hz	82	70	>100	77	66.55	104.3 @50 Hz	98.28 @50 Hz	68.6 @50 Hz
PSRR (dB)	N/A	87	76	88	N/A	77.6 @50 Hz	81	N/A	>70	>60	54.99	N/A	92.48 @50 Hz	73.3 @50 Hz
Input impedance (Ω)	300 M @DC	N/A	1.6 G @DC	N/A	N/A	N/A	N/A	3 G @DC	440 M	N/A	N/A	1.8 G @10 Hz	N/A	117.4 M @50 Hz
THD	−74 dB @40 mV_{pp} ,1 kHz input	N/A	−76 dB @80 mV_{pp},1 kHz input	N/A	IM3 = -63 dB@ (9.5 and10.5) kHz	−40 dB @14.9 mV_{pp} input	N/A	−35.6 dB @1 mV_{pp} ,1 kHz input	−61 dB @5 mV_{pp},1 kHz input	−75 dB @1 mV_{pp}, 1 kHz input	−40 dB @1.2 V_{pp} output	−71.9 dB @40 mV_{pp}, 1 kHz input	−46.3 dB @1 mV_{pp},1kHz input	−41.7 dB @1 mV_{pp},1 kHz input
Meas./Sim.	Meas.	Meas.	Meas.	Sim.	Sim.	Meas.	Meas.	Meas.	Meas.	Sim.	Sim.	Sim.	Sim.	Sim.

any additional power consumption compared to the conventional TC OTA. The proposed OTA has been designed for a neural amplifier. The simulation results in 0.18-μm CMOS show the GBW in the proposed OTA is increased by about 60% in comparison with the conventional TC OTA with the same power consumption. Besides, it improves DC gain by 3.1 times. In addition, the neural amplifier has a NEF equal to 3.03 and 1.22 for LFP and AP signals, respectively, which is among the best reported works for neural recording amplifiers.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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