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A linear current-reused LNA for 3.1-10.6 GHz UWB receivers

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Abstract: An ultra-wide-band CMOS low-noise amplifier (LNA) employing a common-gate (CG) stage for wideband input matching is presented. This LNA utilizes the concurrent noise and distortion canceling techniques. Moreover, the current-reused technique exploiting the passive network instead of using the active and power consuming element is introduced to preserve the power consumption while contributing to the noise canceling trend. In other words, this topology is capable of canceling the noise effect of input transistor without consuming much current. Simulation results based on a 0.13 μm standard RFCMOS technology shows that a power gain of 13.5 dB and the noise figure of 2.7–4.2 dB over the −3-dB bandwidth of 2.6–10.7 GHz. With the presence of a weak inversion biased transistor, an input third-order intercept point (IIP3) of +5 dBm is achieved. The power consumption is 13.5 mW from a single 1.2 V power supply.

Keywords: UWB LNA, current-reuse, noise and distortion canceling

Classification: Integrated circuits

References

[1] C.-F. Liao and S.-I. Liu, "A Broadband Noise-Canceling CMOS LNA for 3.1–10.6-GHz UWB Receivers," *IEEE J. Solid-State Circuits*, vol. 42, no. 2, pp. 329–339, Feb. 2007.

[2] W.-H. Chen et al., "A Highly Linear Broadband CMOS LNA Employing Noise and Distortion Cancellation," *IEEE J. Solid-State Circuits*, vol. 43, no. 5, pp. 1164–1176, May 2008.

[3] V. Aparin and L. E. Larson, "Modified Derivative Superposition Method for Linearizing FET Low-Noise Amplifiers," *IEEE Trans. Microw. Theory Tech.*, vol. 53, no. 2, pp. 571–581, Feb. 2005.

[4] K.-H. Chen et al., "An Ultra-Wide-Band 0.4–10-GHz LNA in 0.18-μm CMOS," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 54, no. 3, pp. 217–221, March 2007.

[5] Y.-J. Lin et al., "A 3.1–10.6 GHz Ultra-Wideband CMOS Low Noise Amplifier with Current-Reused Technique," *IEEE Microw. Wireless Compon. Lett.*, vol. 17, no. 3, pp. 232–234, March 2007.

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1 Introduction

In ultra wide band (UWB) systems, designing low noise amplifiers (LNAs) which satisfy both low noise figure and high linearity is a major concern. In addition, high power gain and good impedance matching across the whole UWB band are required. Low power consumption and small size die area are the other design issues. Furthermore, achieving the high linearity in deep submicron CMOS technologies with low power supply voltage demands the linearization techniques.

Several CMOS UWB LNAs such as the feedback and common-gate (CG) amplifiers have been reported [4]. Shunt feedback amplifiers provide wideband input matching and low noise figure (NF) at the cost of high power dissipation and the stability problems. Common gate amplifiers, in contrast, are a good candidate for wideband matching. Another way is embedding a bandpass filter (BPF) in the input of the LNA as the wideband input matching network (IMN) [1]. The current-reused architectures with their outstanding trait, i.e. preserving the power consumption, are also used in the UWB design [5]. The noise and distortion cancellation techniques which have been used in [1, 2] are going to become the unique trends toward satisfying stringent features of an LNA that are the NF and third-order intercept point (IP3). In this paper, an LNA using the noise and distortion canceling trends is proposed for UWB receivers. Besides, a transistor biased in the weak inversion (WI) region is used to increase the value of IP3.

2 Proposed broadband linear LNA

2.1 Circuit topology and noise analysis

Fig. 1 shows the evolution trend toward the proposed LNA. The basic notion for noise cancellation is the combination of an auxiliary sensing amplifier with the input matching stage in a way that the noise of the matching device cancels, while the arrival signal intensify at the output. Fig. 1 (a) is the core of the noise-canceling LNA proposed in [1]. In this LNA, transistor M_3 needs high dc current to cancel the noise contribution of M_1 resulting in a high power dissipation and eventually large NF. This drawback has been also addressed in [2]. It is evident from the noise cancellation criterion, which is $g_{m2}R_{L1} = g_{m3}R_s$, that the transistor M_3 requires much more current than the transistor M_2 since the input source resistance, R_s, is generally smaller than R_{L1}. To solving this issue, the circuit shown in Fig. 1 (b) is introduced which uses current-reused technique in transistors M_2 and M_3. The effective transconductance of this circuit is given by the following where R_{in} is equal to $(R_{L1} + r_{o1})/(1 + g_{m1}r_{o1})$ and $g_{oi} = 1/r_{oi}$.

$$G_m = \frac{R_{in}}{R_{in} + R_s}\left(\frac{g_{m1}g_{m2}g_{o3}R_{L1} + g_{m3}(g_{m2} + g_{o2})}{g_{o2}g_{o3}Z_L + g_{02} + g_{o3} + g_{m2}}\right) \tag{1}$$

To cancel the noise contribution of M_1 in the output signal we must satisfy Eq. (2). As a result, the stringent criterion of high g_{m3} is eliminated.

$$\frac{R_{L1}}{R_s} = \frac{g_{m3}(g_{m2} + g_{o2})}{g_{o3}g_{m2}} \cong \frac{g_{m3}}{g_{m2}}(r_{o3}g_{m2}) \tag{2}$$

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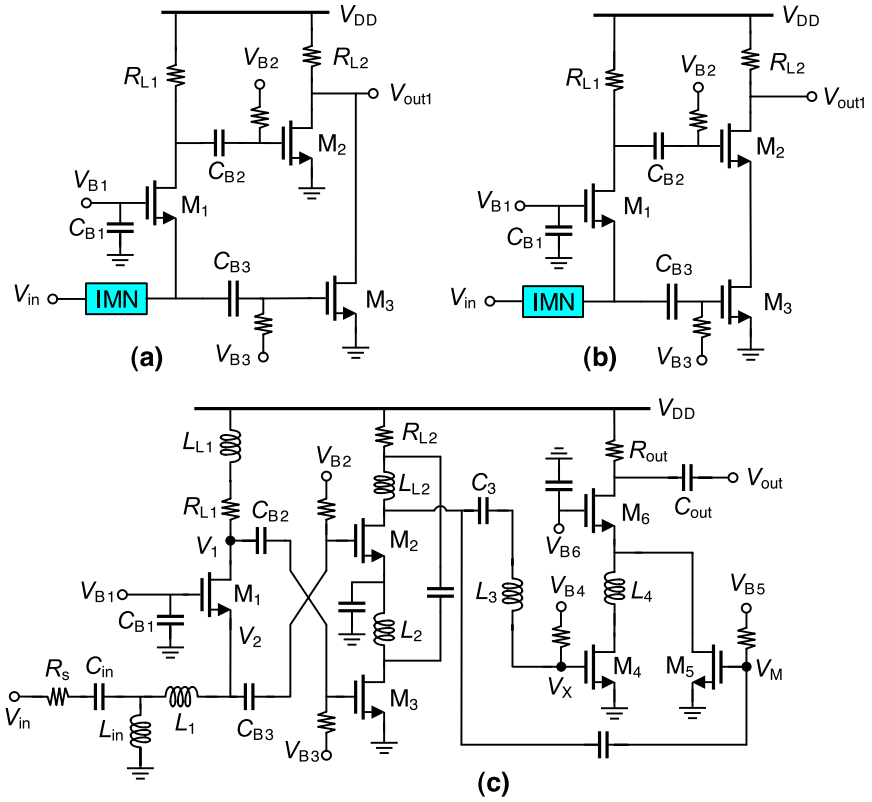

Fig. 1. (a) The LNA proposed in [1], (b) the first proposed LNA, and (c) the final proposed LNA.

The noise figure of this circuit, with the assumption of Eq. (2) is given by Eq. (3).

$$F = 1 + \frac{R_s}{R_{L1}} + \frac{R_s}{R_{L1}}\frac{\gamma}{\alpha}\frac{1}{g_{m2}R_{L1}} + \frac{\gamma}{\alpha}\frac{1}{g_{m3}R_s} \tag{3}$$

Nonetheless, the proposed LNA shown in Fig. 1 (b) has low gain and poor input IP3 (IIP3). Therefore, we have changed this circuit and proposed the final circuit shown in Fig. 1 (c) which delivers an acceptable gain. The voltage gain of the first two stages of this circuit is obtained as follows:

$$A_{v2} = \frac{R_{in}\cdot\beta(s)}{R_{in}+R_s}\cdot[g_{m3}Z_d g_{m1}(R_{L1}+sL_{L1}) + g_{m2}(sL_{L2}+Z_d)] \tag{4}$$

where $Z_d = sL_2 \| R_{L2} \| r_{o3}$ and $\beta(s) = r_{o2}/(Z_d + sL_{L2} + r_{o2})$.

We have used the shunt and series peaking techniques composed of L_{L2} and L_3, respectively, to increase the total bandwidth of the circuit. The last stage provides the output matching to the output 50 Ω with the favor of R_{out}. Since the impedance seen from the drain of transistor M_6 is much more than R_{out}, the output impedance matching is simply accomplished by setting R_{out} in the vicinity of 50 Ω. Moreover, this stage thrusts the upper frequency band to the higher points using the inductive inter-stage gain bandwidth (GBW) boosting technique by L_4. In addition, this stage with the help of transistor M_5 which is biased in the weak inversion region improves the linearity performance of the LNA.

The proposed architecture cancels the noise contribution of transistor M_1 while preserving the power using the current-reused technique in the

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second stage. According to Fig. 1 (c) the voltage noise at the drain and source of transistor M_1 due to its channel thermal noise, i.e. I_{nd1}, equal to $-\alpha I_{nd1}(R_{L1}+sL_{L1})$ and $\alpha I_{nd1}R_s$, respectively, where αI_{nd1} is the part of I_{nd1} which goes out of the transistor. The voltage noise at the output of second stage is given by:

$$v_{no}=\beta(s)[(sL_{L2}+Z_d)\cdot g_{m2}R_s-(sL_{L1}+R_{L1})Z_d g_{m3}]\cdot I_{nd1} \tag{5}$$

Accordingly the condition for noise cancellation is obtained by setting relation (5) equal to zero which results in Eq. (6). This condition can be satisfied by correctly tuning sL_{L2} and Z_d.

$$\frac{sL_{L1}+R_{L1}}{R_s}g_{m3}=\frac{sL_{L2}+Z_d}{Z_d}g_{m2} \tag{6}$$

The total NF of the proposed LNA is readily obtained as given by:

$$F=1+\frac{R_{L1}R_s}{(R_{L1}+sL_{L1})^2}+\frac{\gamma}{\alpha}\frac{1}{g_{m2}R_s}+\frac{R_s}{(R_{L1}+sL_{L1})^2}\frac{\gamma}{\alpha}\frac{1}{g_{m3}} \tag{7}$$

2.2 Linearity analysis

Linearity is a major concern in RF systems. Achieving high IIP3 in MOSFETs needs the large amount of dc current. This fact together the other limitations of the submicron CMOS designs make the linearization techniques a necessity to achieve the higher linearity in RF receivers. The optimum gate biasing and the usage of nonlinear elements for compensating the distortion of the main transistor are the common trends toward the distortion canceling [3]. In the second technique, the nonlinearity of an additional transistor which is usually biased in the weak inversion region is employed to compensate or even to cancel the nonlinearity of the main transistor which should be biased in the strong inversion region. We used this technique in the proposed LNA shown in Fig. 1 (c). For linearity analysis, we followed the same procedure as [2, 3]. First, we considered the CG input stage. The V_1 and V_2 voltages can be modeled by the following Volterra series in terms of the excitation voltage V_s.

$$V_1=A_1(s)oV_s+A_2(s_1,s_2)oV_s^2+A_3(s_1,s_2,s_3)oV_s^3 \tag{8}$$

$$V_2=B_1(s)oV_s+B_2(s_1,s_2)oV_s^2+B_3(s_1,s_2,s_3)oV_s^3 \tag{9}$$

We assumed that the major source of nonlinearity is emanated from the current of transistor M_1 defined as Eq. (10). Using the harmonic input and nonlinear current method, we solved the KCL equations in the drain and source nodes of transistor M_1 in order to find the nonlinear transfer functions of V_1 and V_2. Then for the sake of simplicity, we focused our attention to the last stage and neglected the nonlinearities of the second stage. The output voltage of the proposed LNA is expressed in Eq. (11) as the Volterra series, where V_s is the excitation voltage.

$$i_{m1}=g_{m1}(-V_2)+\frac{g'_{m1}}{2}V_2^2-\frac{g''_{m1}}{6}V_2^3 \tag{10}$$

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$$V_{out} = C_1(s)oV_s + C_2(s_1, s_2)oV_s^2 + C_3(s_1, s_2, s_3)oV_s^3 \tag{11}$$

To avoid complexity of equations, we have assumed that V_M in Fig. 1 (c) defined as $V_M = \beta(s)[g_{m3}Z_dV_1 + g_{m2}(Z_d + sL_{L2})V_2]$. This means that we behave the second stage as a linear part. According to Fig. 1 (c), we have $V_X = V_M/(1 + sC_{gs4}Z_B)$ where $Z_B = sL_3 + 1/(sC_3)$. According to [3], for a two tone excitation as $V_s = A\{cos(\omega_a t) + cos(\omega_b t)\}$ and setting $s_1 = s_2 = s_b$ and $s_3 = -s_a$, the IIP3 is defined as Eq. (12). The output voltage is calculated as Eq. (13), where Z_L is the output impedance.

$$IIP3(2\omega_b - \omega_a) = \frac{1}{6\mathrm{Re}(Z_s(s))}\left|\frac{C_1(s_a)}{C_3(s_b, s_b, -s_a)}\right| \tag{12}$$

$$V_{out} = \left[\left(g_{m4}V_x + \frac{g'_{m4}}{2}V_x^2 + \frac{g''_{m4}}{6}V_x^3\right) + \left(g_{m5}V_M + \frac{g'_{m5}}{2}V_M^2 + \frac{g''_{m5}}{6}V_M^3\right)\right] \cdot Z_L \tag{13}$$

After some math calculations, the fundamental term and the third order nonlinearity of the output voltage assuming $s_a \approx s_b \approx s$ is calculated as Eq. (14) and Eq. (15), respectively. By replacing these voltages in Eq. (13), we could calculate the Volterra series of V_{out}, where $\varepsilon(s) = 1 + sC_{gs4}Z_B$.

$$C_1(s_a) = [\beta(s)(g_{m3}Z_dA_1(s) + g_{m2}(Z_d + sL_{L2})B_1(s))](g_{m5} + g_{m4}\varepsilon(s)) \cdot Z_L \tag{14}$$

$$\begin{aligned} C_3(s_b, s_b, -s_a) &= [\beta(s)(g_{m3}Z_dA_3 + g_{m2}(Z_d + sL_{L2})B_3)] \cdot (g_{m5} + g_{m4}\varepsilon(s)) \\ &+ \left[g'_{m4}\overline{V_{X1}(s_b)V_{X2}(s_b, -s_a)} + g'_{m5}\overline{V_{M1}(s_b)V_{M2}(s_b, -s_a)}\right] \\ &+ (1/6)\left[g''_{m4}V_{X1}^3(s) + g''_{m5}V_{M1}^3(s)\right] \end{aligned} \tag{15}$$

For calculating the IIP3, it is sufficed to pay our attention to the Eq. (14) and Eq. (15). According to the IIP3 formula, for distortion canceling we must minimize the third order nonlinearity of the output voltage, i.e. $C_3(s_b,s_b,-s_a)$. Based upon this fact, we derived the conditions for eliminating its terms. According to the 3rd–order nonlinearity of the output voltage in Eq. (15), we derived the conditions in which all three terms of this equation equal to zero. For neutralizing the first term of Eq. (15), we must satisfy the condition given in Eq. (16) where $Z_1(s) = (R_{L1} + sL_{L1})||(1/sC_1)$, and $Z_2(s) = 1/(sC_2)$. Moreover, C_1 and C_2 are modeled as the total capacitances of drain and source of transistor M_1, respectively. Z_s is the transfer function of the input BPF.

$$\frac{Z_2(s)Z_s(s)}{Z_1(s)(Z_2(s) + Z_s(s))} = \frac{g_{m3}}{g_{m2}}\frac{Z_d}{(Z_d + sL_{L2})} \tag{16}$$

From Eq. (16) since $Z_2 \gg Z_s$, we have $(g_{m3}/g_{m2})(Z_d/(Z_d + sL_{L2})) = (R_s/(R_{L1} + sL_{L1}))$ which is exactly the condition for canceling the noise contribution of the transistor M_1. As a result, this first term is deleted as we cancelled the noise of transistor M_1 in the output voltage. This indicates the simultaneous noise and distortion canceling. For neutralizing the second term of Eq. (15), we must satisfy the Eq. (17).

$$\begin{aligned} &g'_{m4}[2V_{X1}(s_b)V_{X2}(s_b, -s_a) + V_{X1}(-s_a)V_{X2}(s_b, s_b)] \\ &+ g'_{m5}[2V_{M1}(s_b)V_{M2}(s_b, -s_a) + V_{M1}(-s_a)V_{M2}(s_b, s_b)] = 0 \end{aligned} \tag{17}$$

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Inasmuch as $s_a \approx s_b$, and $Z_d(s_b - s_a)$ equals zero, two terms of $V_{X2}(s_b, -s_a)$ and $V_{M2}(s_b, -s_a)$ are zero. The remnant of Eq. (17), however, is not eliminated. Consequently, neutralizing the 2nd-term of Eq. (15) is just partially satisfied. Since the absolute value of $(1+sC_{gs4}Z_B(s))^3$ based upon the design values is around unity, the criterion for canceling the third term of Eq. (15) is summarized as Eq. (18). This is done by trimming the V_{gs} of transistor M_5 which is biased in the weak inversion region as also suggested in [3].

$$\frac{g''_{m4}}{g''_{m5}} = -|1 + sC_{gs4}Z_B|^3 \tag{18}$$

3 Simulation results

The proposed LNA shown in Fig. 1 (c) was designed in a 0.13 μm standard RF CMOS technology. The simulations were performed using HSPICE RF tools. Fig. 2 shows the simulation results. As is seen the *NF* varies from 2.7 to 4.2 dB in the whole band. Both input and output return losses are less than 11 dB, and the power gain is 13.5 dB over the −3 dB bandwidth of 2.6–10.7 GHz. A two-tone signal around 6 GHz is used to simulate the linearity performance of the proposed LNA. According to Fig. 2, the IIP3 is around +5 dBm. The total circuit consumes 13.5 mW from a single 1.2 V power supply.

To compare the proposed LNA with the other reported UWB LNAs, we have used the figure of merit, *FOM*, defined as $FOM = OIP3/\{(NF-1)\times P_{dc}\}$, [3]. The simulation results as well as the FOM of the proposed LNA are summarized in Table I. As is seen, the proposed LNA achieves a good *FOM* compared to the other recently reported UWB CMOS LNAs.

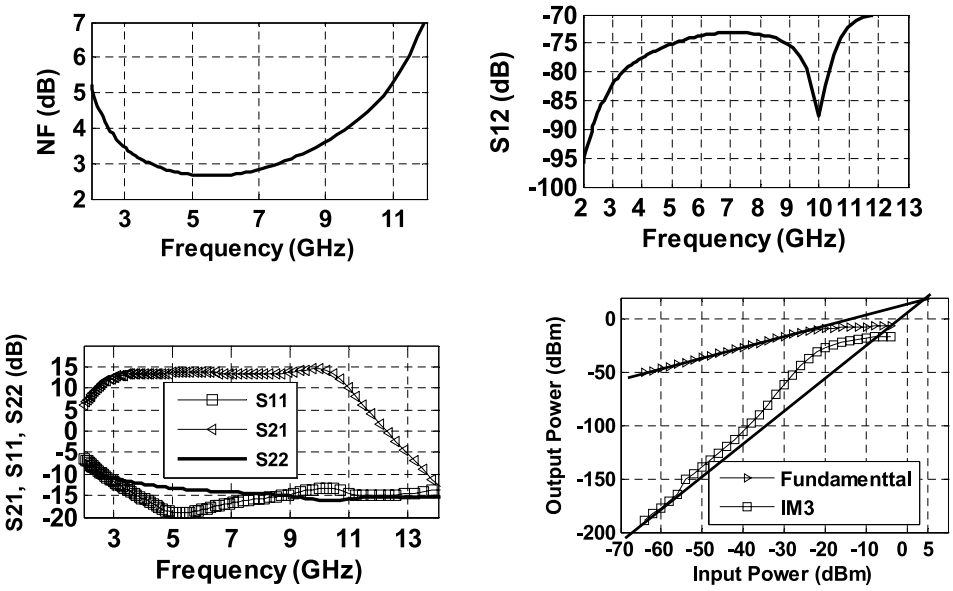

Fig. 2. Simulation results of the proposed LNA.

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Table I. Comparison of various LNAs with the proposed UWB LNA.

Ref.	3dB B.W. (GHz)	S_{11} (dB)	Power (mW)	Gain (dB)	NF (dB)	IIP3 (dBm)	FOM
[1]	1.2-11.9	<-11	20	9.7-7.5	4.5-5.1	-6.2	0.06
[4]	0.4-10	<-10	12	12.4	4.4-6.5	-6	0.21
[5]	3.4-10.6	<-8	11.9	13.5-16	3.1-6	-7	0.64
This work+	2.6-10.7	<-11	13.5	13.5	2.7-4.2	+5	3

+ Simulation results.

4 Conclusions

A distortion and noise-canceling LNA targeting UWB receivers has been proposed. This LNA provides the noise cancellation with the help of current-reused architecture. Besides some part of the distortion cancellation is done by satisfying the noise cancellation condition. Moreover, the linearity improves using a transistor biased in the weak inversion region. The Volterra series of the output voltage indicates that this architecture is capable of eliminating the nonlinearities of the LNA. The simulation results show that the proposed LNA achieves a minimum NF of 2.7 dB, $S_{11} < -11$ dB, $S_{21} > 13.5$ dB and IIP3 $= +5$ dBm in a 0.13 μm CMOS technology. The total power dissipation is 13.5 mW from a single 1.2 V power supply.

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