

## LOW-VOLTAGE DOUBLE-SAMPLED HYBRID CT/DT $\Sigma\Delta$ MODULATOR FOR WIDEBAND APPLICATIONS\*

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A hybrid continuous-time (CT)/discrete-time (DT) multi-stage noise-shaping (MASH)  $\Sigma\Delta$  modulator architecture is presented. The double-sampling technique is employed in the DT second stage modulator. A flat and a unity signal transfer functions (STFs) are used in the first and second stage modulators, respectively, to make the modulator robust to nonlinearities of the analog circuitry and well suited for low-voltage applications without influencing the inherent anti-aliasing behavior of the first stage CT modulator. Unlike the conventional MASH architecture, this structure is insensitive to the amplifier limited DC gain of CT stage and avoids the need of compensation for finite gain-bandwidth induced error in CT loop filter. Behavioral simulations confirm the effectiveness of the proposed scheme over existing cascaded topologies.

*Keywords:* Analog-to-digital converter;  $\Sigma\Delta$  modulation; continuous-time circuits.

### 1. Introduction

Nowadays there is an increasing demand for both higher sampling rates and higher resolution while not expanding the power consumption too much. Because of some meaningful advantages over DT implementations, CT modulators have received increasing attention over the last years in broadband applications, and used in hybrid CT/DT  $\Sigma\Delta$  modulators, provide faster operation and embedded anti-aliasing filtering, while consuming lower power.<sup>1</sup>

Handling DT modulators in broadband applications faced some circuitry limitations. A useful approach for circumventing these limitations is to employ the double-sampling technique.<sup>2,3</sup> In this method, since the integrator circuit operates during both phases of the clock, the effective sampling frequency of the system is

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twice that of the clock frequency. This results in doubling the available time for settling of the integrators if the OSR and input signal bandwidth are fixed.

In CT  $\Sigma\Delta$  architectures the analog coefficients are realized by some inaccurate RC time constants. Although by using an RC time constant tuning approach, the accuracy is improved to 10%,<sup>4</sup> however this is not enough for MASH structures. Therefore the cascaded modulators are not a suitable candidate for high-order CT  $\Sigma\Delta$  modulators. An alternative  $\Sigma\Delta$  architecture that reduces the sensitivity to noise leakages of traditional MASH structures has been recently presented for DT modulators and called Sturdy MASH (SMASH) modulator.<sup>5</sup> This topology replaces the error cancellation logic required in traditional MASH modulators by properly combining the stages outputs by direct feedback paths from the 2nd stage output to the 1st stage input.

In this paper, a new hybrid CT/DT SMASH modulator is proposed for high-resolution low oversampling ratio (OSR) broadband applications. The proposed SMASH  $\Sigma\Delta$ M topology employs the double-sampling technique in the DT second-stage modulator in order to reduce the power consumption of the overall modulator.

### 2. Proposed $\Sigma\Delta$ Modulator

Figure 1 shows the proposed double-sampling hybrid CT/DT SMASH  $\Sigma\Delta$  modulator. The first stage is a CT modulator with an  $m$ -bit internal quantizer and the second stage is a DT one with an  $n$ -bit quantizer. In high-speed modulators, the amplifiers are operated near their maximum bandwidth, so the power consumption dramatically increases with sampling frequency. To reduce the power consumption of the proposed  $\Sigma\Delta$  modulator, the double-sampling technique is used in the second stage. The operating frequency of the second stage is chosen from half of the first-stage modulator. So, the effective sampling frequency of both stages are the same and since the operating frequency of the second stage is halved with respect to the overall

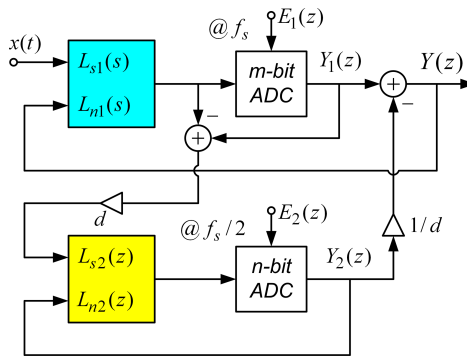


Fig. 1. The general block diagram of proposed hybrid CT/DT SMASH modulators.

modulator sampling rate, the power consumption of the second-stage modulator is reduced.

For CT integrators, a simple finite impulse response (FIR) NTF is chosen. The cascade of integrators feedforward (CIFF) architecture is adopted in the first stage, because it has the advantage of requiring only one DAC, compared to its multiple feedback counterparts that need as many DACs as the modulator order. As stated in Ref. 6, CT DACs are sensitive to the clock jitter, so by reducing the number of DACs, more insensitivity against clock jitter is achieved.

The STF of the first-stage modulator is designed based on the technique proposed in Ref. 7 in order to achieve a flat STF. By employing this technique, the output swing of the integrators is reduced and the effect of amplifiers nonlinear DC gain is mitigated since there is little input related signal at the output of the integrators. Moreover, by using the design methodology presented in Ref. 7, the inherent anti-aliasing behavior of the first-stage CT modulator is not affected. It is worth mentioning that as analyzed in Ref. 7, if a DT modulator is designed with a unity STF and then converted to a CT one, the resulting STF would see a (large) peak in out-of-band frequencies where the out-of-band input signals to the modulator are highly amplified rather than attenuated resulting in degraded anti-aliasing behavior. Since the sampling operation in the CT modulators occurs inside the loop, the anti-aliasing behavior is achieved by both the low-pass forward loop and the noise shaping property of the  $\Sigma\Delta$  loop preceding the quantizer. As in the unity STF, the input of integrators does not contain any product of the input signal, the first attenuation made by the forward loop filter is missed and weak anti-aliasing behavior is obtained. However, since in the flat STF, the input signal is weakly processed by the integrators, the anti-aliasing behavior of the modulator will be preserved.

The second-stage STF does not affect the anti-aliasing performance of the modulator since the input signal is not processed by the second-stage DT modulator. Therefore, a unity STF is selected in order to reduce the output swing requirement of the second-stage integrators.

As a design example the proposed SMASH 2-2 structure shown in Fig. 2 is considered. The DT  $NTF_1(z)$  is chosen as:

$$NTF_1(z) = (1 - z^{-1})^2. \quad (1)$$

The method of equivalent loop filters has been applied to convert Eq. (1) into its CT counterpart.<sup>6</sup> Compensating excess loop delay has been considered in the presented design as proposed in Ref. 4. The multibit non-return-to-zero DAC shape is used in the proposed design for low power consideration and reasonable clock jitter tolerance.<sup>6</sup> Moreover, the local resonance is used to optimally distribute the zeroes of the NTF within the required signal bandwidth. Considering a linear model for the quantizers in Fig. 2, it can be shown that the  $z$ -domain transform of the modulator

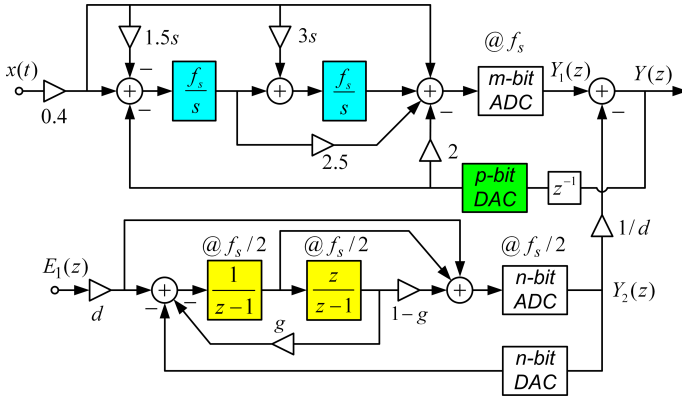


Fig. 2. Proposed hybrid SMASH 2-2 structure.

output is given by:

$$\begin{aligned}
 Y(z) &= X(z) - E_2(z) \frac{NTF_2(z)NTF_1(z)}{d} \\
 &= X(z) - E_2(z) \frac{(1 - z^{-1})^2(1 - (2 - g)z^{-1} + z^{-2})}{d}, \tag{2}
 \end{aligned}$$

where  $X(z)$  stands for the input signal and  $E_2(z)$  is the quantization noise of the second-stage modulator. The parameter  $d$  is chosen to be 4 in the presented work. The optimal value of parameter  $g$  which is a function of the OSR is selected by minimizing the second-stage quantization noise in the overall modulator output and hence maximizing the signal-to-quantization noise ratio (SQNR) resulting in:

$$g_{opt} = \frac{2 \sin \frac{3\pi}{OSR} - 18 \sin \frac{2\pi}{OSR} + 90 \sin \frac{\pi}{OSR} - \frac{60\pi}{OSR}}{24 \sin \frac{\pi}{OSR} - 3 \sin \frac{2\pi}{OSR} - \frac{18\pi}{OSR}}. \tag{3}$$

The  $m = 3$  and  $n = 4$  multibit quantizers are used in the first and second stages, respectively. However, note that feeding the second-stage output back to the first-stage input requires a DAC with double full scale and one more bit than the largest of the resolutions of the ADCs in the stages in order to account for the digital summation of the stages outputs if  $d = 1$ .<sup>8</sup> In the case of  $d = 4$  which is used here, a  $p = 7$  multibit DAC is needed in the first-stage loop filter, making its realizations very difficult. In general, the resolution of this extra DAC is  $p = \max(m, n + \log_2(d)) + 1$ .

On the other hand, tight timings for the quantizer and the digital adder used in the first-stage loop of Fig. 2 might become impractical for high sampling rates, especially when the DAC linearization techniques are needed. Figure 3 shows a way to solve this problem and also to avoid the need for an extra high resolution DAC in

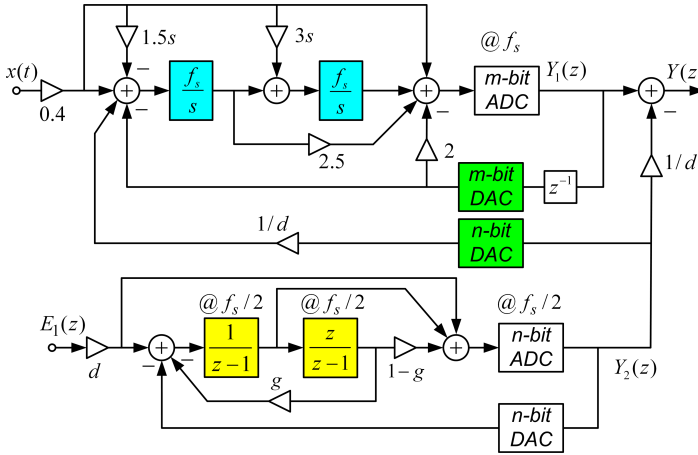


Fig. 3. Modified version of proposed hybrid SMASH 2-2 structure.

the first-stage modulator. The digital adder is replaced by an extra DAC at the input of the 1st integrator in the first-stage loop filter and another digital adder at the final output. In other words, the digital adder in Fig. 2 is replaced by one analog adder realized together by the first integrator and one digital adder outside of the first-stage modulator’s loop.

The implementation of the first-stage adder in Fig. 3 can be performed by a simple passive adder. Since no active adder was used in front of the first-stage quantizer, the error extraction is performed at the input of the second loop filter using the output of the first-stage quantizer, the input signal and the output of first-stage integrators as proposed in Ref. 5. Of course, this complicates the realization of second-stage integrators and quantizer somewhat and is a main drawback of SMASH modulators where the first-stage quantization error is not processed in that stage unlike the conventional MASH structures. So, there is a trade-off between using an active adder preceding the quantizer of the first-stage modulator and the realization of the second-stage building blocks. Nonetheless, since in the proposed modulator structure the double sampling approach is employed in the second-stage modulator resulting in the halved sampling frequency respected to the first-stage modulator, therefore, the realization of extra paths in the second-stage modulator is mitigated somewhat and this is another advantage of the proposed hybrid CT/DT modulators over the conventional SMASH topologies.

Since the error extraction process is done at the input of the second-stage loop, an active adder is necessary in the second-stage modulator. The operating frequency of this adder was chosen to be  $f_s/2$ . Note that by using this method, two active adders with opposite phases are needed. The outputs of these adders are fed into the second-stage quantizer which has an operating frequency of  $f_s/2$  too. In this way, the second-stage quantizer is implemented with  $2 \times 16$  comparators with a sampling rate

of  $f_s/2$ . This will result in the same effective sampling frequency as the first-stage modulator.

### 3. Simulation Results

All simulations have been carried out in the time domain using MATLAB and Simulink. The assumed *OSR* was 8 for all simulations so the optimum value for  $g$  is 0.11.  $m = 3$  and  $n = 4$  multibit quantizers were utilized in the proposed modulator shown in Fig. 3. Figure 4 plots the SNDR versus the first integrator DC gain of SMASH and equivalent MASH structure while all the other integrators are ideal. As seen, the proposed structure is less sensitive to the opamp finite DC gain while achieving high resolution and requires only 30 dB DC gain in the first integrator’s amplifier. A low DC gain requirement allows using simple single stage amplifiers rather than two-stage ones, resulting in some power savings. Behavioral simulations

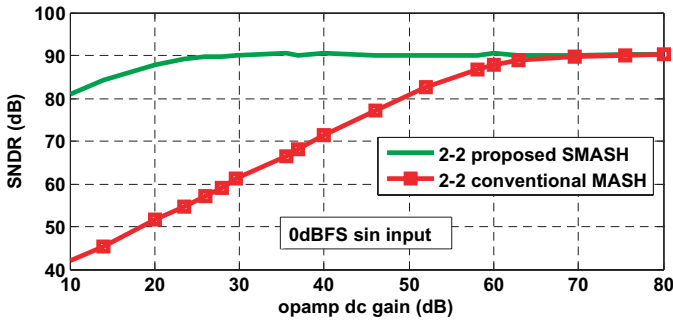


Fig. 4. SNDR versus amplifier DC gain of the first integrator.

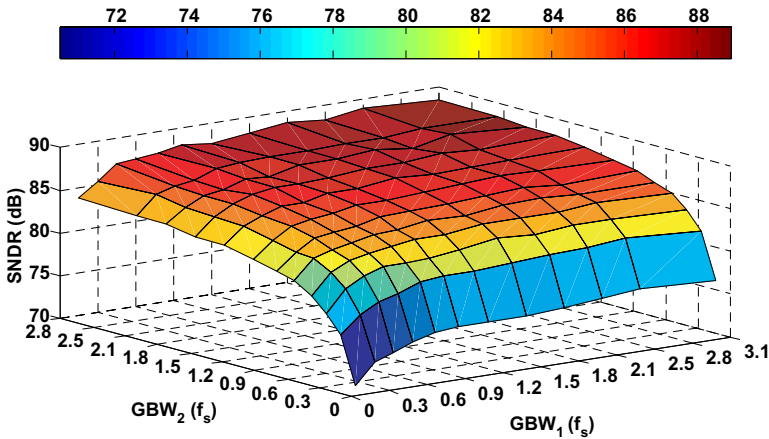


Fig. 5. SNDR versus opamp gain-bandwidth of the first stage integrators.

reveal that, the first and second opamps that are more important than the second-stage opamps, need a bandwidth higher than  $1.8f_s$  and  $1.2f_s$  respectively, as shown in Fig. 5, where  $f_s$  is the sampling rate of the modulator. Note that as mentioned in Ref. 6, CT MASH structures need more bandwidth than the above reported values even after the error compensation of this non-ideality. So, the use of SMASH structure results in both reduced bandwidth requirements and omitting the need for compensation for finite gain-bandwidth induced error in CT loop filter.

As stated later, the double-sampling technique is used in the second-stage DT modulator. It should be noted that any mismatch between the sampling capacitors in double-sampling technique produces unwanted noise which is folded into the inband frequencies.<sup>2</sup> Hence, the SNDR is degraded. This is the main drawback of the double sampling modulators. Several techniques have been proposed to alleviate the quantization noise folding.<sup>3,9</sup> But since the effect of the sampling paths mismatch is attenuated by noise shaping property of the first-stage modulator in the presented work, the double sampling approach is efficiently employed in the proposed modulator without requiring any additional technique to alleviate the mismatch problem. The SNDR degradation of the proposed modulator is negligible (less than 1 dB) even with a 0.5% mismatch between the sampling paths of the second-stage integrators as illustrated in Fig. 6.

Figure 7 shows the anti-aliasing behavior of the proposed modulator. In these simulations, a 0 dBFS signal tone added with a  $-14$  dBFS noise tone at  $f_s - (BW)/4$  was applied to the input of the modulator. As is clear, the proposed modulator which uses a flat STF in the first stage has the same anti-aliasing behavior where a flat STF is not employed. In other words, the anti-aliasing behavior of the first-stage CT modulator is completely preserved while using a flat STF in the first stage. But, as mentioned before, by employing a unity STF in the first stage, the attenuation of the loop filter will be missed and hence about 13 dB lower anti-aliasing attenuation is achieved compared to the flat STF. Also as shown in this figure, the CT STF

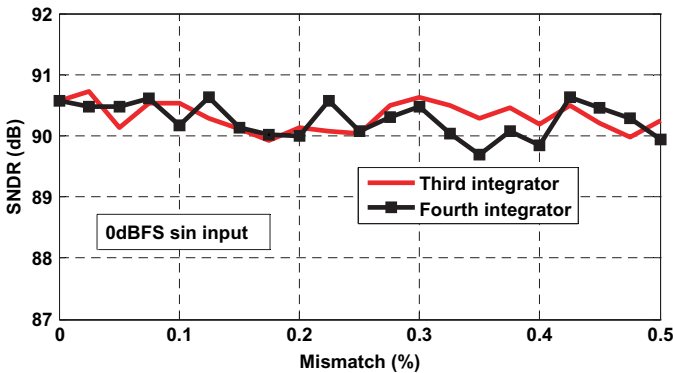


Fig. 6. SNDR versus sampling paths mismatch of the second stage integrators.

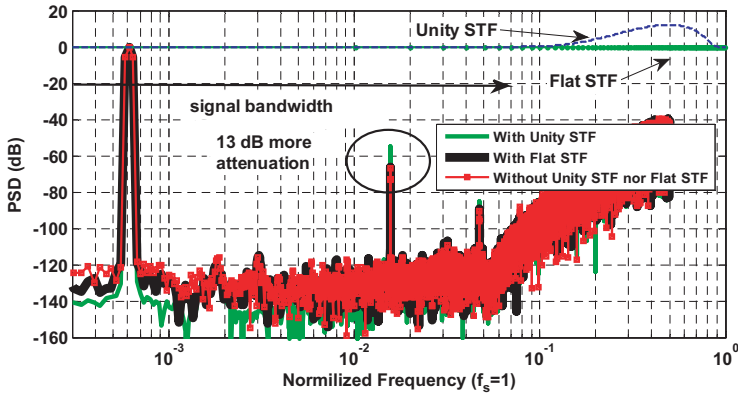


Fig. 7. Anti-aliasing behavior of the proposed SMASH 2-2 modulator.

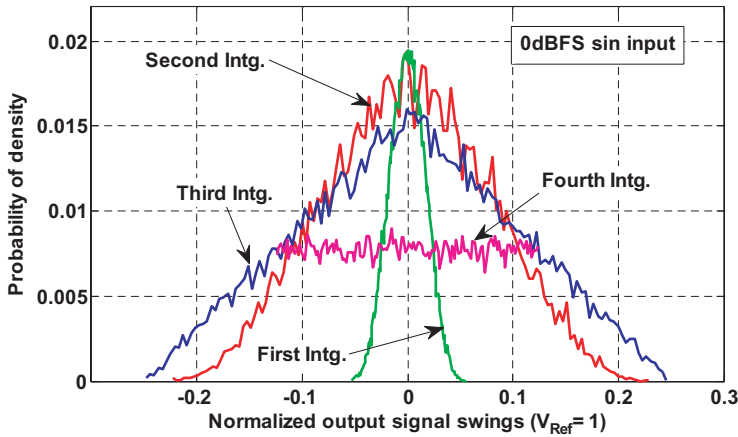


Fig. 8. Output swing of the integrators.

achieves an out-of-band peak after designing the DT STF as unity and then converting that into a CT one unlike the flat STF.

As illustrated in Fig. 8, the integrators output swing in the proposed modulator are much less than the reference voltage level due to the usage of a flat STF in the first stage and a unity STF in the second-stage modulators, respectively. This makes the proposed modulator more feasible in low supply voltage nanometer CMOS technologies.

#### 4. Conclusions

A new hybrid CT/DT SMASH  $\Sigma\Delta$  modulator was proposed. Compared to the traditional MASH structure, the proposed structure provides reduced sensitivity to



the circuit non-idealities. The double-sampling technique is employed in the second-stage discrete-time modulator with much less sensitivity to the sampling paths mismatch. The output swing requirement of the integrators was relaxed by employing a flat STF in the first-stage and a unity STF in the second-stage modulators without any sacrificing the inherent anti-aliasing behavior of the first-stage CT modulator. The proposed modulator is most suitable for wideband and low-voltage A/D converters.

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