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A hybrid CT/DT double-sampled SMASH ΣΔ modulator for broadband applications in 90 nm CMOS technology

Mohammad Hossein Maghami · Mohammad Yavari

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Abstract In this paper, a hybrid continuous-time (CT)/discrete-time (DT) multi-stage noise shaping (MASH) sigma–delta (ΣΔ) modulator architecture for broadband applications is presented. The double-sampling technique is employed in the DT second-stage modulator in order to reduce the power consumption of the overall modulator. Flat and unity signal transfer functions are used in the first- and second-stage modulators, respectively, to relax the output swing of the analog building blocks without influencing the inherent anti-aliasing behavior of the first-stage CT modulator. The proposed structure is insensitive to the amplifier limited dc gain of CT stage and avoids the need of compensation for finite gain-bandwidth induced error in CT loop filter. As a design example, the proposed MASH 2-2 modulator is designed in a 90 nm CMOS technology with 1 V power supply. Circuit level simulation results with HSPICE achieve the maximum SNDR of 74.8 dB and dynamic range of 76.5 dB in 12.5 MHz bandwidth with 17 mW power consumption while operating at 200 MHz sampling rate.

Keywords Analog-to-digital converters · ΣΔ modulation · Continuous-time circuits · Switched-capacitor circuits

1 Introduction

Digital communication applications demand analog-to-digital converters (ADCs) with several megahertz signal bandwidth and high resolution. Two commonly used ADCs in communication systems are pipelined ADCs and sigma–delta (ΣΔ) modulators. Pipeline ADCs are used in wideband moderate-accuracy applications, while ΣΔ modulators are suitable for high-accuracy applications due to their inherent immunity to the circuit non-idealities [1]. Nowadays, there is an increasing demand for both higher sampling rate and higher resolution while not expanding the power consumption too much. Most of the earlier ΣΔ modulators are based on switched-capacitor (SC) circuit techniques, whereas ΣΔ modulators with continuous-time (CT) loop filters can potentially achieve higher clock frequency with lower power consumption. Therefore, CT modulators have received increasing attention over the last years due to their several meaningful advantages over discrete-time (DT) implementations [2].

In practice there exist some non-idealities making CT modulators hard to realize the theoretical systems in an integrated circuit. Among them are large variations of the integrator's time constants, high sensitivity to the clock jitter and excess loop delay (ELD). Recent approaches have been drawn to the hybrid ΣΔ modulators featuring the integration of initial stage(s) as CT integrator(s) and subsequent DT integrators in the loop filter [3, 4]. These hybrid modulators are suitable for high-speed applications. Note, that if the second stage in a cascaded modulator is realized as a CT one, the first-stage sampling circuit would see a resistive input, requiring a low output impedance stage for the sampling circuit amplifier. But, since this circuit is a SC one operating at a high sampling rate, the first-stage sampling circuit amplifier must be a fast single-stage design, and therefore, driving a resistive load would be very difficult. Mainly, due to this reason, DT integrators are employed in the later stages of the cascaded modulators [3].

Employing ΣΔ modulators in wideband applications demands using low oversampling ratios (OSRs). Lowering

M. H. Maghami · M. Yavari (✉)
Integrated Circuits Design Laboratory, Department of Electrical Engineering, Amirkabir University of Technology, Tehran, Iran
e-mail: myavari@aut.ac.ir

the OSR will result in reduction of the modulator's accuracy. Consequently, novel modulator structures are needed to alleviate the reduction of resolution in wideband applications. A useful approach for handling DT modulators in broadband applications is to employ the double-sampling technique [5]. In this method, the integrator circuit operates during both phases of the clock resulting in either doubling the OSR or the available time for settling of the integrators if the OSR and input signal bandwidth are fixed.

Since the OSR must be restricted to low values in wideband applications, a usual design choice in order to achieve the required dynamic range is to employ multi-stage noise shaping (MASH) architectures with multi-bit quantization. These ΣΔ modulator topologies circumvent the stability problems related to the high order loops, but, they are sensitive to the quantization noise leakage caused by mismatches between the analog and digital signal processing parts [6]. Moreover, in CT ΣΔ structures, the analog coefficients are realized by some inaccurate RC time constants which will decrease the modulator's accuracy. An alternative ΣΔ modulator architecture that reduces the sensitivity to the noise leakage of traditional MASH structures has been recently presented for DT modulators and called the Sturdy MASH (SMASH) modulator [7, 8]. This topology replaces the error cancellation logic required in traditional MASH modulators by inherent analog filtering of the modulator stages. This is achieved by simply feeding back the second stage output to the most insensitive node of the first stage modulator which is the output of the first stage quantizer.

In this work, a new hybrid CT/DT SMASH modulator is proposed for low OSR broadband applications. As an example, a cascaded 2-2 modulator is designed in a 90 nm CMOS process achieving a maximum SNDR of 74.8 dB and dynamic range of 76.5 dB over 12.5 MHz signal bandwidth with 17 mW power consumption. The proposed SMASH ΣΔM topology employs the double-sampling technique in the DT second-stage modulator in order to reduce the power consumption of the overall modulator.

This paper is organized as follows. In Sect. 2, the structure of the proposed modulator and its system level design are presented. Several behavioral simulations of the proposed modulator are reported in Sect. 3. Section 4 presents the circuit level design of both CT first-stage and DT second-stage modulators. The circuit level simulation results are provided in Sect. 5. Finally, Sect. 6 concludes the paper.

2 Proposed ΣΔ modulator and system-level design

2.1 Proposed ΣΔ modulator

Figure 1 shows the proposed double-sampling hybrid CT/DT SMASH ΣΔ modulator. L_{si}, L_{ni} and E_i denote the signal loop filter, noise loop filter and quantization error of the ith stage, respectively. The first-stage is a CT modulator with an m-bit internal quantizer and the second-stage is a DT one with an n-bit quantizer. In high-speed ΣΔ modulators, the amplifiers are operated near their maximum bandwidth. In this case, the power consumption dramatically increases with the sampling frequency. To reduce the power consumption of the proposed ΣΔ modulator, the double-sampling technique is used in the second-stage modulator. The operating frequency of the second-stage modulator is chosen half of the first-stage modulator. So, the effective sampling frequency of both stages are the same and since the operating frequency of the second-stage is halved with respect to the overall modulator sampling rate, the power consumption of the second-stage modulator is reduced.

For the first-stage CT integrators, a simple finite impulse response (FIR) noise transfer function (NTF) is chosen. The cascade of integrators feedforward (CIFF) architecture is adopted in the first-stage modulator, because of the relaxed output swings and also this scheme has an advantage of requiring only one multibit digital-to-analog converter (DAC), compared to the multiple feedback counterpart used in distributed feedback structures that needs as many DACs as the modulator's order. As stated in [2], CT DACs are sensitive to the clock jitter, so, by reducing the number of DACs, more insensitivity against clock jitter is reached. The DT second-stage modulator is also designed in a CIFF form, because of requiring one multibit feedback DAC. This would result in reducing the silicon die area and some power saving.

The signal transfer function (STF) of the first-stage modulator is designed based on the technique proposed in [9] in order to achieve a flat STF. CT ΣΔ modulators are considered to be very interesting because of their implicit anti-aliasing filter. However, while an anti-aliasing filter is not necessary, still a 'no-overload' filter should precede the modulator to prevent the instability. This filter is

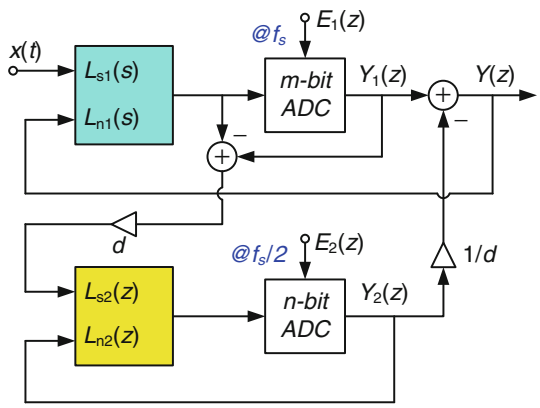


Fig. 1 Proposed hybrid CT/DT SMASH ΣΔ modulator

required in CT ΣΔ modulators when the STF has a peak at the out-of-band frequencies. This causes out-of-band signals to be amplified, which can corrupt the correct operation of the modulator and cause the instability. It is worth mentioning that as analyzed in [9] if a DT modulator is designed with a unity STF [10] and then converted to a CT one, the resulting STF would see a (large) peak at the out-of-band frequencies where the out-of-band input signals to the modulator are highly amplified rather than attenuated resulting in a degraded anti-aliasing behavior.

Also by employing a flat STF, the output swing of the integrators is reduced and the effect of amplifiers dc gain nonlinearity is mitigated since there is little input related signal at the output of the integrators. Moreover, the inherent anti-aliasing behavior of the first-stage CT modulator is not affected by employing this STF. Since the sampling operation in the CT modulators occurs inside the loop, the anti-aliasing behavior is achieved by both the low-pass forward loop and the noise shaping property of the ΣΔ loop preceding the quantizer. As in the unity STF, the input of integrators does not contain any product of the input signal, the first attenuation made by the forward loop filter is missed and a weak anti-aliasing behavior is obtained. However, since in the flat STF, the input signal is weakly processed by the integrators, the anti-aliasing behavior of the modulator is preserved.

As a result of not processing the input signal by the second-stage modulator, there is an option between choosing a unity STF and a flat one in the second-stage modulator. But, since the second-stage STF does not affect the anti-aliasing performance and the unity STF is a stricter condition than the flat STF, the unity STF is chosen in order to achieve low signal swing at the output of second-stage integrators.

2.2 Design example

As an example, the proposed SMASH 2-2 ΣΔ modulator shown in Fig. 2 is designed and simulated. 3- and 4-bit quantizers are used in the first and second stages, respectively, in order to achieve more dynamic range. In this design, the DT $NTF_1(z)$ is chosen as:

$$NTF_1(z) = (1 - z^{-1})^2 \tag{1}$$

In [2] the method of equivalent loop filters has been applied to convert DT modulators into their CT counterpart. The main idea was to convert every existing loop filter from the DT to the CT domain. Therewith exactly the same modulator output spectrum could be obtained. The same procedure is followed for converting (1) to its CT counterpart. Result is the second order, first stage of Fig. 2.

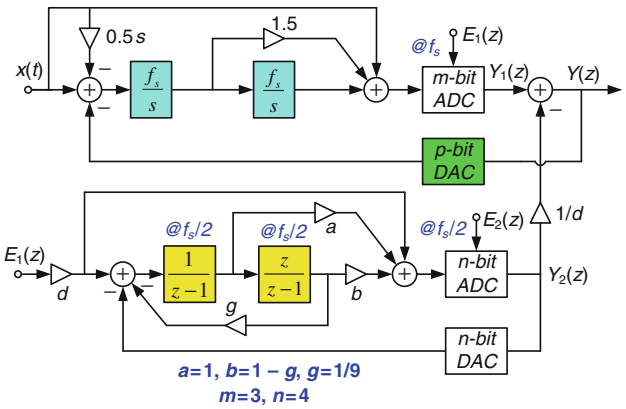


Fig. 2 Proposed hybrid CT/DT SMASH 2-2 ΣΔ modulator

In the proposed design, the DAC feedback pulse shape is chosen considering the clock jitter sensitivity, required gain-bandwidth, and slew rate of the opamps. The use of a decaying waveform minimizes the jitter influence, but the opamp power is increased due to the higher slew rate requirement [11]. Therefore, the non-return-to-zero (NRZ) DAC shape is used for low power considerations and reasonable jitter tolerance. But, it is worth mentioning that there is a concern when using NRZ waveform that is code transitions. To alleviate this problem with NRZ DAC, when a DAC unit element is not selected, that current can be switched to the amplifier common-mode input voltage to minimize transient glitches on the DAC current source outputs [3].

For further reduction of the clock jitter sensitivity, a multibit internal quantizer is used. Equation 2 shows that the in-band noise power (IBN) can be reduced with more internal DAC levels where σ_t, V_{FS}, T_s, and B_{int} correspond to the clock jitter standard deviation, input signal full-scale amplitude, sampling period, and the number of quantization bits, respectively. $A_{NRZ,MB}$ is an activity factor which is typically equal to 1 in the multibit NRZ DAC shape. This factor shows the contribution of DAC waveform in clock jitter sensitivity and is determined and verified by simulations [2].

$$IBN_{\sigma_t} = \frac{V_{FS}^2}{\left(2^{B_{\text{int}}} - 1\right)^2}\left(\frac{\sigma_t}{T_s}\right)^2 \frac{A_{NRZ,MB}}{OSR} \tag{2}$$

Considering $NTF_2(z)$ in Fig. 2 and to match it with an FIR one, second stage modulator coefficients are chosen as $a = 1$ and $b = 1 - g$. So, we have:

$$NTF_2(z) = 1 - (2 - g)z^{-1} + z^{-2} \tag{3}$$

Using a linear model for the quantizers in Fig. 2, it can be shown that the z-domain transform of the modulator output signal in the ideal case is given by:

$$Y(z) = X(z) - E_2(z)\frac{NTF_2(z)NTF_1(z)}{d} = X(z) - E_2(z)\frac{(1-z^{-1})^2[1-(2-g)z^{-1}+z^{-2}]}{d} \quad (4)$$

where $X(z)$ stands for the input signal and $E_2(z)$ is the quantization noise of the second-stage modulator. The parameter d is chosen to be 4 in this work. Regards to the selected NTFs, the contribution of the second-stage quantization error in the overall output is as follows:

$$Y(z)\big|_{E_2(z)} = -\frac{(1-z^{-1})^2[1-(2-g)z^{-1}+z^{-2}]}{d} \quad (5)$$

Now a pair of complex conjugate zeros is introduced in the overall NTF whose location depends on coefficient g. The optimal value of g to maximize the SNDR is obtained as follows [6]:

$$g_{opt} = \arg\min_{g} \int_0^{f_s/(2\times OSR)} \left|(1-z^{-1})^2[1-(2-g)z^{-1}+z^{-2}]\right|^2 df \quad (6)$$

Assuming $z = e^{j\theta}$ and $\theta = 2\pi f/f_s$, the optimal value of g can be found by nulling the first derivative, resulting in:

$$g_{opt} = \frac{2\sin(3\pi/OSR) - 18\sin(2\pi/OSR) + 90\sin(\pi/OSR) - (60\pi/OSR)}{24\sin(\pi/OSR) - 3\sin(2\pi/OSR) - (18\pi/OSR)} \quad (7)$$

As is clear in Fig. 2, the $m = 3$ and $n = 4$ multibit quantizers are used in the first and second stages, respectively. However, note that feeding the second-stage output back to the first-stage input requires a DAC with double full scale and one more bit than the largest of the resolutions of the ADCs in the stages in order to account for the digital summation of the stages outputs if $d = 1$ [12]. In the case of $d = 4$ which is used here, a $p = 7$ multibit DAC is needed in the first stage loop filter making its realizations very difficult. In general, the resolution of this extra DAC is $p = \max(m, n + \log_2(d)) + 1$. On the other hand, tight timings for the quantizer and the digital adder used in the first-stage loop in Fig. 2 might become impractical for high sampling rates, especially when the DAC linearization techniques are needed.

Figure 3 shows a way to solve this problem and also to avoid the need for an extra high resolution DAC in the first-stage modulator. The digital adder is replaced by an extra DAC at the input of the first integrator in the first-stage loop filter and another digital adder at the final output.

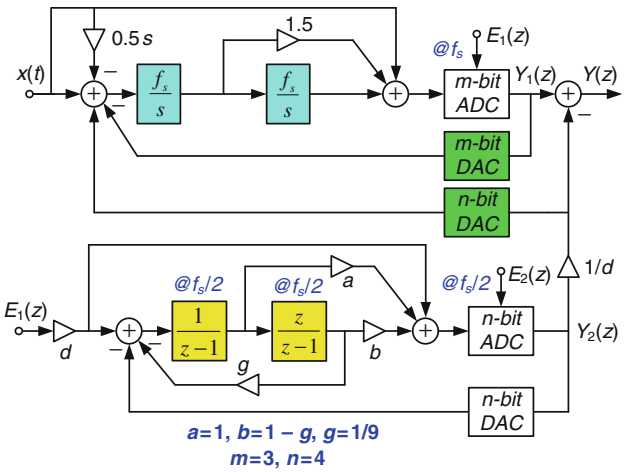


Fig. 3 Proposed hybrid CT/DT SMASH 2-2 ΣΔ modulator with some modifications

In other words, the digital adder in Fig. 2 is replaced by one analog adder realized together by the first integrator and one digital adder outside of the first stage modulator's loop. One can write the equations introduced previously and find that there is no discrepancy between the modified version and the firstly presented modulator.

3 Behavioral simulation results

In order to show the effectiveness of the proposed ΣΔ modulator, several behavioral simulations using MATLAB/Simulink are provided in this section. The OSR was assumed 8 in all simulations. The input signal bandwidth is 12.5 MHz, and hence the sampling frequency is 200 MHz.

One of the most important concerns in MASH ΣΔ modulators is the noise leakage due to the opamp non-idealities used in the integrators. Figure 4 plots the SNDR versus the first integrator dc gain of SMASH and equivalent MASH structures while all the other integrators are ideal. As is seen, the proposed structure is less sensitive to the opamp limited dc gain, while achieving a high resolution (SNDR = 90 dB). A low dc gain requirement allows us to use simple single-stage opamps rather than two-stage ones, leading to more power saving. Behavioral simulations also reveal that the first and second opamps that are more important than the second-stage opamps need a bandwidth higher than 1.8 f_s and 1.2 f_s, respectively. Note,

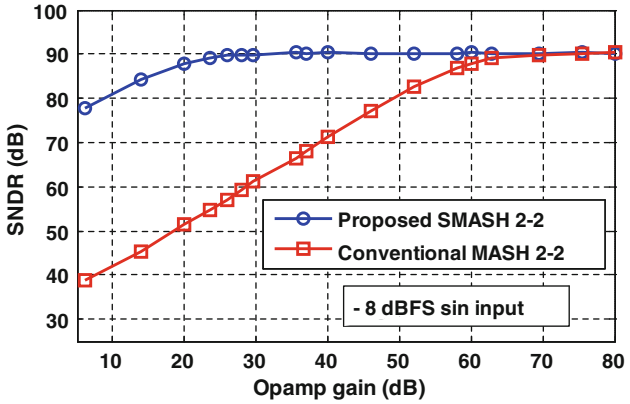


Fig. 4 SNDR versus amplifier dc gain of the first integrator

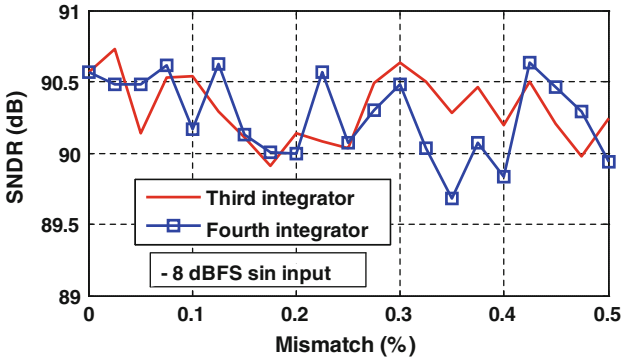


Fig. 5 SNDR degradation versus the sampling paths mismatch

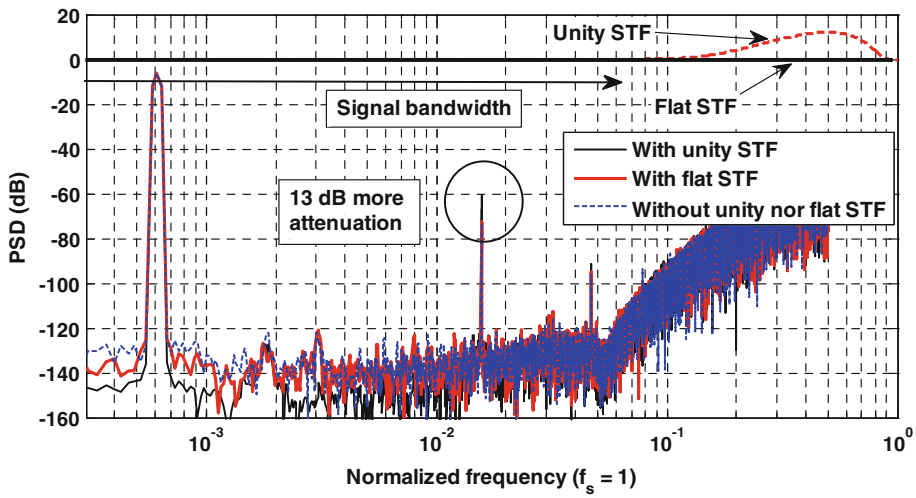
that as mentioned in [13], CT MASH structures need more bandwidth than the above mentioned values even after the error compensation of this non-ideality. So, the use of SMASH structure results in reduced bandwidth requirements and omitting the need for compensation for finite gain-bandwidth induced error in CT loop filter.

As stated before, the double-sampling technique is used in the second-stage DT modulator. It should be noted that any mismatch between the sampling capacitors in the double-sampling technique produces an unwanted noise which is folded into the in-band frequencies. Hence, the SNDR is degraded. This is the main drawback of the double-sampling modulators. Several techniques have been proposed to alleviate the quantization noise folding such as one proposed in [14]. But, since in this work the effect of the sampling paths mismatch is attenuated by noise shaping property of the first-stage modulator, the double-sampling approach is efficiently employed in the proposed modulator without requiring any additional technique to alleviate the mismatch problem. The SNDR degradation of the proposed modulator is negligible since as shown in Fig. 5, there is less than 1 dB SNDR degradation even with a 0.5% mismatch between the sampling paths of the second-stage integrators.

Figure 6 shows the anti-aliasing behavior of the proposed ΣΔ modulator. In these simulations, a −6 dBFS sinusoidal signal added with a −20 dBFS noise tone at $f_s - (BW)/4$ was applied to the input of the modulator. As is clear, the proposed cascaded modulator which uses a flat STF in the first-stage has the same anti-aliasing behavior where a flat STF is not employed. In other words, the anti-aliasing behavior of the first-stage CT modulator is completely preserved while using a flat STF in the first-stage modulator. Note that, if a conventional unity STF is employed in the first-stage modulator, the anti-aliasing behavior of the modulator is degraded. As shown in this figure, the CT STF has an out-of-band peak after designing the DT STF as unity and then converting it to a CT one unlike the flat STF.

As illustrated in Fig. 7, the integrators output swing in the proposed ΣΔ modulator are much less than the reference voltage level due to the usage of a flat STF in the first-stage and a unity STF in the second-stage modulators. This makes the proposed ΣΔ modulator more feasible in low supply voltage nanometer CMOS technologies.

Fig. 6 Anti-aliasing behavior of proposed ΣΔ modulator



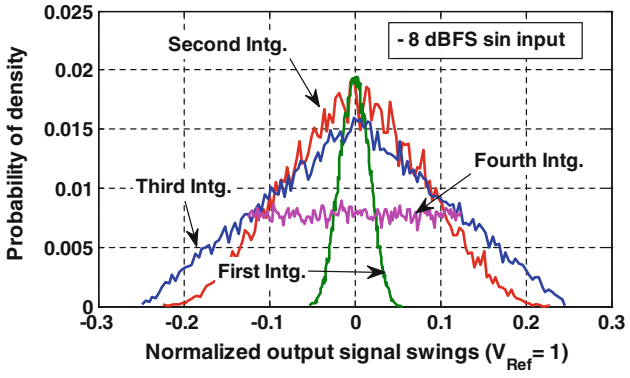


Fig. 7 Output swing of integrators

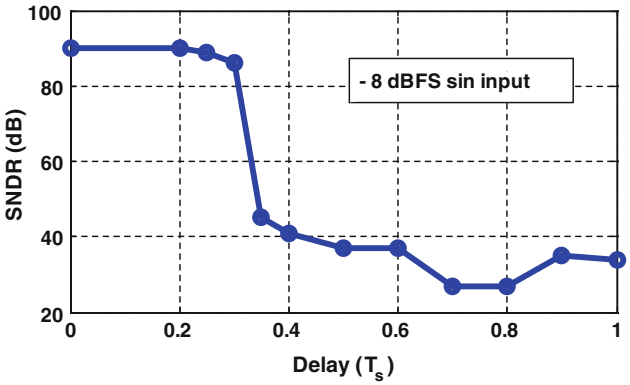


Fig. 8 SNDR versus loop delay

CT ΣΔ modulators suffer from a problem not seen in DT designs that is nonzero delay between the quantizer clock edge and the time when a change in output bit is seen at the feedback point in the modulator known as ELD. ELD may cause the modulator to be unstable [15]. In order to minimize the ELD problem, one of the viable solutions is to reduce the delay of the loop comprising of the quantizer and the DAC. This is accomplished with the help of a high speed comparator embedded in the quantizer in order to reduce the quantizer delay. The ELD problem is analyzed using behavioural simulations. With the delay of $0.3T_s$ which is 1.5 ns in this design, the modulator doesn't show any degradation in its noise shaping property as shown in Fig. 8. Consequently by using a high speed comparator, it is not necessary to compensate for this effect which will result in some power saving in the overall modulator.

4 Circuit level design

4.1 Continuous-time first stage design

The proposed modulator is designed in a 90 nm CMOS technology. It operates at a clock frequency of 200 MHz with a 1 V power supply. The amplitude of the differential reference is 1 V. Firstly, the design of CT first-stage is introduced and then the building blocks of second-stage DT modulator are described. Figure 9 shows the CT first-stage modulator's circuit diagram. The value of integrating resistors and full-scale current DAC are chosen based on their intrinsic noise effect on the modulator's dynamic range. The procedure of reaching these values will be explained later. The implementation of this modulator involves the circuit design of the loop filter with active-RC integrators, 3-bit flash quantizer, passive adder, and a current-steering feedback DAC. The design of these blocks is described in this sub-section.

4.1.1 Loop filter

The second-order loop filter of this design is implemented with CIFF architecture as shown in Fig. 9. There are three types of commonly used CT integrators: active-RC integrators, G_m-C integrators and MOSFET-C integrators. In this work, the first-stage CT modulator uses active-RC integrators rather than G_m-C and MOSFET-C integrators for its superior linearity, simplicity, parasitic insensitivity as well as the overall power consumption [2]. The ideal transfer function of an active-RC integrator is given by:

$$I(s) = k_i \frac{f_s}{s} = \frac{1}{sRC} \tag{8}$$

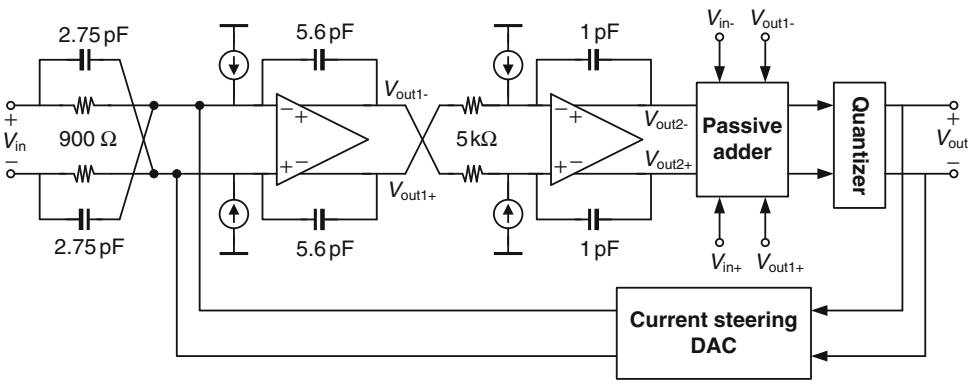


Fig. 9 The circuit implementation of CT first-stage modulator

where f_s is the sampling frequency and k_i is the integrator feedforward gain. Assuming the amplifier dc gain is very high, the input nodes of the opamp closely meet the virtual ground condition, so that the input resistor R performs a linear V/I conversion. Performance limitations result from the limited linearity of the V/I conversion (here the resistor R). A total harmonic distortion (THD) less than −90 dB can be achieved using integrated polysilicon resistors in active RC integrators [2]. Although it seems that the linearity and noise requirements on the second integrator is more relaxed when compared to the first one, but, because of using a low OSR in this work, the second integrator is also implemented as an active-RC one. However, one of the most important concerns in active-RC integrators is the large process variations in CMOS technology which can result in large RC time constant uncertainty, and hence, resulting in the system performance degradation considerably. In order to solve this problem, an on-chip automatic RC tuning circuit is necessary. This can be done by using the master–slave capacitor array tuning scheme presented in [16]. In this method, each integration capacitor in the loop filter is realized as a tunable capacitor with a binary-weighted capacitor array and is digitally controlled by a master RC tuning block.

Figure 10 shows the first-stage active-RC integrator. A multibit current-steering DAC is used in this design. Each current cell contains a cascode current source and a pair of current switches controlled by feedback thermometer digital codes. Two bias current sources inject common mode currents to prevent a common-mode offset from appearing at the amplifier virtual grounds. As discussed later, a simple folded-cascode opamp is chosen to satisfy the required characteristics of amplifiers used in the

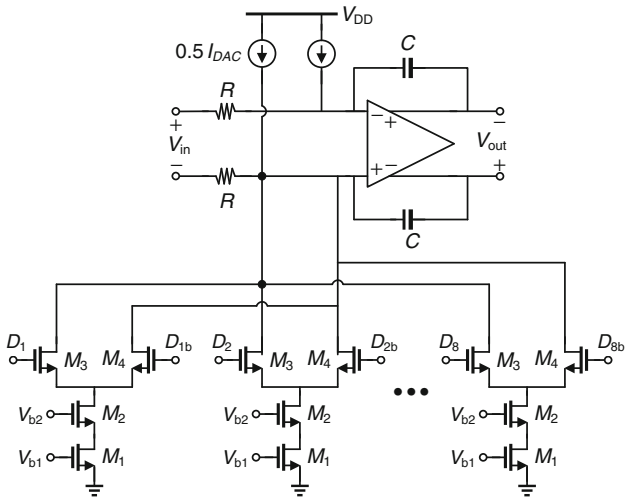


Fig. 10 First active-RC integrator with current-steering DAC

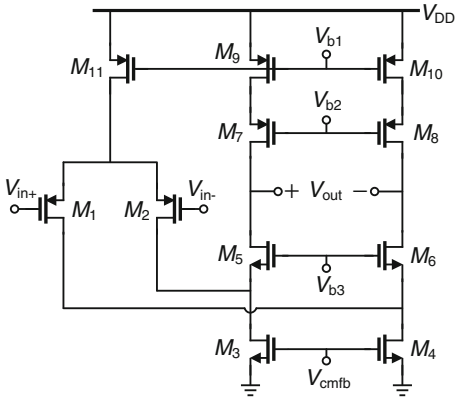


Fig. 11 Folded-cascode operational amplifier

presented modulator (Fig. 11). Each part of the integrator of this figure will be discussed in a separate sub-section. But, first of all, the modulator front-end noise analysis is performed in order to clear how the value of integrating RC time constants and current-steering DAC are calculated.

4.1.2 *Modulator front-end noise analysis*

As the device noise at the modulator front-end is not attenuated, it is a limiting factor in the total input referred noise of the ΣΔ modulator. There are three noise sources of the front-end including (1) noise of the two input integrating resistors, (2) thermal and flicker noise of the opamp, and (3) noise of the current-steering feedback DAC to the virtual grounds of the opamp.

The total IBN of the two input resistors is as follows:

$$\overline{V_{R_{in}}^2} = 8kTR_{in}\Delta f \tag{9}$$

where k represents the Boltzmann constant and is 1.38×10^{-23} J/K, T represents the absolute temperature and Δf is the input signal bandwidth. In this design, the value of input resistors are chosen to be 900 Ω, generating a thermal noise power about 91.3 dB lower than the full-scale input signal. As mentioned later, the sampling frequency is 200 MHz. So, using Eq. 8, this will result in a value of 5.6 pF for the first integrating capacitor.

As the thermal noise generated by second integrating resistor is attenuated when referred to the input of the modulator, its value is not as important as the first integrating resistor. This resistor is chosen to have a high value in order to reduce the integrating capacitor of the second integrator. This will cause the opamp used in this integrator see a low capacitor load and so reaching a desired gain-bandwidth obtained with lower power consumption. As shown in Fig. 9, the second integrating resistor has a value of 5 kΩ, resulting in 1 pF integrating capacitor.

The input referred noise, including thermal and flicker noises, of the opamp shown in Fig. 11 can be expressed as:

$$\overline{V_n^2} = 8kT\gamma\left(\frac{1}{g_{m1,2}} + \frac{g_{m3,4}+g_{m9,10}}{g_{m1,2}^2}\right) + 2\frac{K_P}{(WL)_{1,2}C_{ox}f} + 2\frac{K_N}{(WL)_{3,4}C_{ox}f}\frac{g_{m3,4}^2}{g_{m1,2}^2} + 2\frac{K_P}{(WL)_{9,10}C_{ox}f}\frac{g_{m9,10}^2}{g_{m1,2}^2} \quad (10)$$

The total in-band thermal noise equals to:

$$\overline{V_{in,th}^2} = 8kT\gamma\left(\frac{1}{g_{m1,2}} + \frac{g_{m3,4}+g_{m9,10}}{g_{m1,2}^2}\right)\Delta f \quad (11)$$

and the total in-band flicker noise is given by:

$$\overline{V_{in,1/f}^2} = 2\left(\frac{K_P}{(WL)_{1,2}C_{ox}f} + \frac{K_N}{(WL)_{3,4}C_{ox}f}\frac{g_{m3,4}^2}{g_{m1,2}^2} + \frac{K_P}{(WL)_{9,10}C_{ox}f}\frac{g_{m9,10}^2}{g_{m1,2}^2}\right)\ln(f_{\max}/f_{\min}) \quad (12)$$

In the above equations, K_P and K_N represent the flicker noise coefficients of the pMOS and nMOS transistors, respectively. γ is an excess noise factor used in the thermal noise modeling of transistors [17] and f_{max} and f_{min} are the indicator of input signal bandwidth.

The rules for reaching low thermal noise are considered in this design. For example, large input devices are used to increase the transconductance of transistors in order to reduce both amplifier thermal and flicker noises. The large device size also reduces the input offset voltage.

Looking at one single current cell in the DAC shown in Fig. 10, the major thermal noise is from transistor M_1. Thermal noise from M_2, M_3 and M_4 are greatly attenuated because of the source generation. The total in-band thermal noise power from M_1 can be expressed as [18]:

$$n_{DAC}^2 = \frac{16kT\gamma I_{DAC}R_{in}^2}{(V_{GS}-V_{TH})}\Delta f \quad (13)$$

where $(V_{GS} - V_{TH})$ is the overdrive voltage of the nMOS current source transistor, R_{in} is the first integrating resistor and I_{DAC} is the DAC full scale current. Given $T = 300°K$, $V_{GS} - V_{TH} = 0.2$ V, $I_{DAC1} = 0.888$ mA and $\Delta f = 12.5$ MHz, the total in-band thermal noise power of the first stage DAC would be 84 dB lower than the full-scale input signal. Since the $I_{DAC2} = (1/d)\ I_{DAC1}$, the in-band thermal noise power of the DAC from the second stage to the input of the first stage would be 90 dB lower than the full scale input signal. Note, that the full scale current of the first stage DAC (I_{DAC1}) is calculated using the equation expressed in [3] as:

$$I_{DAC} = \left(\frac{V_{FS}}{R_{in}} - \frac{-V_{FS}}{R_{in}}\right) = \frac{2V_{FS}}{R_{in}} \quad (14)$$

4.1.3 Operational amplifiers

Eliminating all digital noise cancellation filters makes the SMASH structure less sensitive to the opamp limited dc gain compared to the traditional MASH scheme. System level simulations shown in Fig. 4 show that 25 dB opamp dc gain is sufficient to provide 90 dB SNDR. To add a safety margin for process and temperature variations, the opamps with 35 dB open loop dc gain are designed. The folded-cascode opamp shown in Fig. 11 is chosen to satisfy the required dc gain. Transistor sizes are chosen in a way that their intrinsic noise do not restrict the dynamic range of the modulator. PMOS devices are used for the differential input in order to comply with the low common-mode voltage used in this design and also because of their lower flicker noise coefficient than nMOS transistors [17]. Based on the simulations, the input-referred noise (including both thermal and flicker noises) power of the first opamp is $41.6e-12$ V^2, 103.8 dB below the full scale input signal power. In contrast to MASH structure where high gain opamps result in two-stage or gain-boosted topologies with increased power dissipation, in SMASH architecture a single-stage opamp with no additional gain boosting technique allows low-power low-voltage operation and results in a simple design. A fast continuous-time common-mode feedback (CMFB) circuit shown in Fig. 12 is used to set the output common-mode voltage of the opamps to the desired value. The CT CMFB is designed to be faster than the main OTA. The value of R is chosen to be 20 kΩ in order not to limit the output impedance of the amplifiers.

Figure 13(a) shows the bias circuit [19] for the folded-cascode opamps. This circuit forces the g_m's of transistors in the bias circuit to depend only on geometric ratios and R_{ext}. Therefore, the g_m of transistors in the opamp is insensitive to the temperature and process variations. A start-up circuit shown in Fig. 13(b) is needed to avoid the stable zero-current state of the bias circuit. As the transistors M_{s1} and M_{s2} in start-up circuit are always on, their dimensions are chosen to be very small.

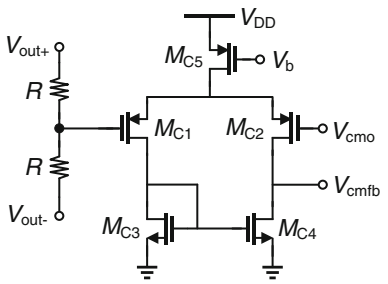


Fig. 12 CT CMFB circuit

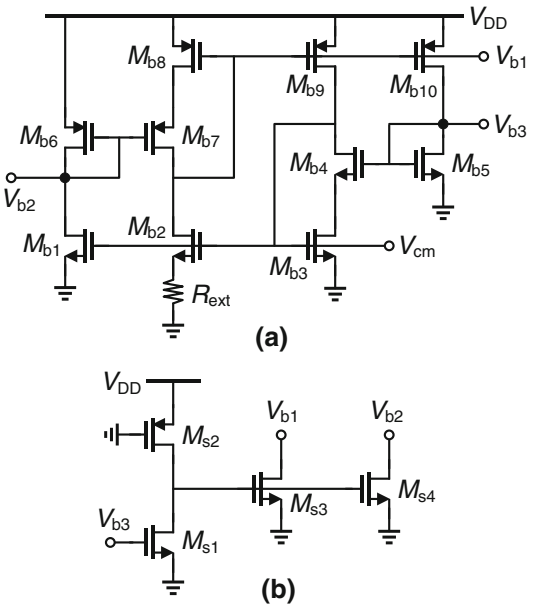


Fig. 13 **a** Bias circuit and **b** start-up circuit [19]

4.1.4 Feedback current DAC and calibration

The first-stage DAC is implemented by a current-steering DAC for its high-speed potential operation. All the current source transistors are cascoded to increase the output impedance. Current switch transistors are always operate in saturation region to provide an additional level of cascoding to further improve the output impedance.

Even though this DAC has a 3-bit resolution, but, its linearity must exceed the overall modulator's accuracy. The linearity requirement of current DACs is as tight as first active-RC integrator. Any nonlinearity of DAC will introduce to the distortion or raise the noise floor of the entire modulator. Usually two techniques can be employed to enhance the linearity of DACs: self-calibrated current-steering technique (SCCS) [20] and data weighted averaging (DWA) algorithm [21]. The DWA circuit increases the ELD in CT modulators. When the sampling rate is high, this phenomenon is very apparent. Another disadvantage of DWA circuit is its complexity, compared with easy implementation of SCCS algorithm. So, the SCCS technique is very suitable for low OSR and wideband CT modulators. An extra spare current source is needed in this method, not to interrupt the operation of the DAC. All the current sources, including the spare one, are calibrated one by one continuously and periodically by the same reference current source.

Besides the current calibration, there are several design issues involved in current-steering DAC and all of them need to be carefully studied and addressed in order not to adversely affect the DAC performance. One of them is the glitch at source node of M_3 and M_4 in the DAC switching transistors (Fig. 14(a)). If for a period of time both M_3 and M_4 are turned off, their source node will drop significantly and then rise back to its normal value when one of the switches is turned on. This glitch can cause long settling times of the output current. The delay and the shape deviation from its idealities in the output current will change the transfer function of the DAC. As a consequence, the modulator performance may be degraded. To prevent clock feedthrough and charge injection through switch transistors, high-crossing low-swing switch drivers are used to drive the current switches. To generate high-crossing, low-swing digital signals, a full-pMOS driver is used as shown in Fig. 14(b). The high level and low level of the output signals, 0.9 and 0.3 V, respectively, are carefully chosen to make sure that the switches can be fully turned on/off with sufficiently low unwanted clock feedthrough and charge injection.

4.1.5 3-Bit flash quantizer with passive adder

The 3-bit flash quantizer used in the first-stage modulator consists of a resistor-based reference ladder and eight clocked comparators. Each clocked comparator is composed of a preamplifier, a regenerative latch and an SR latch. In order to speed up the comparator circuit, latches with two regenerative branches [22] are used (Fig. 15). The dynamic operation of this circuit is divided into the reset and comparison intervals. At the reset interval, ϕ_L is low, transistors M_5 and M_6 are "off" and p-channel precharge transistors M_9 and M_{10} are "on". Therefore, both the p-channel flip-flop nodes, formed by M_7 and M_8, are charged up to the power supply voltage level, and n-channel flip-flop nodes, formed by M_3 and M_4, are discharged to the ground level through n-channel input transistors. When ϕ_L goes high, charging current starts to flow

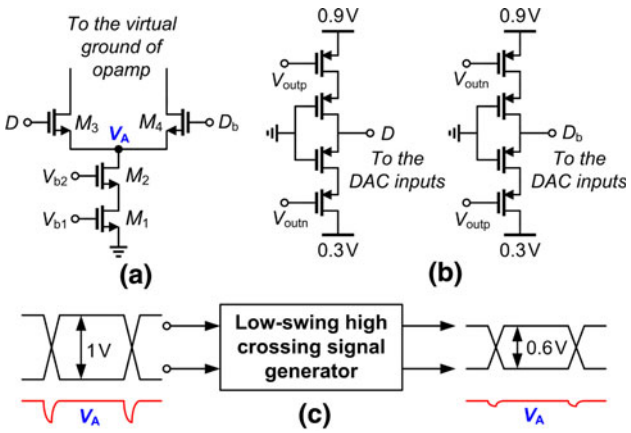


Fig. 14 **a** Current-steering DAC cell, **b** full-pMOS driver, and **c** high crossing low-swing signal generator

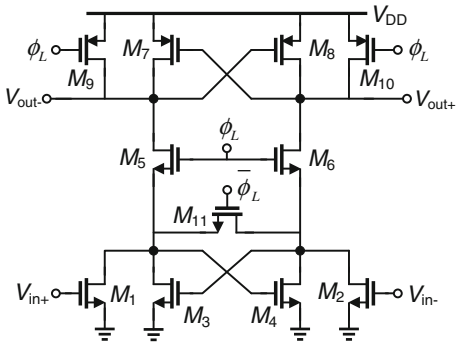


Fig. 15 Latch circuit used in the comparators [22]

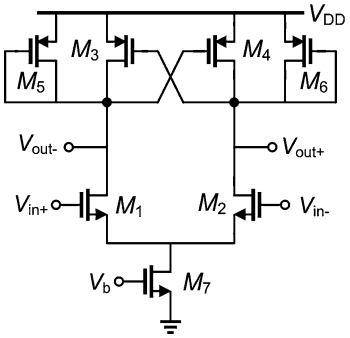


Fig. 16 Preamplifier circuit

from the p-channel side to the n-channel flip-flop and the latching mode is started. Since the output of the latch maintains the final voltage less than half of the clock period, an SR latch is used to convert it to the rail-to-rail value and then sustain for the full clock period.

Figure 16 shows the low-voltage preamp used in this design. A simple topology that does not need any CMFB circuit is chosen for this purpose. The main design considerations of the preamplifiers are: (1) sufficient gain to attenuate the latch offset when it is referred to the input of the comparator, (2) large bandwidth during the amplification phase avoiding any significant delay or attenuation on the main input signal and (3) offset storage and cancellation scheme to meet the offset requirement of the comparator. A switched capacitor summer shown in Fig. 17 is used in front of each preamplifier to add the input signal and output of CT integrators. It is critically to reset the preamplifier in order to minimize the memory effects [23]. To eliminate this effect, the preamplifier is reset in every clock period. The network of three sampling capacitors used in this adder performs two functions. Firstly, it adds the signal $V_{in} + V_{out2} + 1.5V_{out1} - V_{Ri}$ passively and, secondly, the input sampling capacitors are used to store the preamp offset during the reset phase, ϕ_2, and to subsequently cancel it during the amplification phase, ϕ_1.

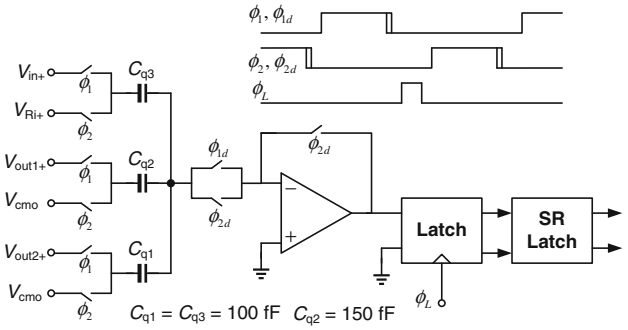


Fig. 17 Passive adder and comparator circuit used in the first-stage modulator (shown as single-ended for simplicity)

4.2 Second stage implementation

The third and fourth integrators are realized in a form of delaying and delay-free integrators, respectively. The third integrator shown in Fig. 18 uses the double-sampling technique. This DT integrator works with sampling frequency of 100 MHz, but as the result of using the double-sampling technique, the effective sampling rate is 200 MHz. Output signals of the third integrator are fed into the inputs of the fourth integrator. Also outputs of the fourth integrator is fed back to the third one in order to put the in-band zeros at the optimal places. The fourth integrator also uses the double-sampling technique with 100 MHz sampling clocks (Fig. 19). Folded-cascode opamps are also used in these integrators. Since the thermal noise of the DT second stage modulator does not restrict the dynamic range of the modulator and to minimize the load on the amplifiers, small size capacitors are used. ϕ_{12}

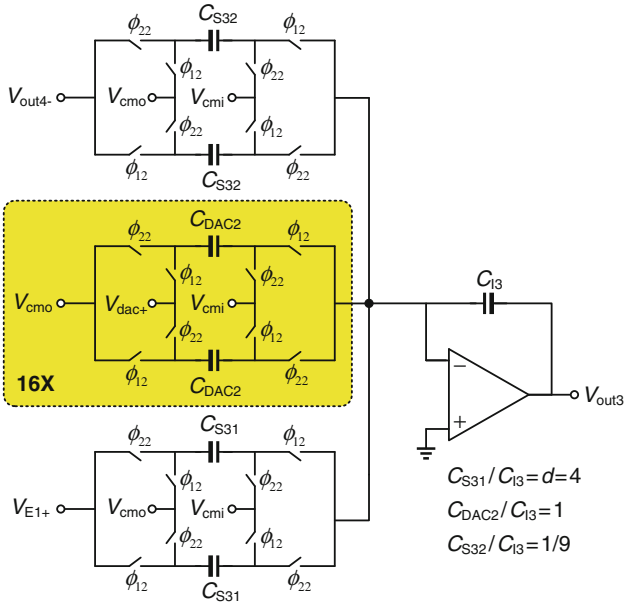


Fig. 18 DT third integrator (shown as single-ended for simplicity)

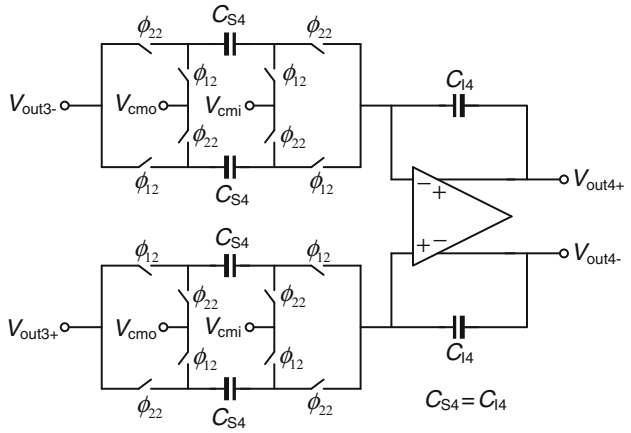


Fig. 19 DT fourth integrator

and ϕ_{22} are two non-overlapping clock phases with 100 MHz frequency.

Since no active adder was used in the front of the first-stage quantizer, the first stage quantization error extraction is done at the input of the second loop using the output of the first-stage quantizer, input signal and the output of first-stage integrators. A conceptual block diagram is depicted in Fig. 20. Shown in Fig. 18, the signal V_{E1} is the quantization noise of the first-stage modulator and it is extracted as shown in Fig. 20. As the result of handling a unity STF in the second-stage modulator, an active adder is required in order to realize the adder of the second-stage in Fig. 20. A simple implementation for this adder is adopted (see Fig. 21). This adder works with a sampling frequency of 100 MHz. As the output of integrators in the double-sampling technique are valid in both phases, two active adders with the opposite phases are used in this design. In this figure, only one path can be seen from the input of the adder to its output, but, in the actual implementation,

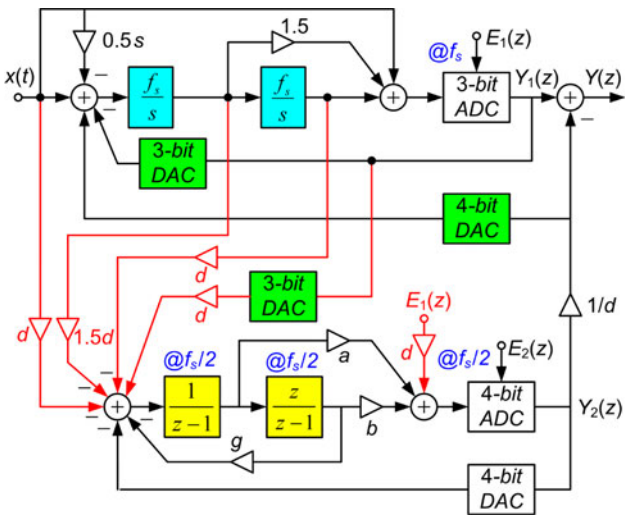


Fig. 20 First-stage quantization noise extraction

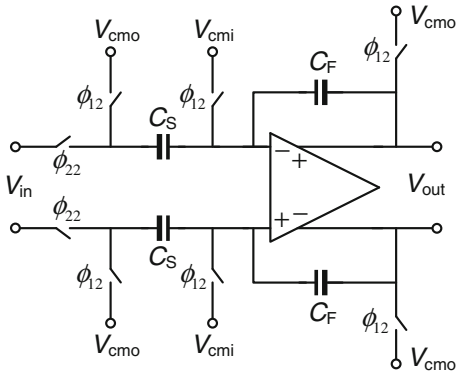


Fig. 21 Active adder used in the second-stage modulator

different paths are used. The different feedforward gains are realized with different capacitor ratios. The fourth integrator opamp is also used in the active adder circuit. Outputs of this adder are fed to the second-stage quantizer. The same latches as the first-stage are used in the second-stage quantizer.

It is worth mentioning that the mismatch between the passive adder in the first-stage modulator and the active adder used in the second-stage modulator can degrade the overall SNDR. If this mismatch is denoted by ε, then the first-stage quantization noise is firstly attenuated by $(1-\varepsilon)$ and then leaks to the output after experiencing the first-stage modulator noise-shaping effect. In this regard, the SMASH modulator is similar to the conventional MASH one. Nonetheless, this issue is not more important in this design, since the targeted resolution is not so high and a moderate matching will be sufficient to achieve more than 13 bit accuracy.

5 Simulation results

In order to verify the validity of the proposed design, HSPICE simulation results are provided. For calculating the parameter SNDR, 32768-points FFT is used with a Hann window [6]. The output spectrum plot for −8 dBFS, 122.0703125 kHz input signal is shown in Fig. 22. Note

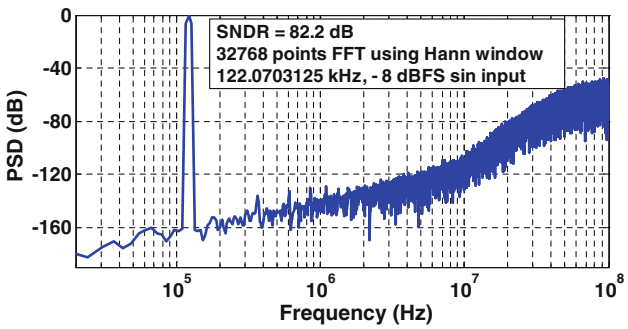


Fig. 22 Output spectrum excluding the circuit noise (TT at 27°C)

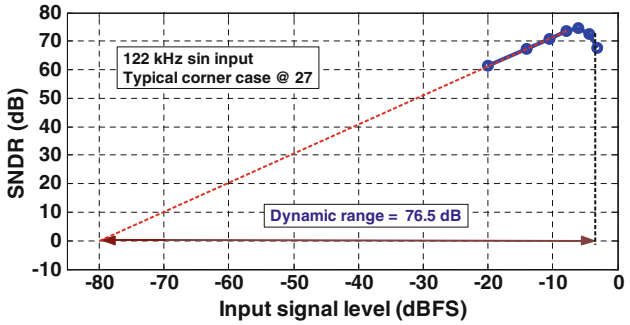


Fig. 23 SNDR versus input signal level

Table 1 Simulated performance summary (−8 dBFS sinusoidal input)

Parameter	TT at 27°C	FF at −40°C	SS at 85°C
SNDR (dB)	73.8	74.2	71.9
Power consumption (mW)	17	15.3	19.4
Power supply voltage	1 V		
OSR	8		
Input signal bandwidth	12.5 MHz		

Table 2 Noise contribution of modulator's building blocks (TT at 27°C, input signal power = −11 dBV)

First-stage integrating resistor	3.73×10^{-10} V^2	−94.3 dBV
Opamp noise	4.16×10^{-11} V^2	−103.8 dBV
First stage DAC	1.99×10^{-9} V^2	−87.0 dBV
DAC from the second-stage to the first-stage input	4.98×10^{-10} V^2	−93.0 dBV
Quantization noise + distortion	4.82×10^{-10} V^2	−93.2 dBV

that in the HSPICE simulations, only the quantization noise is considered. The SNDR versus the input signal power level is plotted in Fig. 23 for seven different values. In this plot, the thermal noise of all modulator building blocks are also considered. The achieved dynamic range is around 76.5 dB (12.4 effective number of bits). The overall performance of the simulated modulator is summarized in Table 1 for three different process/temperature corners. The modulator achieves a peak 74.8 dB SNDR over 12.5 MHz signal bandwidth with an OSR of 8. It dissipates 17 mW power from a 1 V supply. The noise contribution of all building blocks are summarized in Table 2 for typical corner case at room temperature.

To evaluate the performance of the proposed modulator in the context of several state-of-the-art wideband (>7.5 MHz) modulators, the following figure of merit (*FoM*) is employed:

$$FoM = Power/(2 \times BW \times 2^{ENOB}) \quad (15)$$

It takes the relation of overall power consumption over modulator resolution and input signal bandwidth. The smaller the FoM value is, the better the overall performance is. Table 3 lists the performance of several recently published wideband ΣΔ modulators. As is seen, this work is among the best published ones to date. It should be noted that although the reported results for the presented sigma–delta modulator are based on HSPICE simulation results while most of the other modulators are implemented on chip, but, its outstanding FoM verifies its performance as a good candidate for broadband and low-voltage applications and it is also expected a better FoM to be achieved from the measurement results.

6 Conclusions

A new hybrid CT/DT SMASH ΣΔ modulator was proposed. The double-sampling technique was employed in the second-stage which is a DT modulator. Since the double-sampling scheme was utilized in the second-stage,

Table 3 Performance comparison

References	CMOS process/ supply	Modulator resolution (bit)	BW (MHz)	Power (mW)	FoM (pJ/conversion)
[24]	0.18 μm/1.8 V	11.7	10	7.5	0.11
[25][a]	0.13 μm/1.5 V	10.8	15	70	1.31
[26][a]	0.25 μm/2.5 V	10.3	20	32	0.63
[27][a]	0.18 μm/1.8 V	8.8	20	18	0.87
[28]	0.09 μm/1 V	12.2	25	16.4	0.069
[29][a]	0.18 μm/1.8 V	11.1	23	42.6	0.41
[30][a]	0.11 μm/1.1 V	10.1	10	5.32	0.24
[31][a]	0.18 μm/1.8 V	11	25	48	0.47
[32]	0.18 μm/1.8 V	12.9	10	35.5	0.235
This work	0.09 μm/1 V	12.4	12.5	17	0.124

[a] Measurement results

the proposed modulator has much less sensitivity to the sampling paths mismatch of double-sampled SC circuits. The output swing requirement of the integrators was relaxed by employing a flat STF in the first-stage and a unity STF in the second-stage modulators without any sacrificing the inherent anti-aliasing behavior of the first-stage CT modulator. As a design example, a wideband modulator is designed in a 90 nm CMOS technology. It achieves 76.5 dB dynamic range and 74.8 dB maximum SNDR with a signal bandwidth of 12.5 MHz while operating at 200 MHz sampling rate and consuming 17 mW power from a single 1 V supply.

References

1. Northworthy, S., Schreier, R., & Temes, G. C. (Eds.). (1997). *Delta–sigma data converters*. Piscataway, NJ: IEEE Press.
2. Ortmanns, M., & Gerfers, F. (2005). *Continuous-time sigma–delta A/D conversion*. Berlin: Springer.
3. Kulchycki, S. D., Trofin, R., Vleugels, K., & Wooley, B. A. (2008). A 77-dB dynamic range, 7.5-MHz hybrid continuous-time/discrete-time cascaded ΣΔ modulator. *IEEE Journal of Solid-State Circuits, 43*(4), 796–804.
4. Nguyen, K., Adams, R., Sweetland, K., & Chen, H. (2005). A 106-dB SNR hybrid oversampling analog-to-digital converter for digital audio. *IEEE Journal of Solid-State Circuits, 40*(12), 2408–2415.
5. Hurst, P. J., & McIntyre, W. J. (1990). Double-sampling in switched-capacitor delta–sigma A/D converters. In *IEEE international symposium on circuits and systems (ISCAS)*, May 1990 (pp. 902–905).
6. Schreier, R., & Temes, G. C. (2005). *Understanding delta–sigma data converter*. Piscataway, NJ: IEEE Press/Wiley.
7. Maghari, N., Kwon, S., Temes, G. C., & Moon, U.-K. (2006). Sturdy MASH Δ-Σ modulator. *Electronics Letters, 42*(22), 1269–1270.
8. Maghari, N., Kwon, S., & Moon, U.-K. (2009). 74 dB SNDR multi-loop sturdy-MASH delta–sigma modulator using 35 dB open-loop opamp gain. *IEEE Journal of Solid-State Circuits, 44*(8), 2212–2221.
9. Maeyer, J., Raman, J., Rombouts, P., & Weyten, L. (2005). Controlled behavior of STF in CT ΣΔ modulators. *Electronics Letters, 41*(16), 19–20.
10. Silva, J., Moon, U.-K., Steensgaard, J., & Temes, G. C. (2001). Wideband low-distortion delta–sigma ADC topology. *Electronics Letters, 37*(12), 737–738.
11. Ortmanns, M., Gerfers, F., & Manoli, Y. (2005). A continuous-time ΣΔ modulator with reduced sensitivity to clock jitter through SCR feedback. *IEEE Transactions on Circuits and Systems-I: Regular Papers, 52*(5), 875–884.
12. Morgado, A., del Rio, R., & de la Rosa, J. M. (2007). Novel topologies of cascade ΣΔ modulators for low-voltage wideband applications. In *European conference on circuit theory and design (ECCTD)*, Aug. 2007 (pp. 136–139).
13. Ortmanns, M., Gerfers, F., & Manoli, Y. (2004). Compensation of finite gain-bandwidth induced errors in continuous-time sigma–delta modulators. *IEEE Transactions on Circuits and Systems-I: Regular Papers, 51*(6), 1088–1099.
14. Rombouts, P., Raman, J., & Weyten, L. (2003). An approach to tackle quantization noise folding in double-sampling ΣΔ modulation A/D converters. *IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing, 50*(4), 157–163.
15. Cherry, J. A., & Snelgrove, W. M. (1999). *Continuous-time delta–sigma modulators for high-speed A/D conversion*. Dordrecht: Kluwer.
16. Xia, B., Yan, S., & Sanchez-Sinencio, E. (2004). An RC time constant auto-tuning structure for high linearity continuous-time ΣΔ modulators and active filters. *IEEE Transactions on Circuits and Systems-I: Regular Papers, 51*(11), 2179–2188.
17. Razavi, B. (2001). *Design of analog CMOS integrated circuits*. London: McGraw Hill.
18. Li, Z. (2006, June). *Design of a 14-bit continuous-time delta–sigma A/D modulator with 2.5 MHz signal bandwidth*. Ph.D. Dissertation, Oregon State University.
19. Nam, K.-Y. (2005, June). *Design of low-voltage low-power sigma–delta modulators for broadband high-resolution A/D conversion*. Ph.D. Dissertation, Stanford University.
20. Groeneveld, D. W. J., Schouwenaars, H. J., Termeer, H. A. H., & Bastiaansen, C. A. A. (1989). A self-calibration technique for monolithic high resolution D/A converters. *IEEE Journal of Solid-State Circuits, 24*(6), 1517–1522.
21. Baird, R., & Fiez, T. (1995). Linearity enhancement of multibit ΣΔ A/D and D/A converters using data weighted averaging. *IEEE Transactions on Circuits and Systems-II, 42*(12), 735–763.
22. Yukawa, A. (1985). A CMOS 8-bit high-speed A/D converter IC. *IEEE Journal of Solid-State Circuits, 20*(3), 775–779.
23. Sandner, C., Clara, M., Santner, A., Hartig, T., & Kuttner, F. (2005). A 6-bit 1.2-GS/s low-power flash-ADC in 0.13-μm digital CMOS. *IEEE Journal of Solid-State Circuits, 40*(7), 1499–1505.
24. Schoofs, R., Steyaert, M., & Sansen, W. M. (2007). A design-optimized continuous-time delta–sigma ADC for WLAN applications. *IEEE Transactions on Circuits and Systems-I: Regular Papers, 54*(1), 209–217.
25. Paton, S., Di Giandomenico, A., Hernandez, L., Wiesbauer, A., Potscher, T., & Clara, M. (2004). A 70-mW 300-MHz CMOS continuous-time ΣΔ ADC with 15-MHz bandwidth and 11-bits of resolution. *IEEE Journal of Solid-State Circuits, 39*(7), 1056–1063.
26. Arias, J., Kiss, P., Prodanov, V., Boccuzzi, V., Banu, M., Bisbal, D., et al. (2006). A 32-mW 320-MHz continuous-time complex delta–sigma ADC for multimode wireless-LAN receivers. *IEEE Journal of Solid-State Circuits, 41*(2), 339–351.
27. Chen, X., Wang, Y., & Temes, G. C. (2007). A 18mW CT ΔΣ modulator with 25 MHz bandwidth for next generation wireless applications. In *IEEE custom integrated circuits conference (CICC)*, Sept. 2007 (pp. 73–76).
28. Chen, F., Kuendiger, T., Erfani, S., & Ahmadi, M. (2008). Design of wideband low-power continuous-time ΣΔ modulator in 90 nm CMOS technology. *Journal of Analog Integrated Circuits and Signal Processing, 54*(3), 187–199.
29. Yaghini, N., & Johns, D. (2005, Feb). A 43mW CT complex delta sigma ADC with 23 MHz of signal bandwidth and 68.8 dB SNDR. ISSCC Digest Tech. Papers, pp. 502–503.
30. Matsukawa, K., Mitani, Y., Takayama, M., Obata, K., Dosho, S., & Matsuzawa, A. (2010). A fifth-order continuous-time delta–sigma modulator with single-opamp resonator. *IEEE Journal of Solid-State Circuits, 45*(4), 697–706.
31. Lu, Ch., Onabajo, M., Gadde, V., Lo, Y., Chen, H., Periasamy, V., et al. (2010). A 25 MHz bandwidth 5th-order continuous-time

low-pass sigma–delta modulator with 67.7 dB SNDR using time-domain quantization and feedback. *IEEE Journal of Solid-State Circuits, 45*(9), 1795–1808.
32. Chiueh, H. H., et al. (2010). A 36-mW 320-MHz CMOS continuous-time sigma–delta modulator with 10-MHz bandwidth and 12-bit resolution. In *IEEE Midwest symposium on circuits and systems (MWSCAS)*, Aug. 2010 (pp. 725–728).

Mohammad Hossein Maghami received the B.Sc. degree from the Ferdowsi University of Mashhad, Iran, in 2006, and the M.Sc. degree from the Amirkabir University of Technology, Iran, in 2009. Currently, he is working towards Ph.D. degree in Electrical Engineering at the K.N. Toosi University of Technology, Iran. His main areas of interests are high-speed low-power A/D converters, implantable biomedical microsystems and mixed-mode integrated circuits.

Mohammad Yavari received the B.Sc., M.Sc., and Ph.D. degrees in electrical engineering from the University of Tehran, Tehran, Iran, in 1999, 2001, and 2006, respectively. He has been an assistant professor at the Department of Electrical Engineering, Amirkabir University of Technology (AUT), Tehran, Iran, since Sept. 2006 where he founded the Integrated Circuits Design Laboratory in 2007. He spent several research periods at the Institute of Microelectronics of Seville (IMSE-CNM), Seville, Spain. He was with Niktek from May 2004 to April 2005 and Oct. 2006 to May 2007 as a principal design engineer where he was involved in the design of high-resolution A/D and D/A converters for professional digital audio applications. His research interests include analog and mixed-mode integrated circuits and signal processing, data converters, and CMOS RFIC design for wireless communications. He is the author or co-author of more than 80 peer-reviewed papers in international and national journals and conference proceedings on analog integrated circuits. He received the best student research award of the University of Tehran in 2004.