Digital Calibration of Elements Mismatch in Multirate Predictive SAR ADCs

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***Abstract*— This paper presents a multirate predictive successive approximation register (SAR) analog-to-digital converter (ADC). The main objective is to introduce digital frameworks for resolving the weaknesses of the previous predictive schemes in the context of the SAR ADC. The proposed SAR ADC compensates for the capacitive element mismatches, extends the input signal frequency using an adaptive digital predictive machine (ADPM), and relaxes the speed requirement through multirate implementation of the ADPM. As a consequence, the achievable sampling-rate can also be improved by optimizing the capacitors according to the thermal noise requirement. Behavioral simulation results, based on the Monte Carlo method, are provided for a 12-bit SAR ADC to verify the usefulness of the proposed approach. The simulation results indicate that the means of the spurious-free dynamic range (SFDR) and the signal-to-noise and distortion ratio (SNDR) are 82.3 and 69.1 dB, respectively.**

***Index Terms*— Analog-to-digital conversion (ADC), successive approximation register (SAR) ADCs, adaptive systems, prediction, multirate systems, charge redistribution digital-to-analog conversion (CR-DAC), elements mismatch.**

I. Introduction

SUCCESSIVE approximation register (SAR) analog-to-digital converters (ADCs) are known for their power efficiency and simple architecture, and they also benefit from the scaling of advanced CMOS technologies [1]–[8]. Nonetheless, such ADCs are inherently slow due to the required successive conversion steps [1]–[3]. Charge redistribution digital-to-analog converters (CR-DACs) construct the main block of SAR ADCs. Mismatches among the capacitive elements in the CR-DAC directly degrade the accuracy of the SAR ADC. Consequently, in practice, the resolution of such ADCs is limited to about 10 to 12 bits.

Various methods have been proposed to enhance the speed and resolution of SAR ADCs. The sampling-rate of the SAR ADC can be increased through time-interleaving approach [3], [5], [8]–[13]. However, the resolution degradation owing to the offset and timing mismatch among SAR ADCs must be regarded and alleviated [5], [14]–[16]. Furthermore, the subranged structure can reduce the required successive conversion steps to improve the speed of the SAR ADC [12], [17], [18]. Nevertheless, the timing mismatch among the required flash ADC and the elements of the CR-DAC is a limiting factor that needs to be considered and mitigated [19]. The multi-bit per cycle method considerably reduces the required conversion steps in SAR ADCs [6], [20]. However, it substantially increases the analog complexity, and the offset mismatch between comparators also degrades the overall resolution [19]. Additionally, when resolutions of beyond 10 bits are sought, the mismatch among the elements of the CR-DAC must be taken into account and compensated for. Therefore, the size of the CR-DAC elements needs to be scaled up to achieve the desired accuracy at the expense of (considerable) increase in the power dissipation and silicon area. In contrast, the mismatch can be compensated in the digital domain (or it can be alternatively corrected in analog domain) through calibration mechanisms without the need for scaling up the capacitive elements [7], [19], [21], [22].

Scaling of CMOS technologies has helped modern integrated circuits to consume less power and silicon area, and/or to operate at higher frequencies. Digital mechanisms to enhance the performance of the ADCs can thus benefit from the technology scaling [5], [7], [12], [15], [16], [19], [21]–[25]. Among these schemes, digital-prediction-based approaches alleviate the resolution and speed requirements of the analog-to-digital conversion inside the ADCs via a digital prediction machine (DPM) [26]–[32]. In such methods, the digital output of the predictive ADC is digitally estimated by the DPM, and the prediction error is digitized by an ADC; however, the digital implementation of the DPM can limit the operation frequency of the predictive ADCs. Furthermore, the mismatch among the elements of the required capacitive array needs to be considered and compensated for. The existing predictive ADCs employ dynamic element matching (DEM) algorithms for the mismatch compensation, however, such techniques often bound the input signal to low frequencies. Due to advantages of SAR ADCs and alleviation of the need for additional amplifier, the subranged SAR ADC structure is modified to be used as the predictive SAR ADC [27], [28], [31]. In the

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predictive SAR ADCs, the flash ADC is replaced by a DPM; as a key consequence, the adverse effects associated with timing mismatches are eliminated as well.

This paper introduces a multirate predictive SAR ADC to address the shortcomings of the current predictive ADCs. The proposed predictive SAR ADC mitigates the restriction on the input signal frequency through an adaptive digital prediction machine (ADPM). Besides, the resolution of this ADC is enhanced by the digital compensation of the mismatches in the elements of the CR-DAC. Moreover, the presented SAR ADC also relaxes the speed requirements of the ADPM via utilizing a multirate implementation. Due to the digital mismatch calibration, the equivalent sampling capacitor in the SAR ADC can be chosen based on the thermal noise requirements, and thus, the power dissipation of the SAR ADC is reduced. Additionally, similar to [27], [28], [31], the presented SAR ADC alleviates the need for a flash ADC as compared to the subranged mechanism [12], [17], [18], and furthermore, in contrast to [26], [29], [30], [32], the proposed technique does not require a power hungry amplifier. Also, restrictions on the frequency of the input signal imposed by the proposed SAR ADC are not as limiting as those in [26]–[29], [31], [32]. Finally, the proposed architecture for the SAR ADC is not susceptible to the offset of the comparator.

The remainder of the paper is structured as follows. Section II briefly overviews predictive SAR ADCs and their operation concepts. Section III introduces the proposed predictive SAR ADC. Simulation results and discussions are provided in Section IV. Finally, Section V concludes the paper.

II. Predictive SAR ADCs

Traditional ADCs are based on the assumption that the input signal is a random noise with white spectrum [31]. However, in the prediction-based ADCs the input signal is supposed to be *band-limited* [28], [31], [32]. In predictive ADCs, the current sample of the digital output, D_{out}, is estimated from the past samples of the digital output *as long as* the present sample of the digital output exhibits correlation with the previous samples (i.e., band-limited) [33], [34]. As a consequence, the DPM is comprised of a finite impulse response (FIR) filter. The predicted digital output is calculated as:

$$D_{pre}(n) = \sum_{i=1}^{M} F_i \cdot D_{out}(n-i+1) \tag{1}$$

where, n represents the discrete-time index, and F_i and M denote the i^{th} coefficient and the length of the FIR filter, respectively [35], [36]. The coefficients of the FIR filter are determined according to the required bandwidth and frequency by solving the following Yule–Walker equations [33]:

$$\boldsymbol{f} = \boldsymbol{R}^{-1}\boldsymbol{r} \tag{2}$$

where $\boldsymbol{f}$, $\boldsymbol{R}$, and $\boldsymbol{r}$ denote the vector of the M coefficients, the input correlation matrix, and the input correlation vector, respectively, defined as

$$\boldsymbol{f} = \begin{bmatrix} F_1 \\ \vdots \\ F_M \end{bmatrix}, \quad \boldsymbol{R} = \begin{bmatrix} r(0) & \cdots & r(M-1) \\ \vdots & \ddots & \vdots \\ r(M-1) & \cdots & r(0) \end{bmatrix}, \quad \boldsymbol{r} = \begin{bmatrix} r(1) \\ \vdots \\ r(M) \end{bmatrix}$$

where $r(\cdot)$ denotes the input autocorrelation sequence [33], [34]. Consequently, the value of the coefficients $F_i, i = 1, \ldots, M$, depends on the length M and also the amplitude, frequency, and bandwidth of the input signal.

It is worth mentioning that the predicted digital output, D_{pre}, would be estimated without any error *in case* the input signal is a *line spectral process*, consisting of a set of sine-waves [33]. Nevertheless, any other band-limited signal leads to an error in the prediction process. Therefore, the quality of the predicted digital output, D_{pre}, must be evaluated with respect to the desired digital output. As a result, the signal D_{pre} is converted to its analog equivalent, and the difference between the input signal, V_{in}, and the analog format of the predicted digital output is digitized to produce the prediction error, $D_{e,pre}$ [28], [31]. The prediction error is *inherently delayed* through the digitization process by one unit time in the discrete-time domain. It is thus evident that the sum of the delayed version of the predicted digital output and the prediction error represent the desired digital output as

$$D_{out}(n) = D_{pre}(n-1) + D_{e,pre}(n). \tag{3}$$

Moreover, as the length M increases, the prediction error approaches a *white process*, and its standard deviation also reduces [33]. Also, the minimum standard deviation of the prediction error is expressed as following

$$\sigma_{e,pre} = \sqrt{r(0) - \boldsymbol{r}^T \boldsymbol{R}^{-1}\boldsymbol{r}} \tag{4}$$

where the superscript T represents the transpose operator [33], [34]. This standard deviation depends on the input signal and the length M.

As stated earlier, the aim of the predictive SAR ADCs is to alleviate the need for any power hungry amplifier via adopting a subranged method [28], [31]. However, the flash ADC in the subranged structure is replaced by the DPM. Similar to the subranged SAR ADCs, the required number of steps for binary search algorithm (BSA) is consequently decreased since only the prediction error needs to be digitized. The typical architecture of an N-bit predictive SAR ADC is illustrated in Fig. 1 [27], [28], [31]. As seen from the figure, the predictive SAR ADC is comprised of a SAR logic, a CR-DAC, and a comparator in addition to the DPM. In an N-bit predictive SAR ADC, the signal D_{out} consists of the bits $\{B_{N-1}, \ldots, B_0\}$, and it is divided into the signal D_{pre}, comprised of K most significant bits (MSBs) $\{B_{N-1}, \ldots, B_{N-K}\}$, and the signal $D_{e,pre}$, encompassing the $N-K$ least significant bits (LSBs) $\{B_{N-K-1}, \ldots, B_0\}$. The DPM estimates the predicted digital output, D_{pre}, and the binary search algorithm (BSA) determines $D_{e,pre}$.

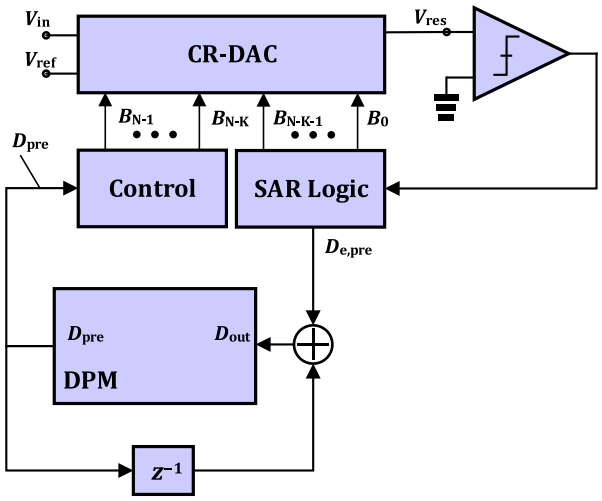

Fig. 1. Typical architecture of the conventional predictive SAR ADC.

The goal of the BSA is to successively control the switches according to the decision of the comparator in each conversion step such that the residue voltage successively approaches to 0. In this paper, it is assumed that all these bits are bipolar and have a value of $\{-1, 1\}$ rather than $\{0, 1\}$ for presentation clarification. The comparator decision in the i^{th} step determines the bit B_{N-K-i}. In the i^{th} step, bit B_{N-K-i} is equal to 1 if the residue voltage is greater than zero, and -1 otherwise. The analog switches, $S_{N-1}, \ldots, S_0$, are controlled by the bits, $B_{N-1}, \ldots, B_0$, respectively. The task of the analog switch is to connect the bottom plate of its corresponding capacitor to V_{ref} if its corresponding bit is -1 or to $-V_{ref}$ otherwise. The BSA requires, at least, K steps for an N-bit resolution.

It is worth mentioning that almost all current predictive ADCs use a DEM-based method to reduce the error due to the mismatches among the elements of the CR-DAC just in a specified frequency interval. Moreover, DEM methods often eliminate the error arising from mismatch in a range of low frequencies. For this certain range, the coefficients of the FIR filter are also set to fixed values according to the Yule-Walker equations. Consequently, the current predictive ADCs are not fully functional over the entire frequency range from 0 to half the Nyquist-rate. Finally, the DPM machine can restrict the maximum sampling-rate of current predictive ADCs. Thus, almost all currently available predictive ADCs have the following shortcomings:

1- They are not capable of removing errors arising from the mismatch among the elements of the CR-DAC over the entire frequency range from 0 to half the Nyquist-rate.
2- The input frequency is restricted to a specified frequency range (e.g., low frequencies).
3- The DPM algorithm can bound the overall speed of the system.

In the following section, an adaptive multirate predictive SAR ADC is proposed to overcome the above-mentioned limitations.

III. Adaptive Multirate Predictive SAR ADC and Digital Calibration of Element Mismatch

The goal of the proposed structure is to resolve the above-mentioned limitations. Although a differential structure is generally employed in practice, without loss of generality and for simplicity of presentation, the single-ended architecture is used here. Besides, all analog and digital signals are scaled to the reference voltage, V_{ref}, and the constant $2^N - 1$, respectively, where the integer N denotes the resolution of the ADC; therefore, all signals are bounded to $[-1, 1]$. The presented predictive SAR ADC exploits a bridged CR-DAC (BCR-DAC) [7], [22]. The BCR-DAC is comprised of two sections:

1) *Subtraction* array consisting of an array of capacitive elements, weighted from W_0C_u to $W_{N-1}C_u$,
2) *Error Extraction* array consisting of an array of capacitive elements, weighted from $LW_{-1}C_u$ to $LW_{K-1}C_u$,

where C_u represents the unit capacitor, L denotes the enlargement factor, and the capacitor weight W_i represents 2^i. It should be noted that a redundancy of 1-bit is exploited in the error extraction array; hence, this array has the extra element with the weight $LW_{-1}C_u$. The BCR-DAC allows the elements of the error extraction array to be enlarged by the factor of L. Thus, the elements mismatch in the error extraction array is mitigated by a factor of $L^{0.5}$. The analog switches of the subtraction section, $S_{N-1}, \ldots, S_0$, are controlled by the bits, $B_{N-1}, \ldots, B_0$. These bits construct the predicted digital output, D_{pre}. Moreover, the bits produced by the traditional BSA algorithm, $B_{e,K-1}, \ldots, B_{e,-1}$ adjust the analog switches in the error extraction array. These sections are also separated by the bridged capacitor, C_b.

In the sampling phase, all the capacitors of the BCR-DAC are placed in parallel. Accordingly, the equivalent capacitor is

$$C_S = C_{sub} + \frac{C_b \times (C_p + C_{ee})}{C_b + C_p + C_{ee}} \tag{5}$$

where, C_{sub} denotes the equivalent capacitance of the subtraction array, and also, C_{ee} and C_p represent the total and parasitic capacitance of the error extraction array, respectively. The parasitic capacitor C_p arises from the capacitors of the error extraction array and randomly varies between 10 to 30% of C_{ee} [7], [22], [37], [38]. The minimum value of the capacitor C_S is determined by the thermal noise requirements. At the end of the sampling phase, the input voltage, V_{in}, is sampled onto the array of capacitors. In the conversion phase, the charge at the residue voltage is preserved, and the charge of C_b is identical the charge on C_{ee}. Therefore, the residue voltage, V_{res}, can be expressed as [22]

$$V_{res} = V_{in} - \alpha \left\{ \sum_{i=0}^{N-1} B_i W_i + \gamma \sum_{i=-1}^{K-1} B_{e,i} W_i \right\} \tag{6}$$

where, the variables α and γ are defined as

$$\alpha = V_{ref} C_u / C_S, \tag{7}$$

$$\gamma = LC_b / (C_b + C_p + C_{ee}). \tag{8}$$

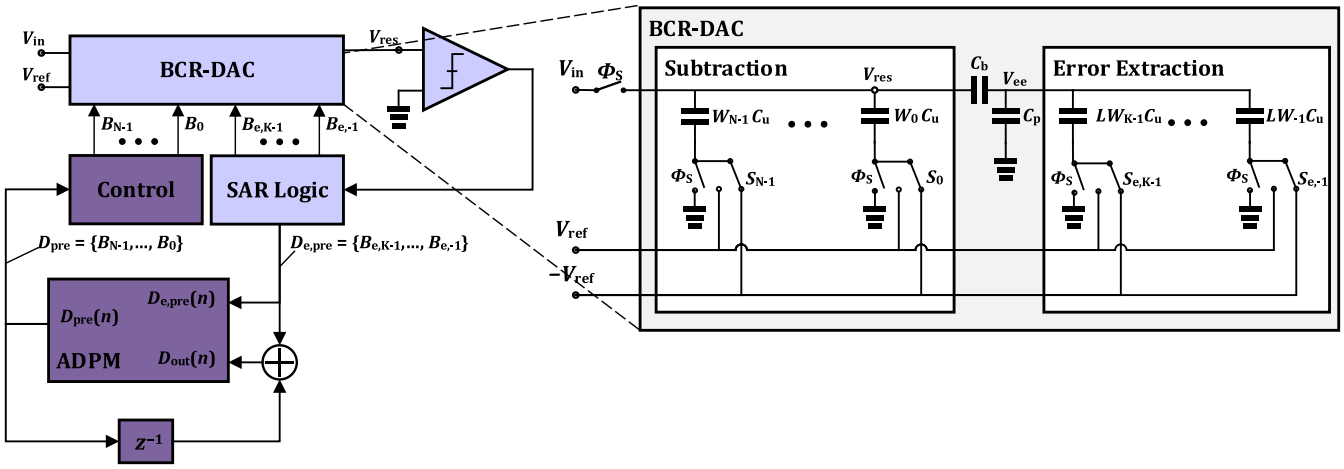

Fig. 2. Proposed SAR ADC.

For presentation simplicity, α is considered equal to $1/(2^N - 1)$. Besides, γ would ideally be equal to 1; consequently, the bridge capacitor must be set to

$$C_b = \left(C_p + C_{ee}\right)/(L-1). \tag{9}$$

In (9), the value of C_p is considered to be 20% of that of C_{ee}. As such, the random deviations of C_p from its nominal value lead to a 1% variation in γ. In this architecture, the ADPM firstly estimates the next value of the digital output, D_{pre}. Afterwards, the ADPM sets the switches, $S_{N-1}, \ldots, S_0$ in the first step of the conversion phase. Then, the BSA algorithm drives the residue voltage to zero by proper adjustment of the switches, $S_{e,K-1}, \ldots, S_{e,-1}$. Note that the required conversion steps for the N-bit SAR ADC are reduced from N to $K+1$. In (6), the bits B_i and $B_{e,i}$ are binary weighted by W_i; as a result, the input voltage can be expressed as a function of the digital signals, D_{pre} and $D_{e,pre}$ as follows

$$V_{in}(n) = D_{pre}(n) + \gamma\, D_{e,pre}(n) + V_{res}(n) \tag{10}$$

where,

$$D_{pre}(n) = \frac{1}{2^N - 1} \sum_{i=0}^{N-1} W_{d,i} B_i, \tag{11}$$

$$D_{e,pre}(n) = \frac{1}{2^N - 1} \sum_{i=-1}^{K-1} W_{e,i} B_{e,i}. \tag{12}$$

In (11) and (12), the digital weights $W_{d,i}$ and $W_{e,i}$ are equal to their corresponding analog weights W_i $(= 2^i)$. At the end of the binary search, the residue voltage, V_{res}, is ideally bounded to the range $[-V_{LSB}/2, V_{LSB}/2]$, where V_{LSB} is $V_{ref}/2^{N-1}$. It should be noted that the predicted digital output varies within the interval $[-1, 1]$, and the range of the prediction error is limited to $[-(2^K - 1)/(2^N - 1), (2^K - 1)/(2^N - 1)]$. The digital output is also expressed as

$$D_{out}(n) = D_{pre}(n-1) + D_{e,pre}(n). \tag{13}$$

Therefore, the signal $D_{out}(n)$ is the digital equivalent of the input voltage *provided that* the variable γ is 1.

A. Multirate Adaptive Digital Prediction Machine

The proposed ADPM is based on the multirate adaptive prediction concept [34], [36], [39], [40]. For this reason, it consists of a multirate block FIR filter. In the block FIR filter, the single-input single-output system is converted to an $R \times R$ matrix through down-sampling and up-sampling operations and a bank of FIR filters [34], [39], [40]. Moreover, the ADPM utilizes a multirate least mean square (M-LMS) approach to adaptively adjust the coefficients of the block FIR filter according to the bandwidth and frequency of the input signal during the normal operation of the predictive SAR ADC [34], [36]. Accordingly, the proposed architecture relaxes the speed requirement of the ADPM by a factor of R, and also, the input frequency can vary from 0 to half the Nyquist-rate.

In the block FIR filter, the input signal is decomposed to R down-sampled signals, $D_{o,1}, \ldots, D_{o,R}$. Then, these down-sampled signals are applied to the bank of 2^R FIR filters operating in parallel. For instance, $D_{o,1}$ is applied to $FIR_{11}, \ldots, FIR_{1R}$, and $D_{o,R}$ is applied to $FIR_{R1}, \ldots, FIR_{RR}$, respectively. The input-output transformations of the filters are expressed as

$$D_{pr,a,b}(m) = \sum_{i=1}^{M} F_{a,b,i} \cdot D_{o,a}(m - i + 1) \tag{14}$$

where, a and b are $1, \ldots, R$, and m denotes the discrete-time time index of the down-sampled signals. Then, the outputs of the bank of FIR filters are combined and up-sampled to create the output signal, D_{pre}. As an example, Fig. 3 shows the block FIR filter for $R = 2$.

Additionally, the coefficients of the block FIR filter, $F_{a,b,i}$, are adaptively tuned during the normal operation of the SAR ADC. Furthermore, for the estimation process to be optimal, the error signal (i.e., the residue voltage at the end of binary search) needs to be as close to zero as possible. Accordingly, a mechanism is needed to adjust the coefficients of the block FIR filter such that the prediction error signal is confined close to zero. The M-LMS algorithm has the capability of tuning the coefficients of the block FIR filter such that the *cost function*,

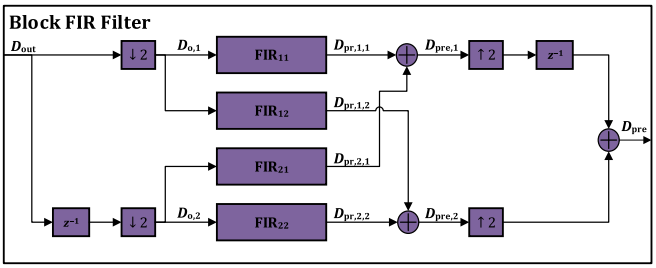

Fig. 3. Block FIR filter.

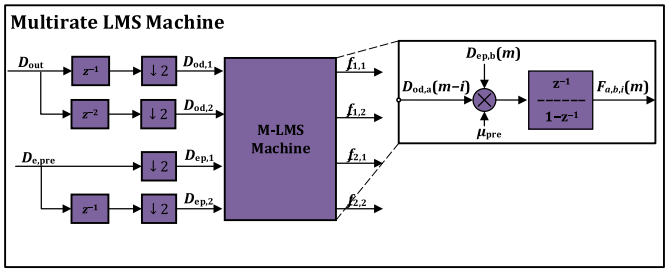

Fig. 4. M-LMS engine.

defined as

$$J_{pre}(n) = D_{e,pre}(n)^2/2, \tag{15}$$

approaches to its possible minimum [35], [36]. However, the prediction error signal, $D_{e,pre}$, must also be decomposed according to its respective decomposed signals $D_{pr,a,b}$ [41]. For this reason, the R down-sampled cost functions are defined as

$$J_{pre,b}(m) = D_{ep,b}(m)^2/2 \quad b = 1, \ldots, R. \tag{16}$$

The M-LMS algorithm drives the down-sampled cost functions to their minimums by suitably adjusting the coefficients $F_{i,a,b}$. The required input signals of the M-LMS algorithm are also decomposed to create the output signals, $D_{od,a}$, and error signals, $D_{ep,a}$. As an example, Fig. 4 illustrates the M-LMS machine for $R = 2$, where the vector $\underline{f}_{a,b}$ denotes the coefficients $\{F_{a,b,1}, \ldots, F_{a,b,M}\}$. The *update-steps* defined as

$$US_{pre,a,b,i}(m) = \partial J_{pre,b}(m)/\partial F_i(m), \tag{17}$$

where $i = 1, \ldots, M$, and a and b are $1, \ldots, R$, provide the direction to the minimum of the down-sampled cost functions. Thus, the minimum of the cost functions can be obtained successively by exploiting the update-steps, $US_{pre,i}(n)$. Consequently, discrete-time integrators are needed to find the minimums. The update-steps of the M-LMS algorithm are expressed as

$$US_{pre,a,b,i}(m) = D_{od,a}(m-i)\, D_{ep,b}(m). \tag{18}$$

The update expression of the M-LMS algorithm is given by

$$F_{a,b,i}(m+1) = F_{a,b,i}(m) + \mu_{pre} US_{pre,a,b,i}(m) \tag{19}$$

where, $i = 1, \ldots, M$, and a and b are $1, \ldots, R$, and μ_{pre} denotes the step-size of the M-LMS algorithm [15], [35], [36], [42]. The step-size, μ_{pre}, determines the size of each step toward the minimum and proper choice of it prevents the instability of the M-LMS algorithm. As this step-size reduces, the convergence rate of the M-LMS algorithm decreases as well. Therefore, it must be chosen such that it assures the stability of the M-LMS algorithm and the maximum possible convergence rate. For each coefficient, a replicated block of the M-LMS machine is employed. All the replicas operate simultaneously.

B. Digital Mismatch Calibration

The capacitors of the BCR-DAC are weighted corresponding to their bit weights in the digital output by the weights W_i; as a result, $W_i, i = 0, \ldots, N-1$, must be the same as $W_{d,i}$. In practice, the value of the capacitive elements manifest random deviations from their desired weights [7], [8], [13], [21], [22], [43]. In this case, the capacitance of the elements does not match with their corresponding digital weights. This leads to the mismatch error, which is nonlinearly related to the predicted digital output. The capacitor mismatch mainly limits the resolution of the ADC. For the compensation of the elements mismatch, the digital weights, $W_{d,i}, i = 0, \ldots, N-1$, need to be corrected in digital domain according to the weight of their equivalent elements, W_i, (or the capacitive elements must be alternatively tuned in analog domain) [13], [21].

For the clarity of the presentation, it is assumed that the ADPM has already converged. The deviations of the capacitors need to be considered and determined for the elements mismatch calibration. In fact, the capacitance of the BCR-DAC elements cannot be directly extracted. For this reason, almost all calibration mechanisms indirectly measure the effects of the elements mismatch. In the presence of the elements mismatch in the BCR-DAC, the residue voltage encompasses the error due to the elements mismatch in addition to the prediction error. In the predictive SAR ADC, the residue voltage exhibits the error resulted from the elements mismatch after the convergence of the ADPM. Therefore, the error signal, $D_{e,pre}$, can also be utilized to digitally measure the elements mismatch and to compensate for it in analog domain.

The objective of the presented mechanism is to generate the corrected signal, D_{cor}, from the predicted digital output by the digital mismatch correction (DMC) block such that D_{cor} is comprised of the digital version of the mismatch errors in addition to the predicted digital output. In the proposed calibration method, the DMC block, consists of the digital correction weights, $W_{c,i}, i = 0, \ldots, N-1$, to compensate for the elements mismatch. Ideally, the analog weights, $W_i, i = 0, \ldots, N-1$, would be $W_{c,i} + W_{d,i}$. The aim of the digital calibration is to satisfy this requirement. Afterwards, instead of the predicted digital output, this corrected signal is used to create the digital output as:

$$D_{out}(n) = D_{cor}(n-1) + D_{e,pre}(n). \tag{20}$$

Since the digital output (before the calibration) consists of the delayed version of the predicted digital output and the

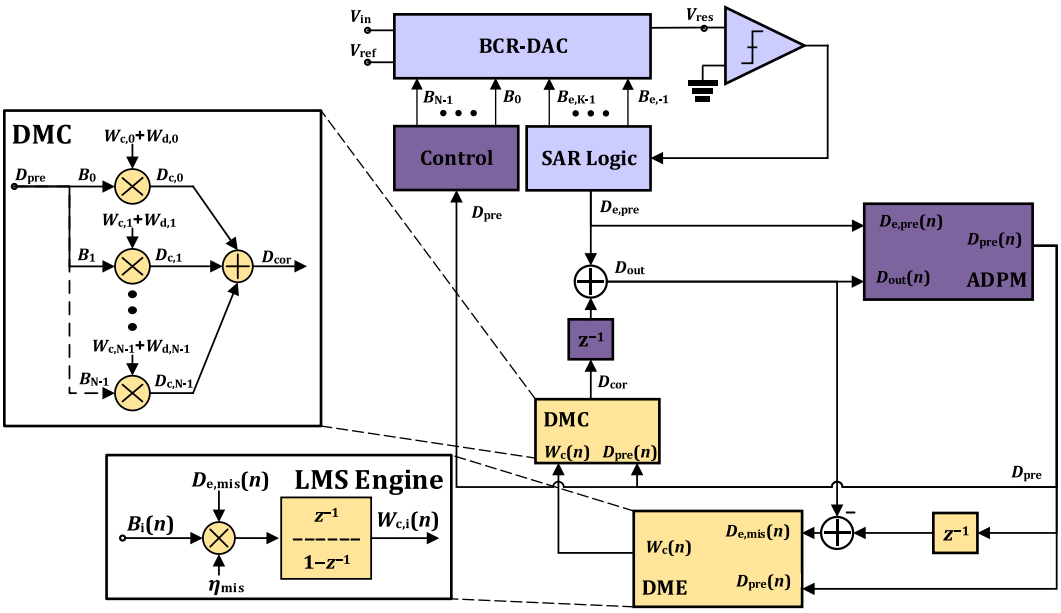

Fig. 5. Complete structure of the proposed predictive SAR ADC.

mismatch error signals, the difference between the delayed predicted digital output and the digital output would this result in the digital format of the error due to the elements mismatch. Therefore, the mismatch error can be calculated as:

$$D_{e,mis}(n) = D_{pre}(n-1) - D_{out}(n). \tag{21}$$

In the proposed calibration algorithm, the digital mismatch estimation (DME) section is used to minimize the mismatch error, $D_{e,mis}$, via an LMS machine. The LMS engine tunes the weights of the DMC block such that the mismatch error approaches its minimum. Depicted in Fig. 5 is the complete architecture of the proposed SAR ADC. The LMS algorithm repeatedly updates the cost function defined as

$$J_{mis}(n) = D_{e,mis}^2(n)/2. \tag{22}$$

The update-step of the LMS algorithm is given by

$$US_{mis,i}(n) = \partial J_{mis}(n)/\partial W_{c,i}, \quad i = 1, \ldots, N. \tag{23}$$

The update-step can be expressed as

$$US_{mis,i}(n) = B_i(n) D_{e,mis}(n), \quad i = 1, \ldots, N \tag{24}$$

where B_i stands for the i^{th} bit of the predicted signal. Finally, the update expression of the LMS algorithm is given by

$$W_{c,i}(n+1) = W_{c,i}(n) + \eta_{mis} US_{mis,i}(n), \quad i = 1, \ldots, N \tag{25}$$

where, η_{mis} denotes the step-size of the LMS algorithm similar to μ_{pre} [15], [42]. This step-size determines the size of each step toward the minimum and prevents the instability of the LMS algorithm. It should be noted that all the digital weights of the DMC block are updated simultaneously through the replicas of the LMS engine.

C. Complete Structure of the Presented SAR ADC

The ADPM and digital elements mismatch calibration sections operate simultaneously as shown in Fig. 5. Note that the error extraction section of the BCR-DAC has two main tasks:

1) Direct measurement and digitization of the error due to the prediction process.
2) Indirect extraction of the error due to the elements mismatch.

It is worth mentioning that the mismatch in the error extraction array can affect the digital calibration mechanism; accordingly, the bridge architecture is used to limit the elements mismatch in the error extraction array to below a specified level. This is achieved via expanding the elements by L. Although the elements mismatch is digitally compensated by the DMC, it can be corrected in analog domain through directly operating on the error signal, $D_{e,pre}$. Since the mismatch calibration engine utilizes the prediction mechanism of the ADPM to detect the elements mismatch of the BCR-DAC, the coefficients of the block FIR filter must be converged to their desired values such that the predicted digital output, D_{pre}, becomes ready to be used by the calibration engine. Consequently, similar to the mechanism in [44], the DME machine is enabled after the convergence of the ADPM. In this scheme, the mean of the absolute value of the prediction error signal over P samples is defined as

$$D_{e,mean}(w) = \sum_{n=Pw}^{P(w+1)-1} \left| D_{e,pre}(n) \right| \tag{26}$$

where $|\cdot|$ denotes the absolute value. The mean $D_{e,mean}$ is compared with a specified value. This value is regarded as half the maximum of $|D_{pre}|$, and P is chosen to be 2^{10}. It must be noted that the constants μ_{pre} and η_{mis} need to be selected such that the fluctuations of the coefficients of the block FIR filter and the digital weights be confined below a specific

TABLE I
THE VALUE OF THE PARAMETERS

	N	K	M	$\sigma_{\text{Mismatch}}(C_u)$*	μ_{pre}	η_{mis}
Value	12	6	8	10%	2^{-5}	2^{-10}

*$\sigma_{\text{Mismatch}}(C_u)$ denotes the standard deviation of the mismatch of C_u.

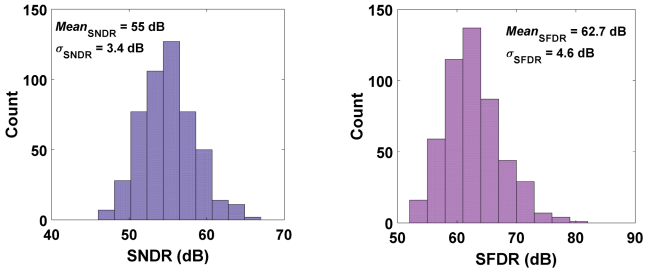

Fig. 6. Monte Carlo simulations for extracting the histogram of the SNDR and SFDR before enabling element mismatch calibration.

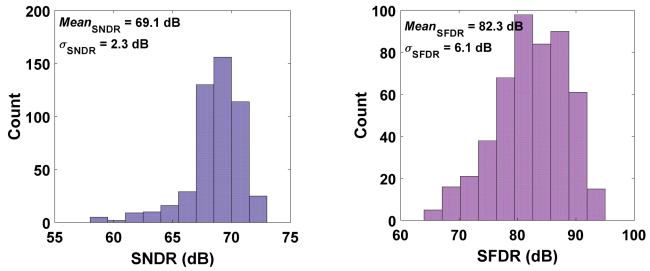

Fig. 7. Monte Carlo simulations for extracting the histogram of the SNDR and SFDR after enabling element mismatch calibration.

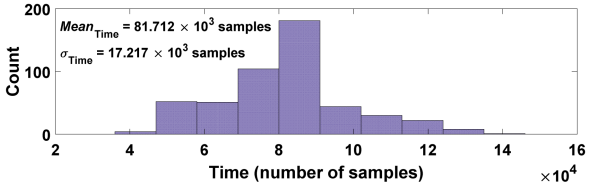

Fig. 8. Monte Carlo simulations for extracting the histogram of the convergence time after enabling element mismatch calibration.

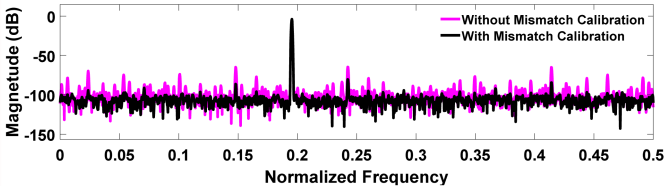

Fig. 9. Output spectrum of the ADC before and after the calibration of mismatch.

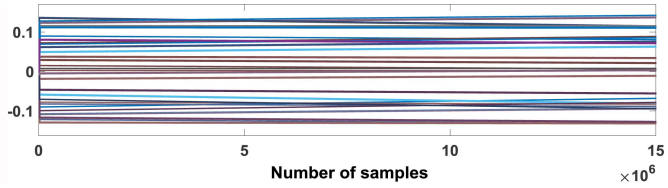

Fig. 10. Convergence of the coefficients of the block FIR filter during the SAR ADC operation.

level, and the resolution of the ADC remain above the desired value. Therefore, these step-sizes must be selected according to the desired resolution of the predictive SAR ADC. Also, the step-sizes need to be decreased by a factor of 4 for each 1-bit increase in the desired resolution of the ADC [45].

IV. SIMULATION RESULTS AND DISCUSSIONS

In this section, the presented multirate predictive SAR ADC along with the proposed calibration mechanism is simulated to evaluate its effectiveness. The target resolution of the ADC is considered to be 12 bits. Therefore, the subtraction and error extraction arrays of the BCR-DAC are binary-weighted and have 12 and 7 capacitive elements, respectively. The thermal noise and the comparator offset are also considered in accordance with the resolution of the ADC. Also, the sampling-frequency is set to 1; as a result, the frequency of all signals is consequently normalized to 1. The following simulations are performed with the values that are shown in Table I. In these simulations, the mismatches among the capacitive elements are assumed to be independent Gaussian random variables. Furthermore, the standard deviation of each element in the CR-DAC is chosen according to its weight with respect to the standard deviation of the unit capacitor.

Firstly, the Monte Carlo method is utilized to evaluate the robustness of the presented SAR ADC to the variability of the input signal frequency, the mismatch among the elements of the subtraction and error extraction arrays, and the offset of the comparator. In these simulations, a single-tone sinusoidal is applied to the ADC as the test input signal, and the spurious-free dynamic range (SFDR) and signal-to-noise and distortion ratio (SNDR) are used as the performance metrics, and for each resultant SNDR histogram, 500 simulations are performed. Moreover, all thermal noise sources, the mismatch in the subtraction and error extraction arrays, and the offset of the comparator are chosen randomly in each of the simulations. In each simulation, the input frequency is also randomly generated to cover almost all the frequency range of 0 to half the Nyquist-rate. Fig. 6 shows the SFDR and SNDR histograms before enabling the mismatch calibration. The mean values of the SFDR and SNDR are 62.7 and 55 dB, respectively. Furthermore, Fig. 7 depicts the SFDR and SNDR histograms after enabling the mismatch calibration. As can be seen from the figure, the means of the SFDR and SNDR are enhanced to 82.3 and 69.1 dB, respectively. As expected, the effective number of bits (ENOB), which is calculated using (SNDR $-$ 1.76)/6.02, is limited to less than 10 bits before the calibration, and it is enhanced to more than 11 bits after calibration. Accordingly, the proposed SAR ADC achieves its desired resolution. The convergence time histogram is illustrated in Fig. 8. For the mean of the convergence time, the required number of samples for convergence is 81.71×10^3.

Additionally, a single simulation with a single-tone sinusoidal is performed to show the power spectral density (PSD)

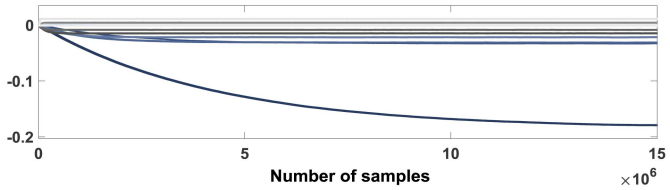

Fig. 11. Convergence of the weights of the DMC block during the normal operation of the ADC with the mismatch calibration.

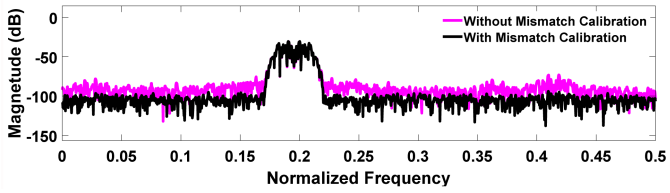

Fig. 12. Output spectrum of the ADC before and after the calibration of mismatch.

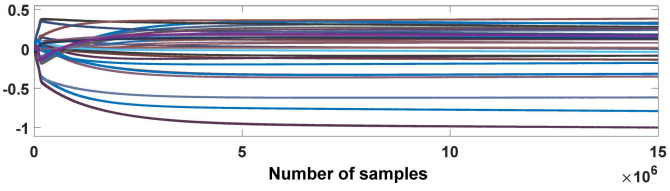

Fig. 13. Convergence of the coefficients of the block FIR filter in the DPM during SAR ADC operation.

of the predictive SAR ADC output and the stability of the coefficients of the block FIR filter and the weights of the DMC. The PSDs of the predictive SAR ADC output before and after enabling the elements mismatch calibration mechanism are shown in Fig. 9. Moreover, Fig. 10 illustrates the convergence of the coefficients of the block FIR filter during the operation of the ADC. In addition, the convergence of the digital weights of the DMC block is depicted in Fig. 11. The operation and stability of the predictive SAR ADC for a sinusoidal modulated by a band-limited random signal is shown with a single simulation. In this simulation, the normalized bandwidth, BW/f_S, of the input signal is 0.05. A block FIR filter with $M = 8$ is sufficient for $BW/f_S = 0.05$. Fig. 12 demonstrates the PSDs of the SAR ADC before and after enabling the mismatch calibration mechanism. Fig. 13 shows the convergence of the coefficients of the block FIR filter during the normal operation of the SAR ADC. The convergence of the digital weights of the DMC block during normal operation of the ADC before and after enabling the elements mismatch calibration are also illustrated in Fig. 14. According to Figs. 9 and 12, the distortions in the PSD of the ADC output are effectively reduced after calibration, as expected. Similar results are obtained for different input frequencies as well.

A. Comparison to Similar Methods

In contrast to the other predictive ADCs [26], [29], [30], the predictive SAR ADCs [27], [28], [31] benefit from the efficiency and simplicity of the SAR approach, and they

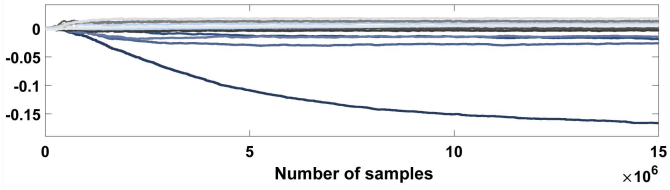

Fig. 14. Convergence of the weights of the DMC block during normal operation of the ADC with the mismatch calibration.

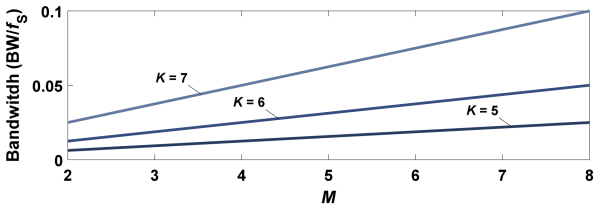

Fig. 15. Maximum bandwidth as a function of M for three values of K.

also do not use any power-hungry amplifier. Not requiring an amplifier is a key advantage as the design of high-gain and high-speed op-amps in advanced CMOS processes is challenging [28], [32]. The predictive SAR ADCs are based on the subranged method. Thus, the predictive SAR ADC has a reduced number of steps in the conversion phase as well. In contrast to the subranged mechanism, the need for the flash ADC is alleviated. Consequently, the associated timing mismatch among the flash ADC and CR-DAC is not a concern. It must be noted that the compensation techniques often need complex digital circuits for resolutions beyond 10 bits, and they also impose various restrictions on the frequency, amplitude, and probability distribution of the input signal.

In the presented SAR ADC, the convergence of the coefficients of the block FIR filter and the weights of the DMC are not susceptible to the offset of the comparator. Finally, the input signal frequency of the proposed SAR ADC can cover the entire frequency range from 0 to half the Nyquist-rate.

As stated earlier, the elements mismatch of the BCR-DAC can be measured and compensated by the residue voltage in analog domain [21]. Conversely, the proposed calibration scheme reuses the predicted signal, D_{pre}, for both digital measurement and adaptive compensation of the elements mismatch of the BCR-DAC. It should be noted that the equivalent sampling capacitance, C_S, can be considerably decreased and chosen in accordance with the thermal noise requirement. This reduction in the sampling capacitance leads to substantial decrease in the power consumption and die area of the SAR ADC [46].

It is worth mentioning that the proposed digital mismatch calibration method reduces the errors arising from the mismatch among the elements of the subtraction array over all frequencies from 0 to half the Nyquist-rate. Moreover, in contrast to the current predictive ADCs, the presented SAR ADC does not limit the input signal frequency to a predetermined range of low frequencies by exploiting the

TABLE II
COMPARISON WITH OTHER TECHNIQUES

Reference	The Capability of Elements Mismatch Calibration	The Need for Power Hungry Opamp	The Need for Extra Flash ADC	Input Frequency Limitations	Input Bandwidth Limitations	The Need for Timing Mismatch Calibration
This Work	✓	×	×	×	✓	×
[28], [31]	×	×	×	✓	✓	×
[26], [30], [32]	×	✓	✓	✓	✓	×
[29]	×	×	×	✓	✓	×
[17], [18]	×	×	✓	×	×	✓

ADPM [26]–[32]. For these reasons, the proposed predictive SAR ADC operates with various frequencies from 0 up to half the Nyquist-rate as verified in the above simulations. In addition, the multirate realization of the ADPM relaxes the speed limitations of this block by a factor of R. Thus, the overall sampling-rate can be increased via the multirate implementation of the ADPM and the digital calibration of the BCR-DAC. In summary, the advantages of the proposed predictive SAR ADC over the currently available predictive ADCs [26]–[32] rely on the digital compensation of the elements mismatch in the BCR-DAC, the restriction alleviation of the input frequency through the presented ADPM, and the relaxing of the speed requirement of the ADPM by utilizing the multirate implementation. The multirate predictive SAR ADC is qualitatively and concisely compared with the other relevant methods in Table II.

B. Adaptive Prediction Considerations

The ADPM is suitable for the improvement of the maximum achievable sampling-rate of a SAR ADC since the power dissipation of the ADPM block can be considerable [see Section IV-D]. The predictive SAR ADC imposes some restrictions on the input signal; nevertheless, these limitations do not affect the feasibility of the predictive SAR ADC. First of all, the input signal must be band-limited. The predictive SAR ADC operates well, even with a small value of M (i.e., $M = 2$). According to (4), it can be shown that the length M needs to be increased as the bandwidth of the input signal is increased. Fig. 15 demonstrates the maximum bandwidth as a function of M and K. Also, the convergence rate of the ADPM decreases as the amplitude of the input signal is reduced.

Since the input of the ADPM is the sum of the delayed predicted digital output and the prediction error, the ADPM input is firstly dominated by the prediction error (which is saturated and just represents the sign of the input signal), and it converges to the digital format of the input signal. Accordingly, it can be argued that the ADPM is not placed in a closed loop. Moreover, the stability of the ADPM can be explained by the adaptive FIR filter theory. Furthermore, the initial saturation of the signal $D_{e,pre}(n)$ does not result in the divergence of the proposed prediction mechanism. It should be noted that the bank of the FIR filters in the ADPM operate independently and concurrently, and these FIR filters can also be evaluated and explained by the traditional adaptive filter theory [34]. The proposed SAR ADC works well *as long as* the equivalent bandwidth of the desired input signal and the blocker are less than the maximum expected bandwidth for which the block FIR filter is designed [33]. For this reason, the equivalent bandwidth must be considered in designing the block FIR filters by increasing the length M.

According to the adaptive filter theory, the constants μ_{pre} and η_{mis} are upper bounded by the minimum of the eigenvalues of the input correlation matrix. Nevertheless, these constants practically must be chosen small for medium to high resolutions to limit the variations of the weights of the DMC and the coefficients of the ADPM and to hold the resolution above the specified value.

C. Sensitivity to Non-Idealities of the Comparator and Error Extraction Array

The noise and the offset of the comparator do not exhibit any major impact on the resolution and performance of the presented SAR ADC. Nonetheless, the imperfections of the error extraction array introduce a nonlinear error related to the prediction error. These imperfections can affect the resolution of the predictive SAR ADC. The sensitivity of the digital calibration method to the error extraction is also resolved through the bridge structure with the enlargement factor L. The elements mismatch in the error extraction array can be bounded by expanding the elements by L. According to extensive simulations, the proposed predictive SAR ADC is not susceptible to the deviation of γ *assuming that* the deviation remains below 10%. In practice, the variation of γ is less than 1% [22].

D. Complexity of the Digital Circuits

It is worth mentioning that the ADPM block makes the main contribution to the digital power consumption. Based on extensive simulations, the presented SAR ADC works well *in case* all the arithmetic operations in the ADPM are performed by a word length of more than 13 bits. As stated above, the predictive SAR ADC operates well with a sine-wave provided that $M \geq 2$. Consequently, the minimum number of gates needed for the digital circuitry is approximately 50 K. Moreover, the required power for every gate in 28 nm CMOS technology is estimated to be less than 0.8 nW/gate-MHz [47], [48], and this power declines as we move to lower feature size CMOS technologies. For this reason, the required power per conversion of the ADPM is estimated to be less than 20 pJ for $M = 2$ in a 28 nm CMOS.

It should be noted that the number of required gates and power consumption both increase proportional to the value of M. For a normalized bandwidth of 0.05, the parameter M must be greater than 7; consequently, for $M = 8$, the required number of gates and power per conversion of the ADPM are less than 200 K and 80 pJ, respectively, in a 28 nm CMOS [47], [48]. However, the power per conversion can be reduced and optimized based on the required maximum bandwidth for a given application.

Additionally, the minimum power dissipation per conversion of a SAR ADC with an SNDR of 70 dB is expected to be more than 100 pJ [18], [46], [49], [50]. This cost could be roughly reduced by a factor of 2 via the predictive SAR ADC. Nonetheless, the extra power per conversion imposed by the ADPM is 80 pJ in a 28 nm CMOS technology. As a consequence, the power per conversion of the predictive SAR ADC is approximately the same as that of the traditional SAR ADCs. Nevertheless, it should be noted that the power dissipation of the ADPM is decreased in lower feature size CMOS technologies. To sum up, the predictive SAR ADC would be an attractive field for research and development in nanometer CMOS technologies, and it could be utilized in future CMOS technologies.

V. Conclusions

In this paper, a multirate predictive SAR ADC has been introduced. The key objective of this paper is the introduction of digital frameworks for resolving the limitations of the past and current state-of-the-art predictive ADCs in the context of SAR ADCs. The proposed SAR ADC uses ADPM to relax the frequency restriction of the input signal; in turn, the ADC operates well with any input frequency within the range of 0 to half the Nyquist frequency. The operational frequency restriction of the ADPM is also alleviated through utilizing multirate implementation. Furthermore, the presented SAR ADC has the resolution enhancement capability by compensating the elements mismatch in digital domain. Accordingly, the achievable sampling-rate can also be increased by optimizing the capacitors according to the thermal noise requirements.

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