Statistics-Based Digital Background Calibration of Residue Amplifier Nonlinearity in Pipelined ADCs

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***Abstract*— In this paper, a statistics-based digital background calibration technique for pipelined analog-to-digital converters (ADCs) is presented. This technique employs the residue voltage probability distribution to continuously estimate and digitally eliminate the conversion errors resulted from the residue amplifier gain error and third-order nonlinearity. In order to remove the conversion errors, the proposed method evaluates and corrects the digitized residue probability distribution exploiting a two-level pseudorandom-noise sequence. Behavioral simulation results are provided for a 12-bit pipelined ADC architecture to validate the effectiveness of this scheme. The required number of conversions for convergence is approximately 5×10^6. With calibration, the signal-to-noise and distortion ratio is improved from 49.9 to 70.9 dB.**

***Index Terms*— Analog-to-digital conversion, pipelined ADCs, digital background calibration, linearization techniques, adaptive systems, digital signal processing.**

I. Introduction

THE dimension scaling of advanced CMOS technologies has resulted in the attractive modifications of data converters, specifically the pipelined analog-to-digital converter (ADC) [1]–[9]. Digital circuits are now realized with high integration density thanks to the dimension scaling, and faster operation rates are now available with lower power dissipation at the same time. Furthermore, it is preferred to design the power-optimized residue amplifier with bandwidth as high as possible [1]–[7], [10]–[24]. Unfortunately, the nonidealities of these amplifiers restrict the accuracy of pipelined ADCs to less than 10 bits. Consequently, digital calibration techniques must be utilized to minimize errors caused by the residue amplifier and to achieve the desired resolution in power-optimized pipelined ADCs with simplified analog circuits [10]–[17], [19], [24].

Digital calibration techniques are categorized into *foreground* and *background* methods [15], [19]. A foreground calibration technique needs to interrupt the data-conversion operation whereas digital background techniques operate in the background without interrupting the ADC normal operation. Since digital background techniques can continuously measure and digitally remove the conversion errors, these schemes are extensively exploited to continuously track and mitigate errors caused by the voltage drifts and temperature variations [10]–[17], [19], [24].

Digital background calibration techniques generally perform two *correction* and *estimation* operations. The correction block is often realized by a digital polynomial function. Besides, an estimation block is required to precisely determine the coefficients of the polynomial. The estimation methods can also be classified as *correlation-based* [10], [11], *statistics-based* [12]–[18], *skip-and-fill* [1], [19], and *split-based* [20], [21], [23], [25] techniques. The correlation-based and skip-and-fill estimation techniques often need multi-bit multipliers in order to measure the conversion errors. Therefore, they dissipate large power in digital domain. Calibration of the split-based ADC often requires double digital circuitry. In contrast, the statistics-based estimation techniques employ input signal statistics and do not require any multi-bit multiplier for extracting the errors at the sampling rate of the ADC. Nevertheless, the relative disadvantage of the statistics-based scheme in [13] is that, it utilizes an array of counters to estimate and correct the residue amplifier non-idealities. Unfortunately, the number of counters in the array increases exponentially with the resolution of the ADC [11]. Moreover, the statistics-based approaches in [13] and [14] strictly depend on the input signal statistics, and the method of [15] requires multi-bit multipliers as well. The drawback of the statistics-based technique of [16] is that it cannot remove the errors introduced by the residue amplifier nonlinearity, while the performance of the pipelined ADCs is limited by the residue amplifier nonlinearity in high-resolution applications [10]–[15].

This paper presents a statistics-based digital background residue amplifier calibration technique for pipelined ADCs. The proposed method can continuously measure and digitally cancel the errors caused by the gain error and third-order nonlinearity of the residue amplifier without the need for the interruption of the converter normal operation. In order to mitigate the errors, this technique evaluates and corrects the digitized residue probability distribution using a *pseudorandom-noise* (*PN*) sequence. This scheme does not need any array of counters as opposed to [12], and any multi-bit multiplier in contrast to [15], and it cancels the residue amplifier nonlinearity in contrast to [16]. Although

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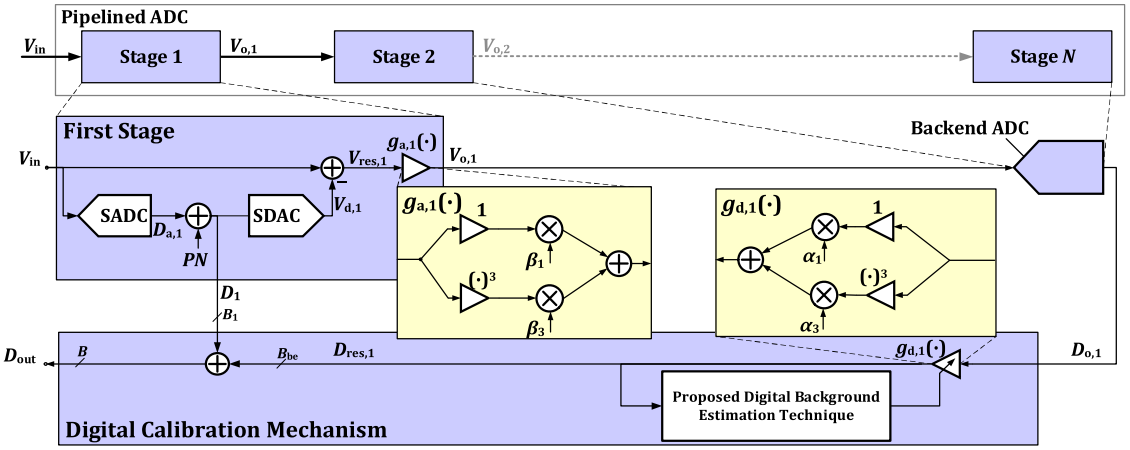

Fig. 1. Simplified model of a pipelined ADC with digital calibration technique.

the presented mechanism exhibits some requirements on the statistics of the input signal similar to other methods, e.g., [12], [15], [16], [18], [26], it does not strictly depend on the input signal statistics in contrast to [13] and [14].

The paper is structured as follows. Section II reviews the architecture of pipelined ADCs and digital cancellation mechanism. Section III presents the proposed digital background estimation technique. Simulation results and discussions are presented in Section IV. Finally, Section V concludes the paper.

II. Architecture of Pipelined ADCs and Digital Cancellation Mechanism

As demonstrated in Fig. 1, N low-resolution pipeline stages construct a pipelined ADC. For the sake of convenience, all signals are distributed inside the interval $[-1, 1]$ by normalizing them to the reference voltage like [11], [12], and [15]. Furthermore, as shown in Fig. 1, the paper initially presents the calibration of the residue amplifier imperfections in the first stage, and the backend ADC, comprised of all the following $(N-1)$ stages, is considered to be ideal. Nevertheless, the proposed calibration scheme can also be applied to each of the stages and utilized concurrently in as many stages as required to achieve the desired resolution [see Section IV]. Due to the fact that the task of the proposed scheme is to eliminate the errors caused by residue amplifier non-idealities, the sub-ADC (SADC) and sub-DAC (SDAC) are also supposed to be ideal as in [10]–[12]. However, all these imperfections are included in the simulations of Section IV. As indicated in Fig. 1, the SADC compares the input voltage, V_{in}, with M reference levels by analog comparators to produce an M-level digital approximation, and the reference levels are equally spaced in the range $[-1, +1]$. The output of each comparator is equal to $+1$ if the input signal is greater than the reference level and it is identical to -1, otherwise. In case, the outputs of the comparators are multiplied by the factor of $\Delta/2$ and summed together, the digital output of the SADC can be expressed as:

$$D_{a,1} = V_{in} + \varepsilon_{q,1} \tag{1}$$

where $\varepsilon_{\text{q},1}$ stands for the SADC *quantization error*. The *probability density function* (PDF) of the SADC quantization error, $f_{\text{EQ1}}(\varepsilon_{\text{q},1})$, is distributed over the interval

$$-\Delta/2 < \varepsilon_{q,1} < \Delta/2 \tag{2}$$

where Δ denotes the *step-size* of the SADC and given by $\Delta = 2/M$ [27]–[29]. In this paper, it is supposed that the probability distribution of the SADC quantization error is approximately uniform within the range $[-\Delta/2, \Delta/2]$ to clarify the presentation [see Section IV-B].

In order to extract and remove the errors resulted from the residue amplifier imperfections, a *pseudorandom-noise* (*PN*) *sequence*, $PN \in \{-1, +1\}$ is also employed [22]. The *PN* signal approximates a *zero-mean random process* as following

$$P(PN = 1) = 0.5, \quad P(PN = -1) = 0.5 \tag{3}$$

where $P(x)$ denotes the probability of happening of the event x. The pseudorandom-noise sequence is *independent* of the SADC quantization error, $\varepsilon_{\text{q},1}$. The digital output of the first stage is obtained by

$$D_1 = D_{a,1} + (\Delta/2) \cdot PN. \tag{4}$$

Afterwards, the SDAC consists of $M+1$ *nominally* identical elements. Each element *ideally* produces its output as

$$y_i = (\Delta/2)\, x_i, \quad i = 1, \ldots, M+1 \tag{5}$$

where x_{i} is the input of the ith element, and Δ can also be considered as the step-size of the elements. The outputs of the comparators are directly applied to M elements. Moreover, the *PN* sequence is also applied to the $(M+1)th$ element to generate the *calibration signal*, *CS*, as

$$CS = \Delta/2 \cdot PN. \tag{6}$$

In reality, the step-size of the SDAC elements randomly deviates from the ideal value of $\Delta/2$, and these non-idealities can bound the desired resolution of the ADC. The SDAC output voltage, $V_{\text{d},1}$, is the sum of the outputs of all the elements, and it can be considered as the analog format of D_1 in the absence of the SDAC imperfections. The SDAC

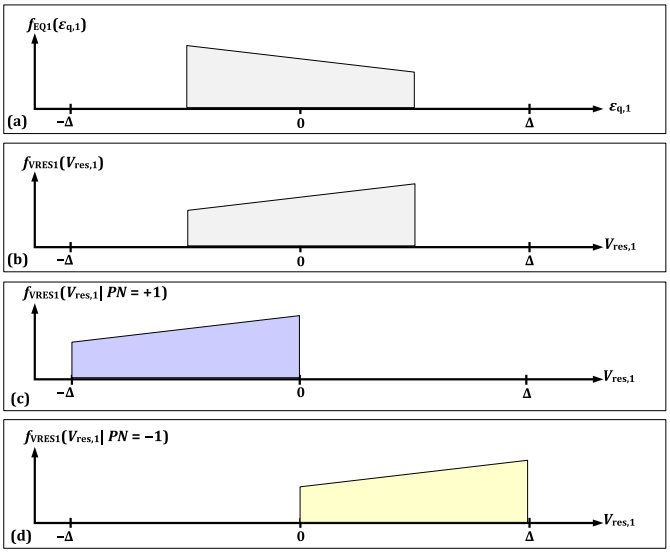

Fig. 2. (a) SADC quantization error distribution, (b) residue voltage distribution without the injection of the calibration signal, (c) residue voltage distribution for $PN = +1$, and (d) residue voltage distribution for $PN = -1$.

output is then subtracted from the sampled input voltage to generate the *residue voltage* as following

$$V_{res,1} = V_{in} - V_{d,1}. \tag{7}$$

By plugging (1) into (4) and exploiting CS instead of the term $(\Delta/2)\times PN$, the residue voltage can be conceptually represented by

$$V_{res,1} = -\left(\varepsilon_{q,1} + CS\right). \tag{8}$$

It is evident from (8) that without the injection of the calibration signal (i.e., $CS = 0$), the residue voltage PDF, $f_{\mathrm{VRES1}}(V_{\mathrm{res},1})$, is identical to $f_{\mathrm{EQ1}}(-V_{\mathrm{res},1})$. Fig. 2(a) depicts an example PDF of the SADC quantization error. Fig. 2(b) demonstrates the residue voltage PDF corresponding to the example probability distribution shown in Fig. 2(a), without the addition of the calibration signal.

Since the residue voltage PDF, $f_{\mathrm{VRES1}}(V_{\mathrm{res},1})$, is analyzed by the proposed technique, the *conditional probability density functions* (CPDFs) of the residue voltage need to be investigated for two possible states of *PN*. It follows from (2), (6), and (8) that the state $PN = +1$ shifts the residue voltage from the range $[-\Delta/2, \Delta/2]$ to the interval $[-\Delta, 0]$ and the residue voltage CPDF for the mode $PN = +1$ is given by

$$f_{VRES1}\left(V_{res,1}\middle|\ PN = +1\right) = f_{EQ1}\left(-V_{res,1} - \Delta/2\right). \tag{9}$$

Similarly, the mode $PN = -1$ shifts the residue voltage from the interval $[-\Delta/2, \Delta/2]$ to the range $[0, \Delta]$, and the residue voltage CPDF for the state $PN = -1$ is also expressed as

$$f_{VRES1}\left(V_{res,1}\middle|\ PN = -1\right) = f_{EQ1}\left(-V_{res,1} + \Delta/2\right). \tag{10}$$

Due to the fact that the SADC quantization error is independent of the calibration signal, from (9) and (10), it can be verified that the residue voltage probability distribution, $f_{\mathrm{VRES1}}(V_{\mathrm{res},1})$, is distributed over the range $-\Delta < V_{\mathrm{res},1} < \Delta$ with the injection of the calibration signal.

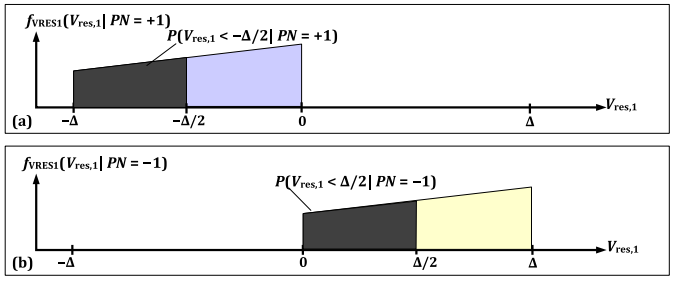

Fig. 3. (a) Probability of $P(V_{\mathrm{res},1} < -\Delta/2|PN = +1)$ and (b) probability of $P\ (V_{\mathrm{res},1} < \Delta/2|PN = -1)$.

Figs. 2(c) and 2(d) depict the CPDFs $f_{\mathrm{VRES1}}(V_{\mathrm{res},1}|PN = +1)$ and $f_{\mathrm{VRES1}}(V_{\mathrm{res},1}|PN = -1)$ corresponding to the PDF $f_{\mathrm{EQ1}}(\varepsilon_{\mathrm{q1}})$ depicted in Fig. 2(a), respectively.

From (9) and (10), it is evident that the residue voltage has the following properties:

Property 1: $f_{\mathrm{VRES1}}(V_{\mathrm{res},1}|PN = +1)$ is a function of $f_{\mathrm{VRES1}}(V_{\mathrm{res},1}|PN = -1)$ as

$$f_{VRES1}\left(V_{res,1}\middle|\ PN = +1\right) = f_{VRES1}\left(V_{res,1} + \Delta\middle|\ PN = -1\right), \tag{11}$$

for $-\Delta < V_{\mathrm{res},1} < 0$.

Property 2: It follows from Property 1 that the probability of a residue voltage sample which is less than $-\Delta/2$ for $PN = +1$ is identical to the probability of a residue voltage sample which is less than $\Delta/2$ for $PN = -1$ as following

$$P\left(V_{res,1} < -\Delta/2\middle|\ PN = +1\right) = P\left(V_{res,1} < \Delta/2\middle|\ PN = -1\right), \tag{12}$$

as illustrated in Figs. 3(a) and 3(b) with shaded areas. The residue voltage CPDFs in Figs. 3(a) and 3(b) are corresponding to the CPDFs in Figs. 2(c) and 2(d), respectively. In (12), $P(x_1 < X < x_2|PN)$ denotes the probability of occurring the event $x_1 < X < x_2$, which is defined as following

$$P\left(x_1 < X < x_2\middle|\ PN\right) = \int_{x_1}^{x_2} f_X\left(x\middle|\ PN\right) dx. \tag{13}$$

Afterwards, the residue $V_{\mathrm{res},1}$ is amplified by the *residue amplifier*, $g_{\mathrm{a},1}$, to generate the *output voltage* of the first stage, $V_{\mathrm{o},1}$. Ideally, the residue amplifier must linearly scale the residue voltage to the range $-1 < V_{\mathrm{o},1} < 1$ [11], [28]. In the perfect case, without the addition of the calibration signal, it follows from (2) that the *nominal gain* of the residue amplifier, β_{nom}, needs to be equal to $2/\Delta$, while with the injection of the calibration signal, from (2), (6), and (8), it is obvious that the residue amplifier nominal gain must be identical to $1/\Delta$. Thus, the reduction of the residue amplifier gain is practically necessary to restrict the output voltage of the first stage within the interval $-1 < V_{\mathrm{o},1} < 1$ [10]–[12], [15], [24]. In other words, the resolution of both SADC and SDAC must be doubled for a specified residue amplifier gain. It is worth mentioning that the residue amplifier gain determines the resolution of any stage, and the stage resolution, B_{i} $(i = 1, \ldots, N)$, is expressed by $log_2(g_{\mathrm{a,i}})$. Moreover, the

ith stage ($i = 1, \ldots, N$) enhances the digitized residue resolution of its following stage by $B_{\rm i}$. As seen from Fig. 1, the first stage improves the resolution of the digitized residue, produced via the following stages, by B_1, and hence, the equivalent resolution of the ADC, B, is identical to $B_1 + B_{\rm be}$. Accordingly, the effective resolution of the ADC is the sum of the resolution of all the stages.

In reality, the non-idealities produced by a wide-bandwidth residue amplifier (e.g., a single-stage amplifier) can be modeled sufficiently enough by a *memory-less weakly-nonlinear* function [10]–[15], [24]. Hence, a practical residue amplifier is actually modeled as [10], [11], [13]–[15], [24]

$$V_{o,1} = g_{a,1}\left(V_{res,1}\right) \approx \beta_1 V_{res,1} + \beta_3 V_{res,1}^3 \tag{14}$$

where β_1 and β_3 stand for the *gain* and *third-order nonlinearity* of the residue amplifier, respectively. In the absence of non-ideal circuit behavior, β_1 and β_3 would be equal to $\beta_{\rm nom}$ and zero, correspondingly. Since the residue amplifier is actually designed using fully differential circuits, *even-order* term is negligible (i.e., $\beta_2 \approx 0$) [see Section IV-C]. The output voltage, $V_{\rm o,1}$, is then digitized by the backend ADC as following

$$D_{o,1} = V_{o,1} + \varepsilon_{qbe} \tag{15}$$

where $D_{\rm o,1}$ and $\varepsilon_{\rm qbe}$ denote the digitized output and the backend ADC quantization error, respectively. In the remainder of the paper, the backend ADC quantization error, $\varepsilon_{\rm qbe}$, is ignored to simplify the analysis.

In fact, severe impacts of a weakly nonlinear residue amplifier can be minimized in digital domain by the *inverse function*, $g_{\rm a,1}^{-1}$ [10]–[14], [19], [24]. As the residue amplifier is often weakly nonlinear, the inverse function, $g_{\rm a,1}^{-1}$, can also be approximated in digital domain as following [10], [11], [13], [14], [24]

$$D_{res,1} = g_{d,1}\left(D_{o,1}\right) = \alpha_1 D_{o,1} + \alpha_3 D_{o,1}^3 \tag{16}$$

where $D_{\rm res,1}$ and $g_{\rm d,1}$, stand for the *digitized residue* and the *digital correction block*, respectively. Moreover, α_1 and α_3 represent the *gain correction coefficient* and the *third-order nonlinearity correction coefficient*, respectively. By substituting (14) into (15), plugging (15) into (16), and neglecting higher-order terms, we have

$$D_{res,1} \approx (1 + e_1)\, V_{res,1} + e_3 V_{res,1}^3 \tag{17}$$

where

$$e_1 = \beta_1\alpha_1 - 1, \tag{18}$$

$$e_3 = \beta_1^3\alpha_3 + \beta_3\alpha_1. \tag{19}$$

The terms e_1 and e_3 in (17) denote the *gain* and *nonlinear errors* in $D_{\rm res,1}$, correspondingly. It follows from (18) and (19) that the errors e_1 and e_3 can be mitigated through properly adjusting α_1 and α_3 *providing that* the values of β_1 and β_3 are known. In the ideal case (i.e., $e_1 = e_3 = 0$), the digitized residue is the digital format of the residue voltage; and hence, the digitized residue probability distribution is equal to the residue voltage PDF. For this reason, the CPDFs of $D_{\rm res,1}$ are also given by

$$f_{DRES1}\left(D_{res,1}\middle|\, PN = +1\right) = f_{VRES1}\left(V_{res,1}\middle|\, PN = +1\right), \tag{20}$$

$$f_{DRES1}\left(D_{res,1}\middle|\, PN = -1\right) = f_{VRES1}\left(V_{res,1}\middle|\, PN = -1\right), \tag{21}$$

with $D_{\rm res,1} = V_{\rm res,1}$. Furthermore, the digitized residue satisfies Property 1 and Property 2, as well. As seen from Fig. 1, the *digital output* of the ADC is given by

$$D_{out} = D_1 + D_{res,1}. \tag{22}$$

In reality, the values of the coefficients of $g_{\rm a,1}$ are not known and can be changed by *supply voltage drifts* and *temperature variations* [10], [12]–[15]. In principle, the digital background calibration method needs to precisely estimate and continuously adjust the coefficients of $g_{\rm d,1}$ during the normal conversion operation. This paper presents a statistics-based digital background estimation method which accurately determines the coefficients of $g_{\rm d,1}$ during the data-conversion process.

III. Digital Background Estimation Technique

The proposed background estimation algorithm exploits the PDF of the SADC quantization error and the calibration signal to extract and correct the residue amplifier non-idealities. In order to eliminate the conversion errors arising from the residue amplifier imperfections, the presented method evaluates and corrects the digitized residue CPDFs using the calibration signal. As explained above, the digitized residue is ideally required to satisfy Property 1 and Property 2, whereas it will be shown that, in the presence of the residue amplifier non-idealities, the digitized residue distribution deviates from its corresponding residue voltage distribution and the digitized residue cannot satisfy Property 1 and Property 2 as well. The presented scheme employs these properties to detect the residue amplifier imperfections and remove the conversion errors.

First of all, a simple operator, which can be simply implemented in hardware, is mentioned. In this paper, the digital conditional comparison is utilized to detect the required conditional probabilities. This operator is defined as

$$h\left(x\middle|\, PN = m\right) = \begin{cases} \operatorname{sgn}(x), & PN = m, \\ 0, & PN \neq m. \end{cases} \tag{23}$$

In (23), the sign operator $\operatorname{sgn}(x) = 2$ if $0 \leq x$ and $\operatorname{sgn}(x) = 0$, otherwise. From the basic probability theory, it is obvious to show that [see Appendix A]

$$E\left[\operatorname{sgn}(x)\right] = 2 \times P\,(0 \leq x) \tag{24}$$

and

$$E\left[h\left(x\middle|\, PN = m\right)\right] = 2P\,(PN = m) \times P\left(0 \leq x\middle|\, PN = m\right) \tag{25}$$

where $E[x]$ is the mean of the variable x. Since the operator $h(.)$ is proportional to its corresponding conditional probability, this operator is employed to extract the required

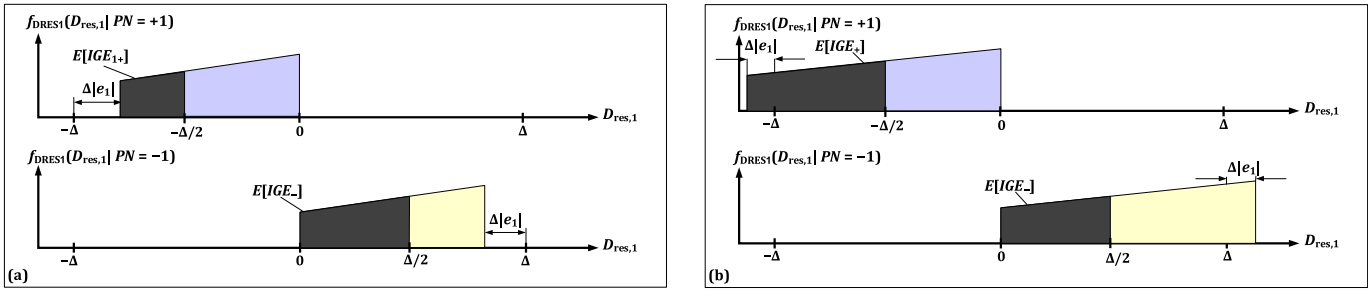

Fig. 4. Digitized residue distribution in the presence of the gain error: (a) for $e_1 < 0$ and (b) for $e_1 > 0$.

conditional probabilities. From (3), the mean of $h(x|PN = m)$ is expressed as

$$E\left[h\left(x\right|PN = m)\right] = P\left(0 \le x\right|PN = m) \quad for\ m = \pm 1. \tag{26}$$

The above expression indicates that the mean of the conditional operator, $h(x|PN = m)$, is identical to its corresponding conditional probability. For this reason, this result will be exploited in the proposed calibration mechanism to estimate the gain and third-order nonlinear errors.

A. Gain Error Estimation Technique

In this sub-section, only the gain error is considered (i.e., $e_1 \neq 0$ and $e_3 = 0$). In the presence of the gain error, it follows from the basic probability and (17) that the digitized residue CPDFs are scaled versions of their corresponding residue voltage CPDFs; it can therefore verify that $f_{\mathrm{DRES1}}(D_{\mathrm{res},1}|PN = +1)$ and $f_{\mathrm{DRES1}}(D_{\mathrm{res},1}|PN = -1)$ are distributed over the intervals $[-\Delta(1 + e_1),\ 0]$ and $[0,\ \Delta(1 + e_1)]$, respectively. Moreover, it can be proved that $f_{\mathrm{DRES1}}(D_{\mathrm{res},1}|PN = +1)$ is a shifted version of $f_{\mathrm{DRES1}}(D_{\mathrm{res},1}|PN = -1)$ as following

$$f_{DRES1}\left(D_{res,1}\right|PN = +1) = f_{DRES1}\left(D_{res,1} + (1 + e_1)\,\Delta\right|PN = -1), \tag{27}$$

for $-\Delta(1 + e_1) < D_{\mathrm{res},1} < 0$. In the desired case, it follows from (20), (21), and Property 2 that the digitized residue CPDFs must satisfy

$$P\left(D_{res,1} < -\Delta/2\right|PN = +1) = P\left(D_{res,1} < \Delta/2\right|PN = -1), \tag{28}$$

while in the presence of the gain error, (28) is not true. In order to show this and practically detect the gain error, the *instantaneous gain error* is defined as

$$IGE = IGE_+ - IGE_- \tag{29}$$

where IGE_+ and IGE_- are implemented as follows:

$$IGE_+ = h\left(-\Delta/2 - D_{res,1}\right|PN = +1), \tag{30}$$

$$IGE_- = h\left(\Delta/2 - D_{res,1}\right|PN = -1). \tag{31}$$

In Addition, by utilizing (3) and (26), the mean of the instantaneous gain error, $E[IGE]$, is given by:

$$E\left[IGE\right] = P\left(D_{res,1} < -\Delta/2\right|PN = +1) + P\left(D_{res,1} < \Delta/2\right|PN = -1). \tag{32}$$

The mean of $E[IGE]$ can be expressed as following [see Appendix B]

$$E\left[IGE\right] = \int_{-\Delta(1/2+e_1)}^{-\Delta/2} f_{DRES1}\left(D_{res,1}\right|PN = +1)\,dD_{res,1}. \tag{33}$$

From (33), it is evident that

1) If $e_1 = 0$, then the limits of integration are identical; *therefore*, $E[IGE] = 0$;
2) If $e_1 < 0$, then the limits of integration are reversed; *therefore*, $E[IGE] < 0$ (see Fig. 4(a));
3) If $e_1 > 0$, then the upper limit is greater than the lower limit; *therefore*, $E[IGE] > 0$ (see Fig. 4(b)).

Accordingly, the mean of the instantaneous gain error, $E[IGE]$, is approximately proportional to e_1. In many communication systems, the SADC quantization error, ε_{q1}, can be considered roughly uniform [12], [14]; hence, from (33), $E[IGE]$ can be expressed as

$$E\left[IGE\right] \approx e_1. \tag{34}$$

Therefore, in this case, the mean of $E[IGE]$ is approximately identical to e_1. Thus, $E[IGE]$ can be exploited as the *estimated gain error*. The gain error can be eliminated by properly tuning the digital variable α_1 such that $E[IGE]$ approaches 0. Since the mean $E[IGE]$ is not available, IGE is simply utilized as the noisy version of $E[IGE]$ in the proposed approach. The *update expression* is given by

$$\alpha_1\left(n + 1\right) = \alpha_1\left(n\right) + \mu_1 IGE\left(n\right) \tag{35}$$

where n and μ_1 denote the discrete-time index and the update step-size, respectively [15], [19], [26], [30].

B. Third-Order Nonlinearity Estimation Technique

Once the gain error is removed, the third-order nonlinearity error limits the ADC performance. From (19), the residue amplifier nonlinearity can be eliminated by optimally adjusting the coefficient α_3. In this sub-section, it is assumed that the gain error is already mitigated through the above-mentioned gain error estimation technique. Due to the key fact that the residue amplifier nonlinearity alters the shape of the digitized residue probability distribution, the CPDFs of the digitized residue deviate from their corresponding residue voltage CPDFs. It can be shown that *if* $e_3 \neq 0$, *then*

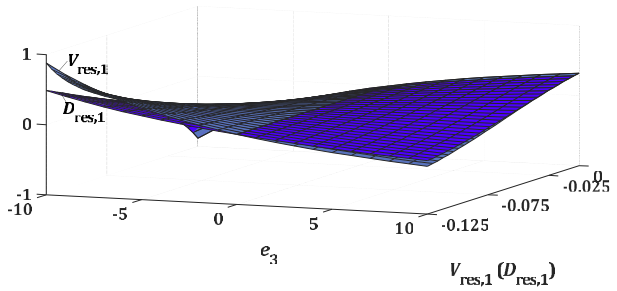

Fig. 5. $J_{\text{res}}(.)$ as a function of e_3 and $V_{\text{res},1}$ and also as a function of e_3 and $D_{\text{res},1}$.

(20) and (21) are not true [see (61) and (62)] and the digitized residue does not satisfy Property 1. In order to show this and exploit Property 1 for the measurement of e_3, the *estimated nonlinear error* (*ENE*) is defined as

$$ENE = ENE_+ - ENE_- \tag{36}$$

where

$$ENE_+ = f_{DRES1}\left(V_{res,1}\middle| PN = +1\right), \tag{37}$$
$$ENE_- = f_{DRES1}\left(V_{res,1} + \Delta\middle| PN = -1\right), \tag{38}$$

for $-\Delta < V_{\text{res},1} < 0$. In the ideal case, it follows from (20), (21), Property 1, and (36)-(38) that *ENE* is equal to zero, whereas in the presence of the residue amplifier third-order nonlinearity, the *ENE* can be written as following [see Appendix C]

$$ENE = J_{res}\left(V_{res,1}, e_3\right) \cdot f_{VRES1}\left(V_{res,1}\middle| PN = +1\right) \tag{39}$$

where

$$J_{res}\left(V_{res,1}, e_3\right) = \left\{\frac{1}{\left|1 + 3e_3 V_{res,1}^2\right|} - \frac{1}{\left|1 + 3e_3\left(V_{res,1} + \Delta\right)^2\right|}\right\}, \tag{40}$$

for $-\Delta < V_{\text{res},1} < 0$. Fig. 5 shows $J_{\text{res}}(V_{\text{res},1}, e_3)$ as a function of $V_{\text{res},1}$ over the range $[-\Delta, 0]$ for $-10 < e_3 < 10$ with $\Delta = 1/8$. As seen from Fig. 5, J_{res} is approximately proportional to e_3 with *identical sign* for $-\Delta/2 < V_{\text{res},1} < 0$, and with *opposite sign* for $-\Delta < V_{\text{res},1} < -\Delta/2$. Since it is supposed that the CPDF $f_{\text{DRES1}}(D_{\text{res},1}|PN = +1)$ is non-zero inside $-\Delta < V_{\text{res},1} < 0$ (as often the case), J_{res} could be used to detect e_3. From Fig. 5, and (39) and (40), it is obvious to verify that *ENE* is related to e_3 as following

1) If $e_3 = 0$, then $ENE = 0$ for $-\Delta < V_{\text{res},1} < 0$;
2) If $e_3 < 0$, then $ENE < 0$ for $-\Delta/2 < V_{\text{res},1} < 0$ and $ENE > 0$ for $-\Delta < V_{\text{res},1} < -\Delta/2$;
3) If $e_3 > 0$, then $ENE > 0$ for $-\Delta/2 < V_{\text{res},1} < 0$ and $ENE < 0$ for $-\Delta < V_{\text{res},1} < -\Delta/2$.

Accordingly, *if* the estimated nonlinear error is made identical to zero, *then* it is expected that the nonlinearity error, e_3, is also removed.

Fig. 5 also shows $J_{\text{res}}(D_{\text{res},1}, e_3)$ as a function of $D_{\text{res},1}$ over the range $[-\Delta, 0]$ for $-10 < e_3 < 10$ and with $\Delta = 1/8$. As seen from this figure, *if* e_3 is small (as often the case), *then* $J_{\text{res}}(D_{\text{res},1}, e_3) \approx J_{\text{res}}(V_{\text{res},1}, e_3)$. As a result, $D_{\text{res},1}$ can be exploited rather than $V_{\text{res},1}$ in (36)-(38). In addition, because the residue voltage, $V_{\text{res},1}$, is not available during the normal conversion operation, $D_{\text{res},1}$ is employed instead of $V_{\text{res},1}$ in (36)-(38) to detect the residue amplifier nonlinearity.

Since *ENE* is the difference between two CPDFs [see (36)-(38)], *ENE* cannot be practically utilized to measure e_3. Consequently, in order to actually work with probabilities, the *instantaneous nonlinear error*s are defined as following

$$INE_1 = INE_{1+} - INE_{1-}, \tag{41}$$
$$INE_2 = INE_{2+} - INE_{2-}. \tag{42}$$

In (41), INE_{1+} and INE_{1-} are implemented as

$$INE_{1+} = h\left((-\Delta + W) - D_{res,1}\middle| PN = +1\right), \tag{43}$$
$$INE_{1-} = h\left(W - D_{res,1}\middle| PN = -1\right). \tag{44}$$

It can be proved that the means $E[INE_{1+}]$ and $E[INE_{1-}]$ are also identical to the integration of ENE_+ and ENE_- within the range $-\Delta < D_{\text{res},1} < -\Delta + W$ as shown in Fig. 6. In other words, the mean $E[INE_1]$ is actually the comparison of $E[INE_{1+}]$ and $E[INE_{1-}]$. Additionally, INE_{2+} and INE_{2-} in (42) are implemented as

$$INE_{2+} = h\left(D_{res,1} + W\middle| PN = +1\right), \tag{45}$$
$$INE_{2-} = h\left(D_{res,1} - (\Delta - W)\middle| PN = -1\right). \tag{46}$$

It is worth mentioning that the means $E[INE_{2+}]$ and $E[INE_{2-}]$ are equal to the integration of ENE_+ and ENE_- over the interval $-W < D_{\text{res},1} < 0$. It follows from Fig. 6 that *ENE* is proportional to e_3 with *identical sign* inside the range $[-W, 0]$ of $D_{\text{res},1}$, and with *opposite sign* over the interval $[-\Delta, -\Delta + W]$ of $D_{\text{res},1}$. Hence, the opposite sign of $E[INE_1]$ is added to $E[INE_2]$ to define the *instantaneous nonlinear error* as following

$$INE = INE_2 - INE_1. \tag{47}$$

It is clear to show that the mean of the *instantaneous nonlinear error*, $E[INE]$, is related to e_3 as following

1) If $e_3 = 0$, then $E[INE_2] = 0$ (i.e., $E[INE_{2+}] = E[INE_{2-}]$), and $E[INE_1] = 0$ (i.e., $E[INE_{1+}] = E[INE_{1-}]$); *hence*, $E[INE] = 0$;
2) If $e_3 < 0$, then $E[INE_2] < 0$ (i.e., $E[INE_{2+}] < E[INE_{2-}]$), and $E[INE_1] > 0$ (i.e., $E[INE_{1+}] > E[INE_{1-}]$); *hence*, $E[INE] < 0$ (see Fig. 6(a));
3) If $e_3 > 0$, then $E[INE_2] > 0$ (i.e., $E[INE_{2+}] > E[INE_{2-}]$), and $E[INE_1] < 0$ (i.e., $E[INE_{1+}] < E[INE_{1-}]$); *hence*, $E[INE] > 0$ (see Fig. 6(b)).

Therefore, $E[INE]$ is roughly proportional to e_3, and it can be considered as the *estimated third-order nonlinear error*. Furthermore, *INE* is the noisy version of $E[INE]$. As a consequence, *INE* could be utilized in an adaptive search algorithm as an unbiased noisy version of $E[INE]$. In order to cancel the amplifier nonlinearity, an adaptive search algorithm is utilized to adjust α_3 such that $E[INE]$ is made equal to 0 [15], [26], [30]. The *update expression*is given by

$$\alpha_3(n+1) = \alpha_3(n) + \mu_3 INE(n) \tag{48}$$

where μ_3 denotes the update step-size [15], [19], [26], [30].

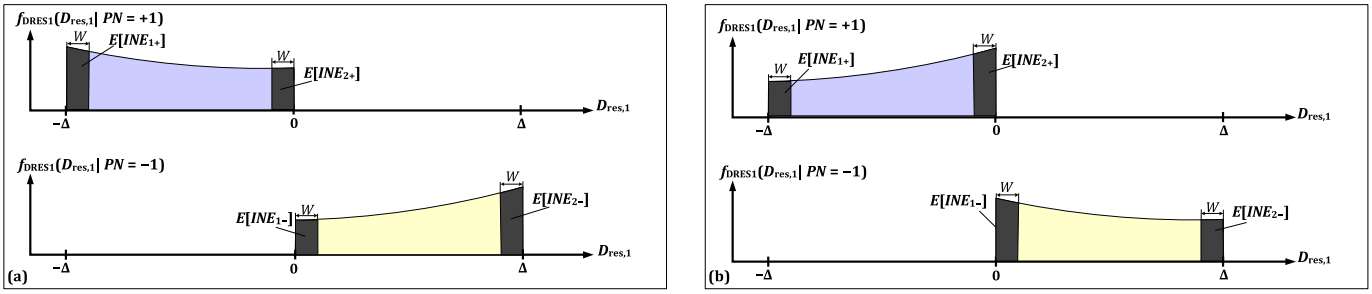

Fig. 6. Digitized residue distribution in the presence of the gain nonlinearity: (a) for $e_3 < 0$ and (b) for $e_3 > 0$.

It can be shown that *if* $W = \Delta/2$, *then* $E[INE] = E[IGE]$. Hence, for $W = \Delta/2$, the residue amplifier nonlinearity cannot be measured. Furthermore, the tracking time of the nonlinearity correction algorithm increases as $W \to 0$. Accordingly, the value of W should be *much less than* $\Delta/2$ to measure the residue amplifier nonlinearity. Nonetheless, it should not be *too small* due to the unacceptable long tracking time. In this design, W is chosen identical to $\Delta/10$.

C. Complete Structure and Implementation of Estimation Algorithm

Thus far, the residue amplifier third-order nonlinearity is measured and corrected under the assumption that the gain error is identical to 0. In fact, a large amount of the residue amplifier gain error can temporarily affect the proper adjustment of the nonlinearity estimation specifically at the beginning of the calibration procedure. This maladjustment may longer the convergence of the technique since after the convergence of the variable α_1 it can also take a long time for the variable α_3 to find its true value again. In order to alleviate this problem, a simple algorithm is exploited to estimate the magnitude of e_1. In this approach, the third-order nonlinearity estimation technique is performed *as long as* the absolute magnitude of e_1 is small enough such that the nonlinearity estimation method is not affected by the gain error. To estimate the absolute magnitude of e_1, *IGE* is averaged as:

$$e_{1-est}(b) = \frac{1}{L}\sum_{n=bL}^{b(L+1)-1} IGE(n) \tag{49}$$

where L and b represent the number of averaged samples and the time-index of the averaging operation, respectively. The absolute value of $e_{1-\text{est}}$ is updated every L samples, and then applied to the comparison operator, *Comp*(.). The output of *Comp*(.), F, is equal to 1 if the absolute magnitude of $e_{1-\text{est}}$ is less than a fixed threshold, e_{th}, and $F = 0$ otherwise. In this scheme, the nonlinearity estimation is performed provided that $F = 1$ (i.e., $|e_{1-\text{est}}| < e_{\text{th}}$) [see Fig. 7 and (50)]. The update expression of the third-order nonlinearity calibration is modified as

$$\alpha_3(n+1) = \alpha_3(n) + \mu_3 INE(n)\cdot F. \tag{50}$$

Fig. 7 shows a possible digital implementation of the proposed calibration technique. Since the *dc gain* of integrators is infinite and the steady-state values of α_1 and α_3 are also

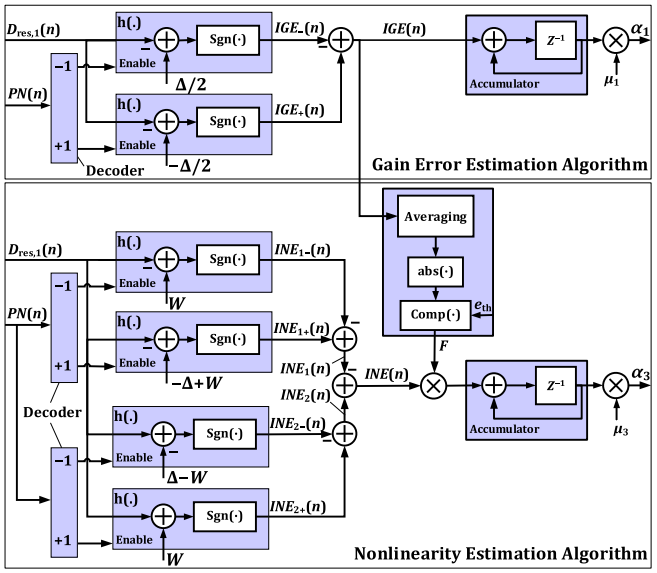

Fig. 7. Detailed block diagram of the proposed estimation algorithm.

finite, the integrators in the estimation loops force the mean of *IGE* and *INE* to zero. Consequently, after a number of iteration steps, *IGE* and *INE* approach zero, and α_1 and α_3 converge to their optimum values. In almost all adaptive algorithms utilized for digital calibration, the convergence time is inversely proportional to μ_1 and μ_3, while the steady-state error is proportional to μ_1 and μ_3. Therefore, the step-sizes should be chosen as a trade-off between the steady-state error and the convergence time [10], [11], [15], [19], [26].

Due to the key fact that the described estimation approach needs no multi-bit multiplier, it has actually an efficient implementation in hardware as seen from Fig. 7. The estimation block just has multi-bit adders. However, these adders can be implemented through digital comparison operators. Furthermore, the sign operator *sgn*(.) is realized by extracting the sign bit of its input. An accumulator is employed to implement each discrete-time integrator. In practice, the step-sizes μ_1 and μ_3 are powers of 2. As a consequence, they are actually implemented through simple bit shift operations. According to the extensive simulations, α_1 and α_3 are adjusted with enough resolution *in case* the resolution of the digitized residue is not 3 bits less than the desired resolution of the ADC.

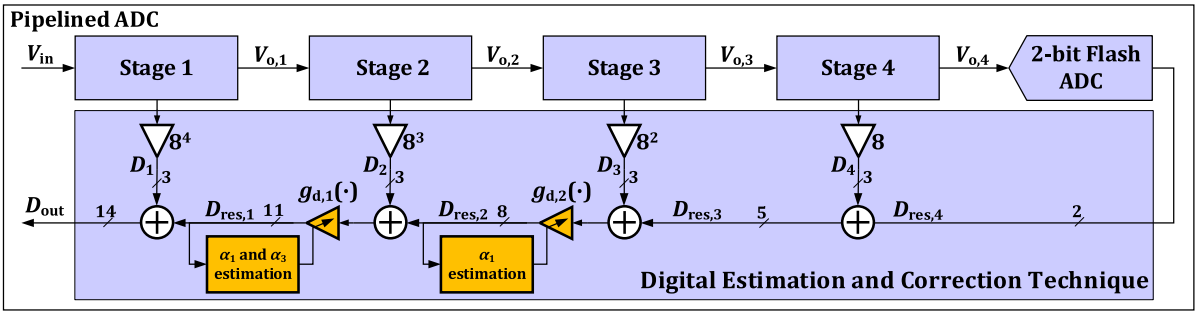

Fig. 8. The example pipelined ADC with the proposed calibration technique.

IV. Simulation Results and Discussions

Behavioral simulations in MATLAB/Simulink have been performed so as to validate the usefulness of the presented background calibration technique. In the following simulations, an example 12-bit pipelined ADC is chosen similar to [10]–[12]. As illustrated in Fig. 8, the ADC consists of four 3-bit stages and a 2-bit flash ADC as the last stage. Thus, all the first four stages must have a nominal gain of 8. It must be noted that the equivalent resolution of the third, fourth, and fifth stages is more than 6 bits. The second stage thus needs to enhance this resolution to 9 bits, and the first stage must also augment the resolution to 12 bits. For this reason, in the first stage, the gain error and third-order nonlinearity of the residue amplifier must be calibrated; nonetheless, the residue amplifier gain error of the second stage just needs to be considered and calibrated. To accommodate the SADC offsets, a redundancy of Δ is considered for the residue voltage in the first four stages [26]. Therefore, the first two stages have a 20-level (instead of 16-level) SADC with step-size of $\Delta = 1/10$ and a 21-level SDAC to accommodate the addition of the calibration signal, and the next two stages also have a 10-level (instead of 8-level) SADC with the step-size of $\Delta = 1/5$ and a 10-level SDAC. Furthermore, the following non-idealities are considered:

1) In the first four stages, the residue amplifier gains (β_1) and third-order nonlinearities (β_3) are chosen as independent Gaussian distributed random variables with means of 7.6 and -15.2, respectively, and standard deviations of 0.1 and 1, correspondingly.
2) In the first four stages, the SADC offset errors are also chosen randomly and separately with Gaussian distribution and standard deviation of 10% of the SADC step-size.
3) The SDAC mismatches are chosen as independent Gaussian distributed random variables with standard deviation of 0.1%, 0.2%, 0.3%, and 0.4% in the first, second, third, and fourth stages, respectively.
4) The flash ADC offset errors are chosen as independent Gaussian distributed random variables with standard deviation of 25%.

According to the above-mentioned imperfections, the ADC is simulated with the specific values of β_1, β_3, μ_1, and μ_3 listed in Table I. The following parameters W, L, and e_{th} are chosen identical to 0.0125, 1×10^4, and 0.0125, correspondingly. Moreover, the degree of the polynomial generator of the periodic *PN* generators is set to 10 in these simulations. Thermal noise is also considered in all the stages. The thermal noise sources restrict the signal-to-noise and distortion ratio (SNDR) to 80 dB. Besides, the SDAC imperfections decline the SNDR to 75 dB. Finally, the sampling frequency is set to one.

TABLE I
Coefficients of the Residue Amplifiers and Value of the Step-Sizes

	Stage 1	Stage 2	Stage 3	Stage 4
β_1	7.76	7.7	7.58	7.63
β_3	−12.8	−13.75	−14.95	−14.86
μ_1	2^{-10}	2^{-9}	Not used	Not used
μ_3	2^{-9}	Not used	Not used	Not used

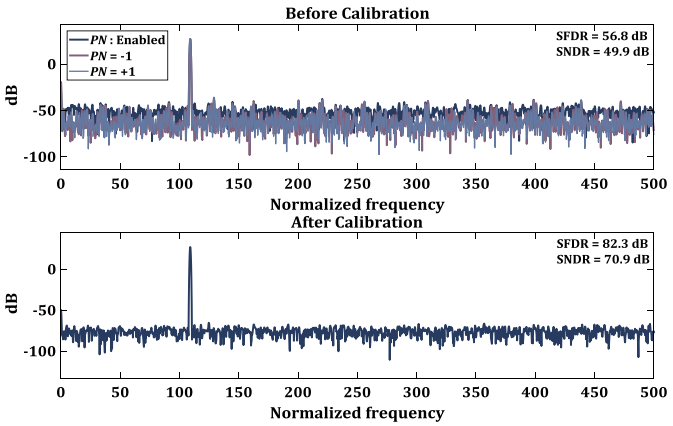

Fig. 9. PSDs of the digital output of the ADC before and after the calibration.

First of all, a full-scale sine-wave is exploited as the input test signal. Fig. 9 shows the power spectral densities (PSDs) of the digital output of the ADC before the calibration for three cases of $PN = +1$, $PN = -1$, and the pseudo-randomly generated *PN*, and also after the calibration. The SNDR is improved from 49.9 dB to 70.9 dB. Moreover, the spurious-free dynamic range (SFDR) is augmented from 56.8 dB to 82.3 dB. Fig. 10 illustrates the integral nonlinearity (INL) and differential nonlinearity (DNL) errors of the ADC before and after the calibration, respectively. In this figure, the digital output is truncated to 12 bits. After the calibration,

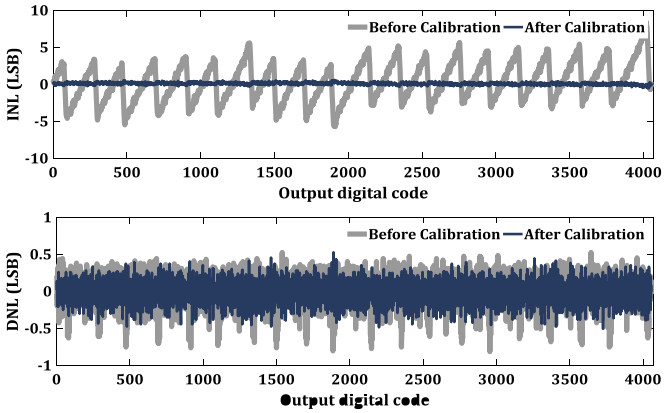

Fig. 10. INL and DNL errors of the ADC before and after the calibration.

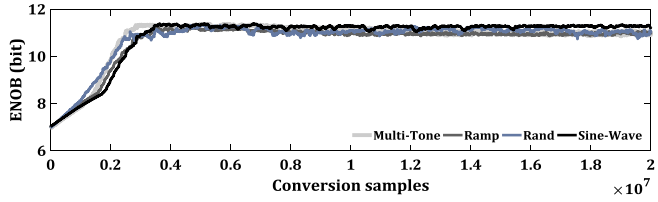

Fig. 11. Convergence of the ENOB with different input signals.

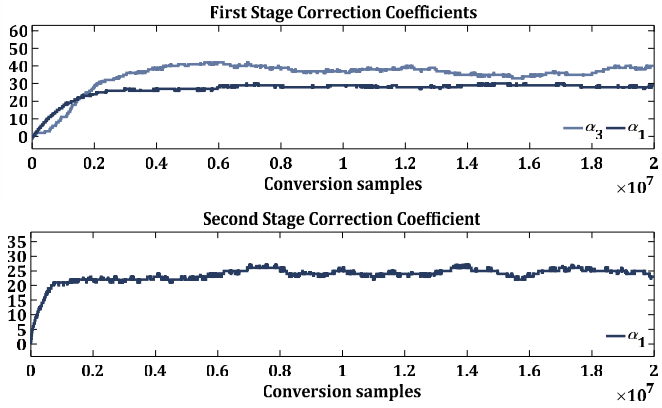

Fig. 12. Convergence of the coefficients of g_{d1} and g_{d2}.

the INL/DNL errors are decreased from more than 10 LSBs to less than 1 LSB.

Depicted in Fig. 11 is the convergence of the effective number of bits (ENOB) during the calibration with the following input signals: a sinusoidal with a frequency of 0.1091 Hz, random, and multi-tone sinusoidal. The multi-tone sinusoidal also consists of the frequencies 0.0994 Hz, 0.1956 Hz, 0.2947 Hz, and 0.3909 Hz. Moreover, Fig. 12 shows the convergence of the correction coefficients of the first two stages with a sinusoidal input signal. The ENOB reaches 11.2 bits after approximately 5×10^6 conversions with the sinusoidal input signal. For an ADC running at 200 MS/s, this translates to about 25 ms.

In order to show the digitized residue empirical distribution before and after the calibration, a ramp test-signal of length

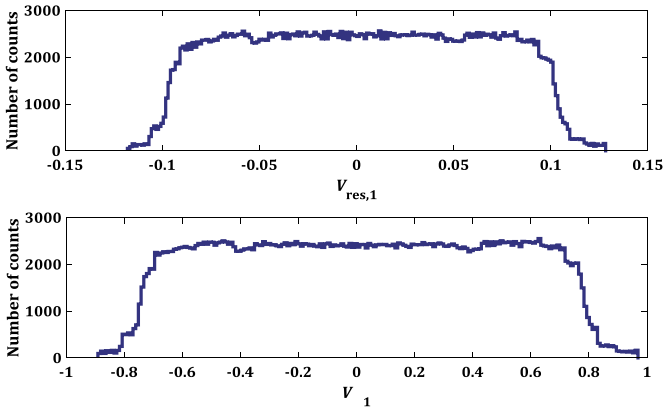

Fig. 13. Histogram of the residue voltage and the output voltage of the first stage.

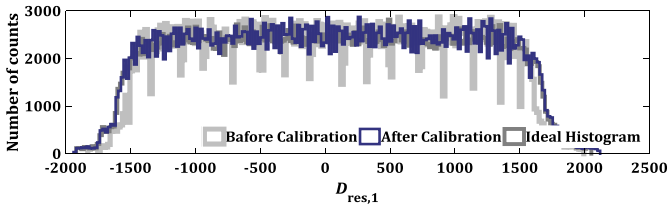

Fig. 14. Histogram of the digitized residue of the first stage before and after the calibration.

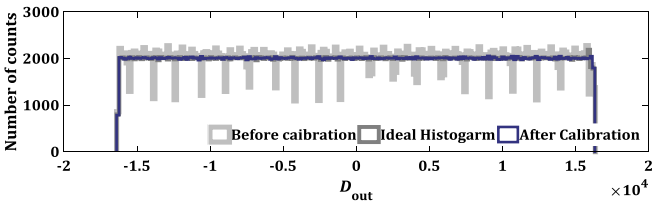

Fig. 15. Histogram of the digital output of the ADC before and after the calibration.

4×10^6 is applied to the ADC. The test-signal is uniformly distributed over the range $[-1, 1]$. The histogram of the residue and output voltages of the first stage are depicted in Fig. 13. The digitized residue histogram before and after the calibration and also the desired histogram are demonstrated in Fig. 14. In the perfect case, the digitized residue histogram needs to be identical to the desired histogram (which is the digital format of the histogram of the residue voltage), while, in the presence of the residue amplifier non-idealities, the shape of the digitized residue distribution deviates from the desired distribution as seen from Fig. 14. After the calibration, the digitized residue distribution approaches its ideal case. Furthermore, the distribution of the digital output histogram is approximately identical to its desired distribution after the calibration as shown in Fig. 15.

Finally, the impact of the elements mismatch of the SDACs on the ENOB is regarded. The standard deviations of the elements mismatch of the SDACs in all the stages are considered identical. Also, the mismatches are then removed in digital domain by the prior knowledge of them. Fig. 16 shows

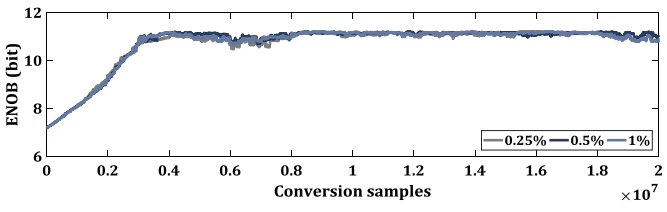

Fig. 16. Convergence of the ENOB with different standard deviations of the elements mismatch in the SDACs.

the convergence of the ENOB for the standard deviations of 0.25%, 0.5% and 1%. As seen from the figure, the proposed method is almost insensitive to the elements mismatch of the SDACs.

A. Comparison to Previous Techniques

The concept of the presented estimation approach is different from the statistics-based estimation techniques in [12]–[15]. The described scheme directly operates on the PDF of the digitized residue, and it exploits the deviations of the digitized residue probability distribution from its corresponding residue voltage probability distribution in order to estimate and correct the residue amplifier imperfections. The proposed algorithm eliminates the conversion errors by forcing the digitized residue PDF to be identical to its corresponding residue voltage PDF. In contrast, the estimation technique of [12] ignores the deviations of the PDF of the digitized residue, and it is based on measuring and correcting the *digitized residue distance* for two modes of the calibration signal. The digitized residue distances corresponding to two input voltages are analyzed and corrected in order to cancel the conversion errors. To extract the digitized residue distance corresponding to a specific input, a single counter estimates the *cumulative distribution function* (CDF) of the digitized residue corresponding to the given digitized residue for $PN = +1$ and an array of counters estimates the CDFs of the digitized residue for $PN = -1$ corresponding to several digitized residue values. The CDF of the single counter is then compared with CDF of the counters in the array. From the closest match, the digitized residue distance is measured [11], [12]. The method in [12] converges after approximately 50×10^6 conversion operations for an SNDR of 70.9 dB, whereas the introduced estimation algorithm requires roughly 5×10^6 conversion samples for convergence. Therefore, the presented technique has a faster convergence rate by more than 10 times.

The element mismatch calibration in [26] exploits the statistics of the quantization error to continuously and digitally compensate for the mismatch among the elements of the SDAC. Although the method of [26] is proposed so as to eliminate the SDAC mismatch, it is capable of correcting the residue amplifier gain error. In the presented method, the PDF of the digitized residue is estimated and altered utilizing the center points (i.e., $\pm\Delta/2$) to mitigate the gain error, while the technique of [26] does not alter the PDF of the digitized residue, and it measures the mismatch of the SDAC by tuning the center points (i.e., $\pm\Delta/2$) for each of the SDAC elements. Besides, the calibration method in [15] exploits an LMS algorithm to eliminate the gain, second-, and third-order nonlinearities of the residue amplifier. However, it can consume considerable die area for implementing of the required multipliers. The proposed technique operates with simpler digital circuitry and without the need for any multi-bit multiplier despite the fact that it cannot correct the second-order nonlinearity similar to [13] and [14].

The advantage of the introduced estimation algorithm is that it needs only two accumulators to implement the discrete-time integrators [see Fig. 7], and the values of μ_1 and μ_3 must also be reduced by a factor of 4 if the ADC resolution is increased by one bit. In contrast, the estimation technique in [12] requires an array of counters and the number of counters must also be doubled for each additional bit in the ADC resolution [11]. It is worth mentioning that the described technique operates without the need for any multi-bit multiplier similar to [12]–[15], while the algorithms in [10], [11], and [15] require several multi-bit multipliers. However, the multi-bit multipliers of the scheme in [15] operate at a lower rate than the ADC sampling rate. Furthermore, the relative advantage of the techniques in [10]–[12] and [15] over the proposed algorithm is that these methods can detect and correct the second-order nonlinearity error of the residue amplifier.

Additionally, the performance of the pipelined ADC is limited by the residue amplifier nonlinearity [10]–[15] in high-resolution applications. The presented scheme corrects the residue amplifier third-order nonlinearity, while the technique of [16] cannot mitigate the third-order error introduced by the residue amplifier nonlinearity. The methods of [13] and [14] directly utilize the input signal distribution for their operation; thus, they strictly depend on input signal statistics. In contrast, the introduced method operates on the digitized residue similar to [12] and [15]. The comparison of the presented technique with similar methods is also summarized in Table II. In this table, the power dissipation of each gate is considered as 16 nW/gate/MHz in a 0.18-μm CMOS technology [31]. The order of the power consumptions is obtained using the required adders, multipliers, and registers with the word length of 16 bits at the frequency of 200 MHz.

B. Input Signal Limitations

The described algorithm has restriction on the statistics of the input signal similar to almost all digital calibration techniques. Nevertheless, the proposed technique works well with sinusoidal, multi-tone sine-wave, and Gaussian distributed input signals. Hence, it can be argued that the introduced scheme operates well in most communication applications. Although the proposed method manifest its best performance under the uniformly distributed SADC quantization error, the presented algorithm works well *as long as* the PDF of the SADC quantization error is continuously distributed and it is not too small over the interval $[-\Delta/2,\ \Delta/2]$. Furthermore, this algorithm works well *providing that* the residue voltage exercises the whole range $[-\Delta/2,\ \Delta/2]$. It is worth mentioning that the presented method can be simply extended to evaluate the digitized residue range and to prevent the maladjustment

TABLE II
COMPARISON WITH SIMILAR TECHNIQUES

	This work	[10]	[11]	[12]	[13], [14]	[15]
Convergence Samples	5×10^6	10^9	4×10^6	50×10^6	10^6	5×10^6
Input Signal Distribution	Moderate	Low	Low	Moderate	High	Moderate
Digital Power Consumption*	$O(1)$	$O(10)$	$O(10)$	$O(10)$	$O(0.1)$	$O(10)$
Digital Complexity#	Low	Moderate	High	Moderate	Low	High
Extra Analog Complexity	Moderate	High	Moderate	Moderate	Low	Moderate
Second-Order Error Correction	×	✓	✓	✓	×	✓

* O(x) denotes the order of the power consumption in mW.
# **High**: the need for multi-bit multipliers; **Moderate**: the need for array of counters or integrators; **Low**: without the need for any multi-bit multiplier and/or array of counters.

of the correction coefficients *in case* the digitized residue does not exercise the whole range $[-\Delta/2,\ \Delta/2]$.

C. Residue Amplifier Nonlinearities

In wideband amplifiers, *memory-effects* are negligible [2], [10], [12]–[15]. Although the proposed calibration technique cannot measure and correct the *offset* and *even-order* errors similar to [13] and [14], the proposed method is not susceptible to these errors, and these error sources are actually suppressed and can be practically neglected due to the fully-differential nature of the residue amplifier [1]–[6], [13], [14]. In addition, most communication systems are not sensitive to the offset of the ADCs [10]–[12], [15], [16]. Moreover, the residue amplifier offset can also be removed through a separate offset cancellation mechanism, e.g., [32]. It is worth mentioning that other methods (e.g., [2], [10], [12], [17]) must be utilized in case the second-order nonlinearity limits the ADC resolution to less than the desired amount.

D. Imperfections of SADC and SDAC

The offsets of the SADC alter the distribution of the quantization error. However, these offsets don't affect the injected amplitude of the *CS* signal for both sates of *PN*. For this reason, the quantization error is just shifted via the *CS* signal in the presence of the offsets, and the mean $E[IGE]$ is also eliminated *providing that* the gain error is removed. Afterwards, with the injection of the calibration signal, the distribution of the residue voltage signal is ideally restricted to $[-\Delta,\ \Delta]$, and the output voltage of the stage is also limited to $[-\beta_1\times\Delta,\ \beta_1\times\Delta]$. For this reason, the headroom for tolerating the offsets is bounded to $\pm(1-\beta_1\times\Delta)$. Consequently, the maximum bearable offset is restricted to $\pm(1-\beta_1\times\Delta)/\beta_1$ as well. In the simulations, the standard deviation of the offsets is considered 3 times less than the maximum bearable offset (i.e., $(1-\beta_1\times\Delta)/3\beta_1$). Moreover, a separate mechanism can be utilized to effectively reduce the standard deviation of the offsets (e.g., [5], [32]).

Additionally, based on extensive simulation results, the described method is not susceptible to the imperfections of the SDAC, and the element mismatch of the SDAC does not affect the proper adjustment of the digital correction coefficients. Nevertheless, a separate algorithm (e.g., [26], [29]) needs to be utilized concurrently with the proposed method if the ADC resolution is also restricted by the SDAC non-idealities. Similar to the methods of [10]–[12], the presented technique is suitable for multi-bit stages (e.g., for stage resolutions equal or more than 2 bits).

V. CONCLUSION

A digital background residue amplifier calibration for pipelined ADCs has been proposed. This scheme can mitigate the conversion errors introduced by the residue amplifier non-idealities. Since the proposed estimation method needs no multi-bit multiplier, it has an efficient hardware implementation. The described scheme can be used to reduce the power of pipelined ADCs and/or increase the conversion rate.

APPENDIX A

In this appendix, the means of the operators $\mathrm{sgn}(x)$ and $h(x|PN=m)$ are derived. Because the sign operator $\mathrm{sgn}(x)=2$ for $x\geq 0$ and $\mathrm{sgn}(x)=0$ otherwise, it is obvious to prove that

$$P\left(\mathrm{sgn}(x)=2\right)=P\left(0\leq x\right), \tag{51}$$

$$P\left(\mathrm{sgn}(x)=0\right)=1-P\left(0\leq x\right). \tag{52}$$

Consequently, the mean of $\mathrm{sgn}(x)$ is identical to

$$E\left(\mathrm{sgn}(x)\right)=2P\left(0\leq x\right). \tag{53}$$

In addition, since the operator $h(x|PN=m)$ is disabled for $PN\neq m$; therefore, for the case $PN\neq m$, we have

$$P\left(h\left(x|\,PN\neq m\right)=0\right)=P\left(PN\neq m\right). \tag{54}$$

For the state $PN=m$, the operator $h(x|PN=m)$ is enabled; hence, from the basic probability, (51), and (52), it is evident to verify that

$$P\left(h\left(x|\,PN=m\right)=2\right)=P\left(PN=m\right)\times P\left(0\leq x|\,PN=m\right), \tag{55}$$

$$P\left(h\left(x|\,PN=m\right)=0\right)=P\left(PN=m\right)\times\left[1-P\left(0\leq x|\,PN=m\right)\right]. \tag{56}$$

From (23), (55), and (56), it is clear to show that the mean of $h(x|PN=m)$ is equal to

$$E\left(h\left(x\right|PN=m\right))=2P\left(PN=m\right)\times P\left(0\le x\right|PN=m\right) \tag{57}$$

APPENDIX B

This appendix derives (33) from (32). Substituting (32) into (13), and using (27) and the fact that $f_{\mathrm{DRES1}}(V_{\mathrm{res},1}|PN=+1)$ is distributed over the range $[-\Delta(1+e_1), 0]$, $E[IGE]$ can be expressed as

$$\begin{aligned}E\left[IGE\right]=&\int_{-(1+e_1)\Delta}^{-\Delta/2} f_{DRES1}\left(D_{res,1}\right|PN=+1\right)dD_{res,1}\\&-\int_{0}^{\Delta/2} f_{DRES1}\left(D_{res,1}-(1+e_1)\,\Delta\right|PN=+1\right)\\&\times dD_{res,1}.\end{aligned} \tag{58}$$

Applying the variable substitution $D'=D_{\mathrm{res},1}-(1+e_1)\Delta$ into the second integral, $E[IGE]$ can be represented by

$$\begin{aligned}E\left[IGE\right]=&\int_{-(1+e_1)\Delta}^{-\Delta/2} f_{DRES1}\left(D_{res,1}\right|PN=+1\right)dD_{res,1}\\&-\int_{-(1+e_1)\Delta}^{-(1/2+e_1)\Delta} f_{DRES1}\left(D'\right|PN=+1\right)dD'.\end{aligned} \tag{59}$$

Combining the two integrals in (59) results in

$$E\left[IGE\right]=\int_{-(1/2+e_1)\Delta}^{-\Delta/2} f_{DRES1}\left(D_{res,1}\right|PN=+1\right)dD_{res,1}. \tag{60}$$

APPENDIX C

In the absence of the gain error, it follows from the basic probability [15], and (17) that the digitized residue CPDFs are given by

$$f_{DRES1}\left(V_{res,1}\right|PN=+1\right)=\frac{f_{VRES1}\left(V_{res,1}\right|PN=+1\right)}{\left|1+3e_3V_{res,1}^2\right|}, \tag{61}$$

$$f_{DRES1}\left(V_{res,1}\right|PN=-1\right)=\frac{f_{VRES1}\left(V_{res,1}\right|PN=-1\right)}{\left|1+3e_3V_{res,1}^2\right|}. \tag{62}$$

It follows from (36)-(38), (61), and (62) that *ENE* is represented by

$$\begin{aligned}ENE=&\frac{f_{VRES1}\left(V_{res,1}\right|PN=+1\right)}{\left|1+3e_3V_{res,1}^2\right|}\\&-\frac{f_{VRES1}\left(V_{res,1}+\Delta\right|PN=-1\right)}{\left|1+3e_3\left(V_{res,1}+\Delta\right)^2\right|}.\end{aligned} \tag{63}$$

Using Property 1 for $f_{\mathrm{VRES1}}(V_{\mathrm{res},1}+\Delta|PN=-1)$, *ENE* can be expressed as following

$$\begin{aligned}ENE=&\left\{\frac{1}{\left|1+3e_3V_{res,1}^2\right|}-\frac{1}{\left|1+3e_3\left(V_{res,1}+\Delta\right)^2\right|}\right\}\\&\times f_{VRES1}\left(V_{res,1}\right|PN=+1\right),\end{aligned} \tag{64}$$

inside the interval $-\Delta < V_{\mathrm{res},1} < 0$.

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