Digital Blind Background Calibration of Imperfections in Time-Interleaved ADCs

Hamidreza Mafi, Mostafa Yargholi, and Mohammad Yavari, *Member, IEEE*

***Abstract*— This paper presents a digital blind background calibration technique of imperfections in time-interleaved analog-to-digital converters (TI-ADCs). The proposed technique directly operates on the statistics of the input signal to continuously estimate and eliminate the conversion errors resulted from offset, gain, and timing mismatch. Behavioral simulations are presented for a 4-channel 10-bit TI-ADC in order to verify the effectiveness of the proposed method. The signal-to-noise-and-distortion ratio (SNDR) is enhanced from 33.7 dB to more than 61 dB using the introduced calibration technique. This calibration method converges after roughly 4×10^6 conversions.**

***Index Terms*— Adaptive systems, digital background calibration, digital signal processing, time-interleaved analog-to-digital conversion.**

I. Introduction

TIME-interleaved analog-to-digital converters (TI-ADCs) have been proposed to achieve the conversion rates beyond limits of a given IC technology [1], [2]. The TI-ADC is also popular in high-speed digital communication systems [3], [4]. A TI-ADC is comprised of a set of parallel ADCs, referred to as *sub-ADCs* [4], [5]. In the design of high-resolution TI-ADCs (i.e., TI-ADCs with a resolution more than 5 bits), performance degradation arising from the TI-ADC non-idealities, consisting of *offset*, *gain*, and *timing* mismatch among the sub-ADCs, needs to be considered, measured, and mitigated [2], [5]. In the TI-ADC, the mismatch between the sub-ADCs is mostly unknown since the imperfections of the sub-ADCs are introduced during fabrication process and they depend on temperature variations and voltage drift. Consequently, the mismatch among the sub-ADCs must be *continuously* tracked and canceled for the performance enhancement of a TI-ADC.

Several calibration schemes have been developed for the compensation and cancellation of the mismatch in TI-ADCs [1]–[16]. Digital background calibration approaches are capable of extracting and correcting the ADC non-idealities in the background without interrupting its operation. So, these schemes are extensively employed in order to alleviate the severe effects of the offset [5], [12], gain [5], timing [1]–[11], and frequency response mismatch [13]–[16] during the normal data conversion of the TI-ADC. A digital calibration technique is typically comprised of *estimation* and *correction* blocks [1], [2]. The aim of the estimation block is to digitally extract and track the imperfections in the TI-ADC. Besides, the correction block cancels the non-idealities in digital or analog domains. It is often preferred to mitigate the impact of the offset and gain mismatch between the channels in digital domain [5], [12], and to compensate the timing mismatch in analog domain [1], [2]. Nonetheless, the timing mismatch can be corrected in digital domain at the expense of complex digital circuits [4], [5]. It should be noted that most of the timing mismatch calibration methods (e.g., [1], [2]) operate well provided that the offset and gain mismatch among the sub-ADCs are calibrated firstly.

This paper presents a digital blind background calibration of the imperfections in TI-ADCs. The proposed technique continuously measures and digitally removes the errors arising from the offset, gain, and timing mismatch without interrupting the data conversion of the TI-ADC. This scheme *directly* operates on the statistics of the input signal so as to *indirectly* mitigate the non-idealities in the TI-ADC. In the presented method, the offset and gain mismatch are digitally compensated, and the timing mismatch is cancelled in analog domain as well.

The remainder of the paper is structured as follows. Section II briefly reviews the structure of the TI-ADC. Section III presents the proposed digital background calibration technique. Simulation results are provided in Section IV. Discussions are presented in Section V. Finally, Section VI concludes the paper.

II. Architecture of Time-Interleaved ADCs

This section concisely describes the traditional structure of the TI-ADC, provides the essential frameworks, and introduces the statistical features required for the proposed calibration technique. In this paper, all analog and digital signals are scaled to the reference voltage for presentation convenience; as a consequence, all signals are supposed to be distributed within the range of $[-1, 1]$. Moreover, it is assumed that the input signal *probability density function* (PDF) is continuous and non-zero (as often the case). Therefore, the PDF of the TI-ADC input signal, $p_{\mathrm{VIN}}(V_{\mathrm{in}})$, is restricted to the range of $[-1, 1]$. Depicted in Fig. 1 is a TI-ADC, consisting of M sub-ADCs and operating at f_{s} ($T_{\mathrm{s}} = 1/f_{\mathrm{s}}$). The ith sub-ADC ($i = 1, \ldots, M$) ideally samples the input signal at $f_{\mathrm{c}} = f_{\mathrm{s}}/M$

Manuscript received July 14, 2016; revised November 8, 2016 and December 26, 2016; accepted December 31, 2016. Date of publication January 30, 2017; date of current version May 25, 2017. This paper was recommended by Associate Editor L. Hernandez.

H. Mafi and M. Yargholi are with the Electrical and Computer Engineering Department, University of Zanjan, Zanjan, Iran (e-mail: h.mafi@znu.ac.ir; yargholi@znu.ac.ir).

M. Yavari is with the Integrated Circuits Design Laboratory, Department of Electrical Engineering, Amirkabir University of Technology (Tehran Polytechnic), Tehran 15914, Iran (e-mail: myavari@aut.ac.ir).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TCSI.2017.2647758

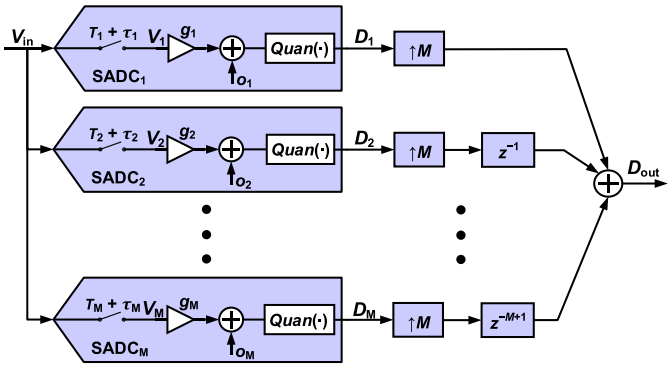

Fig. 1. Simplified architecture of a TI-ADC.

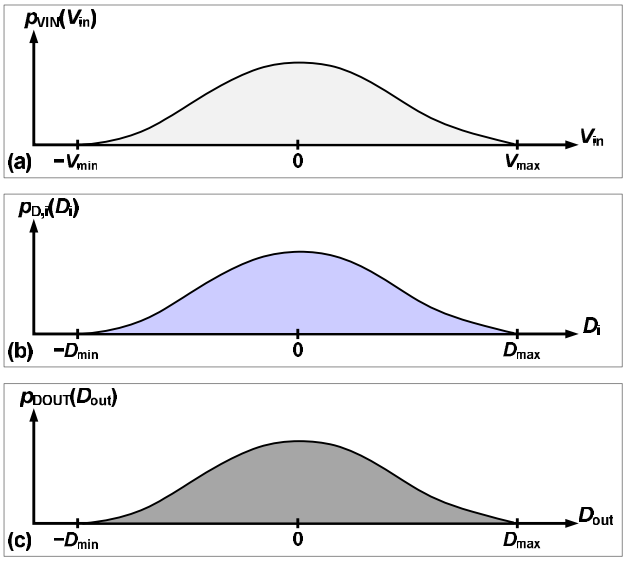

Fig. 2. Example PDF of (a) the input signal, (b) the digital output of the ith sub-ADC, and (c) the digital output.

with a timing delay of $T_i = (M - i)/f_s$ to produce the ith sampled signal, V_i [17]. Nevertheless, the ith sub-ADC actually samples the input signal with a timing error of τ_i.

To begin with, an interesting property from the basic probability theory is briefly stated. Since each sub-ADC samples the same input signal, the signals V_i $(i = 1, \ldots, M)$ are resulted of the same source. Accordingly, it follows from the basic probability theory that the PDF of all the sampled signals, $p_{V,i}(V_i)$ $(i = 1, \ldots, M)$, are the same and identical to the input signal PDF [18], [19], expressed as:

$$p_{V,i}(V_i) = p_{VIN}(V_{in}), \quad i = 1, \ldots, M. \tag{1}$$

Fig. 2(a) depicts a typical example of the input signal PDF. Fig. 2(b) illustrates the PDF of the sampled signal in the ith sub-ADC corresponding to the example PDF in Fig. 2(a).

Additionally, the difference between two consecutive samples of the input signal, $V_{diff}(t) = V_{in}(t) - V_{in}(t - \Delta)$, can convey information about the time difference Δ [1]. For this reason, an interesting feature of the PDF $p_{DIF}(V_{diff}(t))$ will be shown. The PDF of the difference signal $p_{DIF}(V_{diff}(t))$ is an impulse at zero if $\Delta = 0$, as depicted in Fig. 3(a). Besides, the distribution of $p_{DIF}(V_{diff}(t))$ becomes wider and wider as Δ increases more and more. For a special value of the time

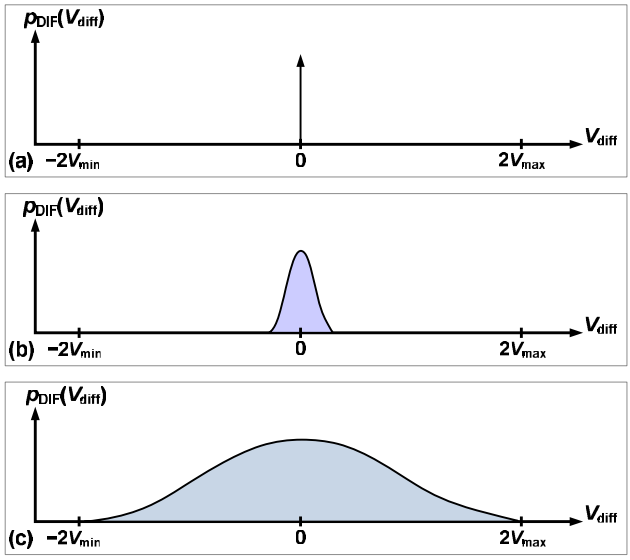

Fig. 3. Example PDF of the difference signal for (a) $\Delta = 0$, (b) $0 < \Delta < \Delta_{ind}$, and (c) $\Delta = \Delta_{ind}$.

difference, Δ_{ind}, $V_{in}(t)$ and $V_{in}(t - \Delta_{ind})$ become independent from each other. For $\Delta = \Delta_{ind}$, $p_{DIF}(V_{diff}(t))$ is equal to the convolution of the input signal PDF with itself. The special value of Δ for which $V_{in}(t)$ and $V_{in}(t-\Delta)$ become independent is given by [19]:

$$\begin{aligned} &\Delta_{ind} > T_s, \quad BW < f_s/2, \\ &\Delta_{ind} = T_s, \quad BW = f_s/2, \\ &\Delta_{ind} < T_s, \quad BW > f_s/2, \end{aligned} \tag{2}$$

where BW stands for the bandwidth of the input signal. Typical examples of $p_{DIF}(V_{diff}(t))$ for $0 < \Delta < \Delta_{ind}$ and $\Delta = \Delta_{ind}$, are depicted in Fig. 3(b) and 3(c), respectively. As shown in plots of Fig. 3, the spread of $p_{DIF}(V_{diff}(t))$ is strictly proportional to the time difference Δ for $\Delta < \Delta_{ind}$. Furthermore, it is assumed that BW is limited to the Nyquist rate.

Afterwards, the signal V_i $(i = 1, \ldots, M)$ is digitized by the quantization block, *Quan*(.), to a B-bit digital output. In the ith sub-ADC, the sampled signal is digitized as [17]:

$$D_i = g_i V_i + o_i + \varepsilon_{qi} \quad i = 1, \ldots, M \tag{3}$$

where D_i and ε_{qi} stand for the *digital output* and *quantization error* of the ith sub-ADC, respectively. The terms o_i, g_i, and τ_i are the offset, gain, and timing errors in the ith sub-ADC, correspondingly. Besides, g_i, o_i, and τ_i would be ideally identical to 1, 0, and 0, respectively. It is worth mentioning that the PDF distribution range of the ith sub-ADC quantization error, $p_{EQI}(\varepsilon_{qi})$, with a B-bit resolution is given by:

$$-\Delta_{QS}/2 < \varepsilon_{qi} < \Delta_{QS}/2 \quad i = 1, \ldots, M \tag{4}$$

where Δ_{QS} represents the ith sub-ADC *step size* equal to $\Delta_{QS} = 2/2^B$ [18]. In the remainder of the paper, the quantization error of sub-ADCs is neglected for the presentation simplicity. Nevertheless, this simplification doesn't affect the applicability of the proposed calibration method in Section III.

Finally, as depicted in Fig. 1, the digital outputs are up-sampled by a factor of M, and added together in order to generate the TI-ADC digital output [17] as following:

$$D_{out}(n) = \sum_{i=1}^{M} D_i(n/M)\, z^{-i+1}. \quad (5)$$

In (5), $D_i(n/M)$ is equal to 0 if n is not a multiple of M, and n also denotes the discrete time index. In the absence of the mismatch among the sub-ADCs, it is evident that the probability distribution of the digital output of the TI-ADC, D_{out}, is equal to the digital output PDF of each sub-ADC and the input signal PDF as shown in Fig. 2(c).

In the digital output of a TI-ADC, the offset, gain, and timing mismatch manifest themselves by adding a repeating sequence pattern, modulating the ideal TI-ADC digital output, and generating a phase modulation of the ideal digital output, respectively [2], [5], [17]. Consequently, any deviation of these parameters from their ideal cases leads to the performance degradation in the TI-ADC. The main goal of the background calibration is to estimate and correct the TI-ADC imperfections during its normal operation as the sources of the mismatch are unknown in nature and dependent on the variations of the ambient temperature, reference voltage drift, and aging [2], [5].

III. Proposed Digital Background Calibration Technique

This section presents the proposed digital background measurement and cancellation of the mismatch among the sub-ADCs based on a statistics-based estimation approach. The presented scheme *directly* operates on the digital output PDF of the sub-ADCs in order to *indirectly* estimate and correct the mismatch between the sub-ADCs.

A. Statistics-Based Estimation Mechanism

In this sub-section, the required probabilistic mechanism for the estimation and correction of the offset and gain mismatch in the TI-ADC is described. For the time being, the timing mismatch is ignored since it doesn't alter the PDF shape of the digital output of the sub-ADCs. From the basic probability theory, it is evident that the presence of the offset and gain errors causes the digital output PDF of the sub-ADCs to be [18]–[20]

$$p_{D,i}(D_i) = p_{V,i}(D_i/g_i - o_i)/g_i, \quad i = 1, \ldots, M. \quad (6)$$

Fig. 4 demonstrates the example PDFs of the first and ith sub-ADCs corresponding to the input signal PDF shown in Fig. 2(a) in the presence of the offset and gain mismatch. Accordingly, the offset and gain mismatch also result in *the mismatch among the digital output PDF of the sub-ADCs*. For this reason, this key feature can be utilized to *indirectly* detect the offset and gain mismatch between the sub-ADCs in digital domain. Moreover, the offset and gain mismatch among the sub-ADCs are removed *on condition that* the digital output probability distribution of all the sub-ADCs are made equal. Because the exact PDF of the TI-ADC input signal is not actually available, the digital output PDF of one of the sub-ADCs can be considered as the reference PDF rather than the input signal PDF. In turn, the TI-ADC digital output exhibits just offset and gain errors identical to the offset and gain errors of the reference sub-ADC, after applying this approach.

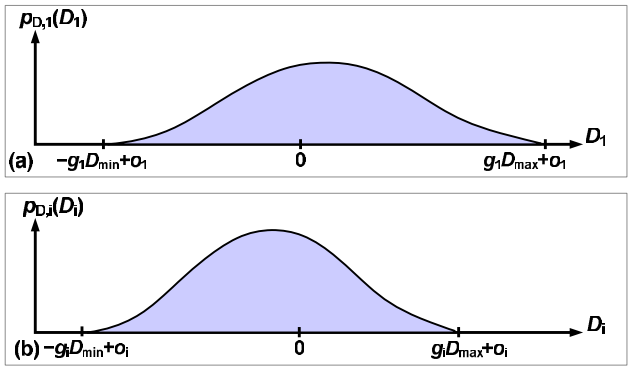

Fig. 4. (a) Digital output PDF of the first sub-ADC and (b) the digital output PDF of the ith sub-ADC.

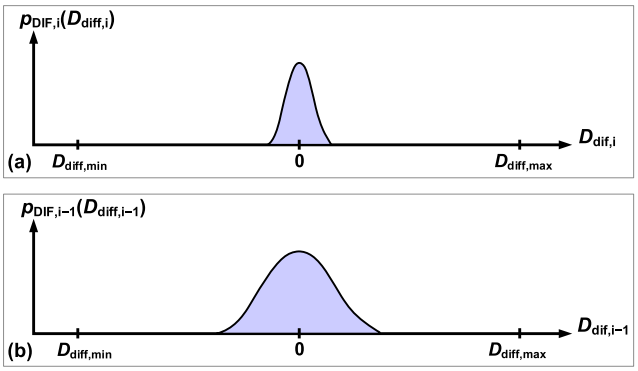

Fig. 5. (a) PDF of ith digital difference and (b) the PDF of $(i-1)$th digital difference.

As explained earlier, the PDF distribution width of the difference input signal proportionally varies with respect to the time difference between the two samples of the input signal. In addition, the digital output of each sub-ADC is just the digital representation of its sampled signal in the absence of the offset and gain mismatch. Consequently, the digital signals D_{i} and $D_{\text{i}-1}$ are ideally the successive outcomes of the input signal with a time difference of $\Delta = T_{\text{s}}$. The time difference between $D_{\text{i}-1}$ and D_{i} is practically more (or less) than the time difference among D_{i} and $D_{\text{i}+1}$ *in case* the ith timing mismatch is more (or less) than zero.

The digital differences, $D_{\text{dif,i}} = D_{\text{i}} - D_{\text{i}+1}$ $(i = 1, \ldots, M-1)$ and $D_{\text{dif,M}} = z^{-1}D_{\text{M}} - D_1$, can be utilized to measure and correct the timing errors [1]. Shown in Fig. 5 are the PDF examples of $D_{\text{dif,i}}$ and $D_{\text{dif,i}-1}$ in the presence of the timing mismatch. As seen from the figure, the PDFs $p_{\text{DIF,i}}(D_{\text{dif,i}})$ and $p_{\text{DIF,i}-1}(D_{\text{dif,i}-1})$ are not equally distributed in this case. In turn, the impact of the timing errors can be extracted and minimized through the PDFs of the digital differences.

In reality, the use of the PDF distribution is not feasible. Nonetheless, *cumulative distribution functions* (*CDFs*) are

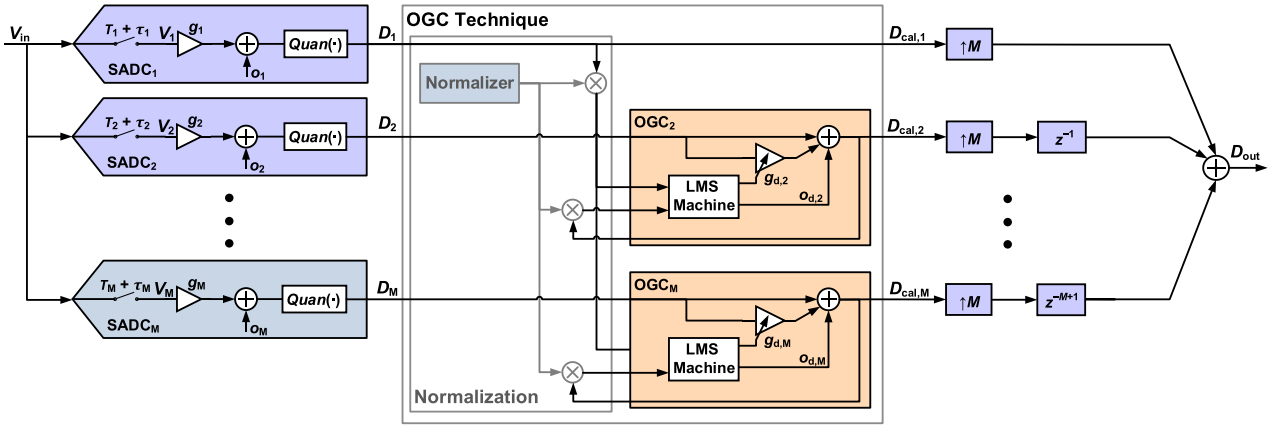

Fig. 6. Block diagram of the proposed offset and gain mismatch calibration technique.

practically utilized instead of the required PDFs for the mismatch extraction. The CDF of a variable is given by

$$P\left(D_{th}\right)=\int_{ll}^{D_{th}} p\left(D\right)dD \tag{7}$$

where ll denotes the lowest limit of the PDF $p(D_{\rm th})$. As evident from (7), the two CDFs are the same *if and only if* their respective PDFs are identical. For this reason, a given PDF can be actually replaced by its respective CDF.

B. Proposed Statistics-Based Calibration Technique

This sub-section introduces a digital calibration technique for the TI-ADC imperfections based on the probabilistic features in Section III-A. Since the presented scheme doesn't require any calibration signal, this calibration technique utilizes a blind *least-mean-square* (*LMS*) algorithm.

First of all, the proposed *offset and gain calibration* (*OGC*) method is presented as illustrated in Fig. 6. The digital outputs are firstly scaled to [−1, 1] by a normalizer [see Section III-D]. In the OGC scheme, the digital output CDF of the first sub-ADC is chosen as the reference CDF. Therefore, the calibrated digital output CDF of the ith sub-ADC ($i = 2, \ldots, M$) is equalized with the calibrated digital output CDF of the first sub-ADC. As depicted in Fig. 6, the offset and gain mismatch between the sub-ADCs are eliminated by the addition of adjustable digital offsets, $o_{\rm d,i}$ ($i = 2, \ldots, M$), and variable digital gains, $g_{\rm d,i}$ ($i = 2, \ldots, M$), with the following ideal values

$$o_{d,i}=o_1-o_i(1+g_{d,i}),\quad i=2,\ldots,M, \tag{8}$$

and

$$g_{d,i}=(g_1-g_i)/g_i,\quad i=2,\ldots,M. \tag{9}$$

The primary task of the OGC technique is to continuously adjust $o_{\rm d,i}$ and $g_{\rm d,i}$ ($i = 2, \ldots, M$) through the probabilistic property in Section III-A such that (8) and (9) are satisfied.

Depicted in Fig. 7 are the example PDF of the first and ith sub-ADCs in the presence of the offset and gain mismatch. As seen from the figure, the CDFs for a given level, $D_{\rm th}$, is not equal inside the PDF range of the digital output of the first sub-ADC. In order to equalize the CDF of the digital outputs, the

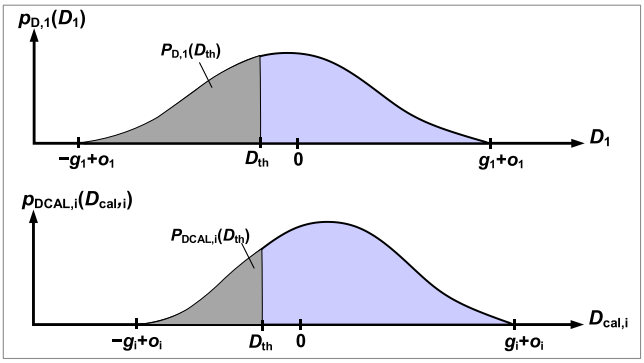

Fig. 7. Digital output PDF of the first and ith sub-ADCs.

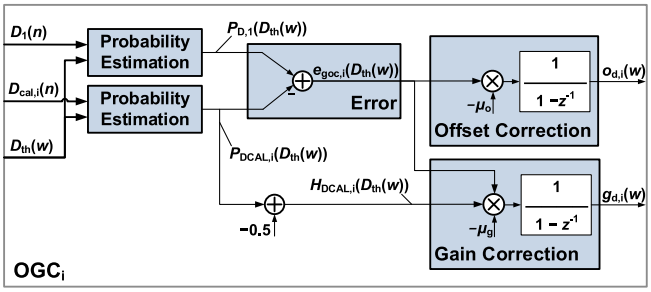

Fig. 8. Detailed block diagram of the ith replica in the OGC method.

deviation of the calibrated digital output CDF of the sub-ADCs from the digital output CDF of the first sub-ADC is considered as *the estimated offset and gain error* defined as

$$e_{ogc,i}\left(D_{th}\right)=P_{D,1}\left(D_{th}\right)-P_{DCAL,i}\left(D_{th}\right),\quad i=2,\ldots,M \tag{10}$$

where $D_{\rm th}$ is an L-level equally spaced digital level, explained in Section III-D. The calibrated digital output CDF of the sub-ADCs are matched *if and only if* $e_{\rm ogc,i}$ ($i = 2, \ldots, M$) are forced to zero over the distribution interval of the digital output of the first sub-ADC. The LMS algorithm can adaptively make the mean of $e_{\rm ogc,i}$ (i.e., $E[e_{\rm ogc,i}]$) equal to zero by optimally adjusting the respective coefficients of $o_{\rm d,i}$ and $g_{\rm d,i}$ [21], [22], [23]. The detailed block of the ith replica of the OGC technique is shown in Fig. 8. Because the term $o_{\rm d,i}$ just

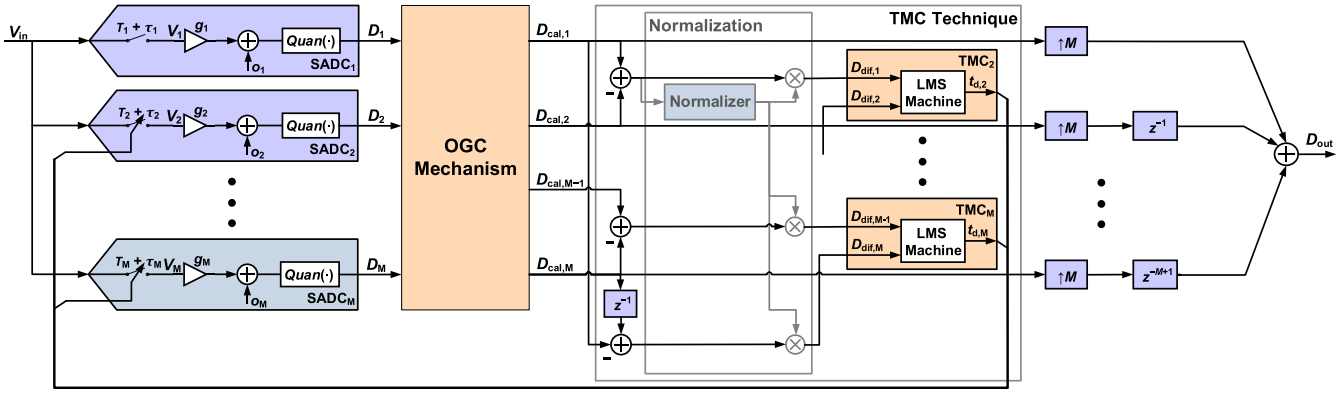

Fig. 9. Block diagram of the proposed TMC technique.

shifts the PDF of a digital output and doesn't disturb the PDF shape [20], [Appendix B], the LMS update equation for the offset mismatch calibration is expressed as following

$$o_{d,i}(w+1) = o_{d,i}(w) - \mu_o e_{ogc,i}(D_{th}(w)), \quad i = 2, \ldots, M \tag{11}$$

where w and μ_o denote the iteration index and offset step size of the LMS algorithm, respectively [21], [22]. In addition, since the coefficient $g_{d,i}$ only affects the width of the probability distribution of a digital output [20], [Appendix B], the LMS update expression for the gain mismatch calibration is also represented as

$$g_{d,i}(w+1) = g_{d,i}(w) - \mu_g H_{DCAL,i}(D_{th}(w))\, e_{ogc,i}(D_{th}(w)) \quad i = 2, \ldots, M \tag{12}$$

where μ_g stands for the gain step size of the LMS algorithm [21], [22]. Moreover, $H_{DCAL,i}(.)$ denotes the shifted CDF defined in Appendix B as $P_{DCAL,i}(.) + \eta$ where η is a constant (i.e., identical to -0.5). After settling of the coefficients $o_{d,i}$ and $g_{d,i}$, the mean of $e_{ogc,i}$ is forced to zero.

Fig. 9 illustrates the timing mismatch calibration (TMC) architecture. For presentation simplicity, it is assumed that the offset and gain mismatch have been already equalized using the above-mentioned OGC scheme similar to almost all other timing mismatch calibration techniques, e.g., [1], [2]. For this reason, the TMC method operates on the calibrated digital outputs $D_{cal,i}$ $(i = 1, \ldots, M)$ rather than the digital signal D_i. The digital differences are firstly scaled to $[-1, 1]$ by a normalizer [see Section III-D]. As stated before, the distribution of the PDFs $p_{DIF,i}(D_{dif,i})$ $(i = 1, \ldots, M)$ can be exploited to detect and correct the timing mismatch. The example PDF of the ith and $(i-1)$th digital differences in the presence of the timing errors are depicted in Fig. 10. As shown in the figure, the CDFs for a given level, D_{th}, is not equal within the PDF range of the digital differences. The CDF distribution of the digital difference must be thus made equal so as to eliminate the timing mismatch among the sub-ADCs. In the TMC method, the timing of the first sub-ADC is considered as the reference (i.e., ideal). Besides, the CDF $P_{DIF,i}(D_{th})$ is compared with the CDF $P_{DIF,i-1}(D_{th})$

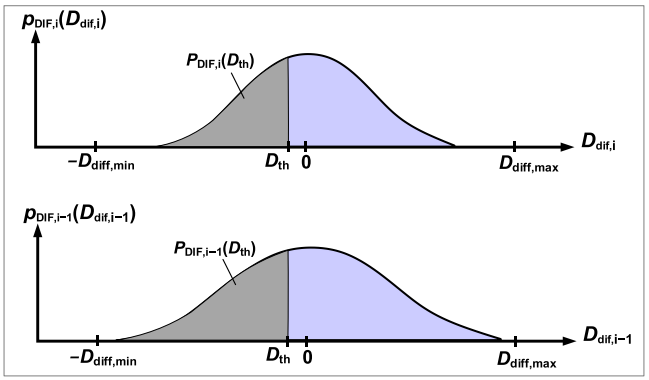

Fig. 10. Probability distribution of the ith and $(i-1)$th digital differences.

for $i = 2, \ldots, M$. Furthermore, *the estimated timing error* is defined as

$$e_{tm,i}(D_{th}) = P_{DIF,i}(D_{th}) - P_{DIF,i-1}(D_{th}) \tag{13}$$

for $i = 2, \ldots, M$ to measure and correct the timing mismatch.

The variable delay lines (VDLs) are often utilized to realize an adjustable timing correction coefficient $t_{d,i}$ $(i = 2, \ldots, M)$ and to mitigate the timing mismatch in analog domain [1], [2]. The LMS engine can also be used to adaptively determine the coefficient $t_{d,i}$ such that the mean of the respective estimated error $e_{tm,i}$ is removed (i.e., $E[e_{tm,i}] = 0$) [20], [Appendix B]. Since the coefficient $t_{d,i}$ proportionally and monotonically alters the spread of the PDF of a digital difference [20], the LMS update equation can be expressed as

$$t_{d,i}(w+1) = t_{d,i}(w) - \mu_{tm} H_{DIF,i}(D_{th}(w)) e_{tm,i}(D_{th}(w)), \quad i = 2, \ldots, M \tag{14}$$

where μ_{tm} stands for the step size of the LMS engine for the timing mismatch calibration [21], [22], and $H_{DIF,i}(.)$ represents the shifted CDF as $P_{DIF,i}(.) + \eta$ with $\eta = -0.5$. In (14), the CDF $P_{DIF,i}(.)$ $(i = 2, \ldots, M)$ is utilized since the sampled signals are not practically available in TMC technique. The detailed block of the ith replica of the TMC method is shown in Fig. 11.

C. CDF Estimation Block

In reality, the digital output CDF of each sub-ADC is not known; however, an estimate of a required CDF can be simply

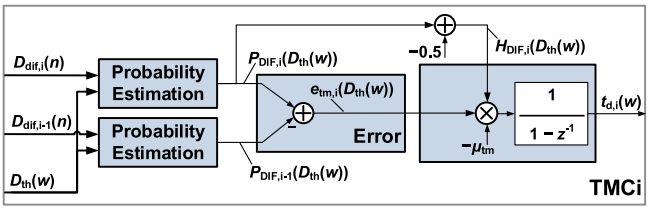

Fig. 11. Detailed block of the ith replica in the TMC method.

extracted as

$$P_{Dx\_est}\left(D_{th}\left(w\right)\right) = \frac{1}{N}\sum_{n=wN}^{w(N+1)-1} CMP_{Dx}\left(D_{th}\left(n\right)\right) \quad (15)$$

where $P_{\mathrm{Dx\_est}}(.)$ and N denote the estimate of the CDF $P_{\mathrm{DX}}(.)$ and the *averaging size*. Moreover, D_{x} and $D_{\mathrm{th}}(w)$ represent a digital variable and a digital level inside the distribution range of D_{x}. In (15), the operator $CMP_{\mathrm{Dx}}(D_{\mathrm{th}}(w))$ is equal to 0 if $D_{\mathrm{th}}(w) \leq D_x(n)$ and identical to 1 otherwise [20]. It can be shown that $P_{\mathrm{Dx\_est}}(D_{\mathrm{th}}(w))$ approaches $P_{\mathrm{DX}}(D_{\mathrm{th}}(w))$ as $N \to \infty$ [Appendix A]. Furthermore, the mean of $P_{\mathrm{Dx\_est}}(D_{\mathrm{th}}(w))$ is identical to $P_{\mathrm{DX}}(D_{\mathrm{th}}(w))$. Hence $P_{\mathrm{Dx\_est}}(D_{\mathrm{th}}(w))$ is utilized as a noisy estimate of $P_{\mathrm{DX}}(D_{\mathrm{th}}(w))$. Since the estimation block needs N samples to produce the estimated CDF $P_{\mathrm{Dx\_est}}(D_{\mathrm{th}}(w))$, each estimated CDF is generated every N clock cycles. Therefore, the iteration index, w, is updated every N clock cycles.

D. Complete Structure of the Calibration Technique

As depicted in Figs. 6 and 9, all replicas of the OGC and TMC techniques operate concurrently at the same time. Each replica separately works on its own input so as to perform its dedicated correction task. In addition, all the replicas of the OGC and TMC blocks share $D_{\mathrm{th}}(w)$. The values of $D_{\mathrm{th}}(w)$ must be updated every iteration, w (i.e., every N clock cycles). In this paper, the values of these parameters are generated as a repeating sequence. The value of a PDF outside its distribution range is zero, and its respective CDF is also zero (or one) for the interval below (or above) its distribution range. Consequently, a PDF does not convey any information for the levels of $D_{\mathrm{th}}(w)$ outside its distribution. Furthermore, the input signal amplitude vary the distribution interval of the calibrated digital outputs $D_{\mathrm{cal,i}}$ $(i = 1, \ldots, M)$, and both the frequency and magnitude of the input signal alter the PDF spread of the digital differences $D_{\mathrm{diff,i}}$ $(i = 1, \ldots, M)$. For this reason, a normalizer is proposed in Appendix C to scale the distribution intervals of $D_{\mathrm{cal,i}}$ and $D_{\mathrm{diff,i}}$ to $[-1, 1]$. The inverse of the distribution intervals of $D_{\mathrm{cal},1}$ and $D_{\mathrm{diff},1}$ are firstly extracted by two normalizers and multiplied with $D_{\mathrm{cal,i}}$ and $D_{\mathrm{diff,i}}$ $(i = 1, \ldots, M)$, respectively. These scaled digital signals are then applied to the OGC and TMC techniques.

It is worth mentioning that the variations of the correction coefficients lead to the SNDR fluctuation. Therefore, these parameters must be selected such that the fluctuations of the correction coefficients remain below a desired amount despite the fact that the values of the averaging size, N, and the step sizes μ_{o}, μ_{g}, and μ_{tm} can be chosen arbitrary. For instance, as the value of N decreases, the step sizes μ_{o}, μ_{g}, and μ_{tm} need to be reduced as well.

Finally, the convergence rate and stability of the TMC method can be affected by the offset and gain mismatch during the concurrent operation of the TMC method and the OGC technique. To alleviate this effect, a simple digital mechanism can be utilized to detect when the offset and gain mismatch drop below a certain level so as to enable the TMC technique.

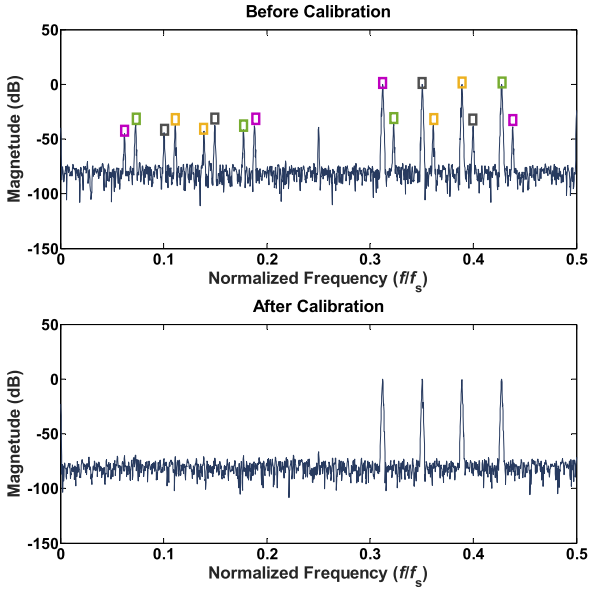

Fig. 12. PSD of the TI-ADC before and after the calibration with a phase modulated 4-tone sine wave.

IV. Simulation Results

Several behavioral simulations have been performed in MATLAB/Simulink to verify the effectiveness of the proposed calibration technique. In these simulations, a TI-ADC consisting of four 10-bit sub-ADCs has been utilized as an example. Moreover, thermal noise is considered in the example TI-ADC. In each sub-ADC, the thermal noise variance is set equal to the variance of the quantization noise. The step size of each sub-ADC, Δ_{QS}, is thus set to $2/2^{11}$. In the simulations, the timing error in each sub-ADC is chosen as independent Gaussian-distributed random variables with a standard deviation of 2%. In addition, a 7-bit VDL block is utilized with a step size of 4×10^{-4} to correct the timing mismatch in the range of $[-25 \times 10^{-3}, 25 \times 10^{-3}]$. A phase modulated 4-tone sine wave is applied to the TI-ADC. The step sizes μ_{o}, μ_{g}, and μ_{tm} are set to 2^{-6}, 2^{-4}, and 2^{-5}, respectively. The averaging size for the CDF estimation, N, and the number of points evaluated by the LMS algorithm, L, are set to 1024 and 8, respectively.

Depicted in Fig. 12 are the output spectra of the TI-ADC before and after the calibration of the gain, offset, and timing mismatch. Fig. 13 illustrates the PDF of the calibrated digital outputs $D_{\mathrm{cal,i}}$ before and after the calibration. Fig. 14 shows the PDF of the digital differences $D_{\mathrm{diff,i}}$ before and after the calibration. As seen from the figures, the spurs resulted from the mismatch among the sub-ADCs are vanished after the calibration, and the PDFs of the calibrated digital output

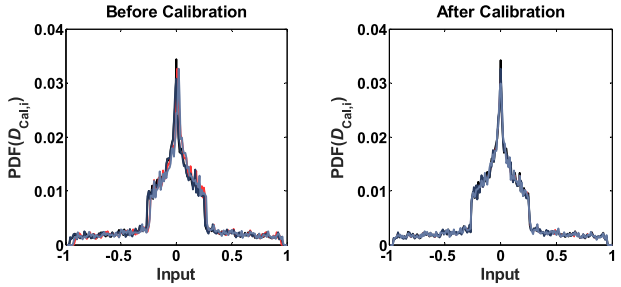

Fig. 13. PDFs of the calibrated digital outputs of sub-ADCs with a phase modulated 4-tone sine wave before and after the calibration.

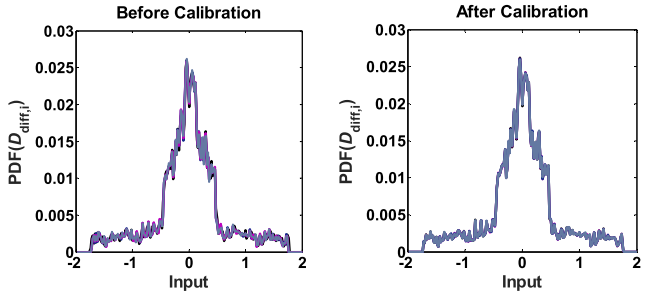

Fig. 14. PDFs of the digital differences with a phase modulated 4-tone sine wave before and after the calibration.

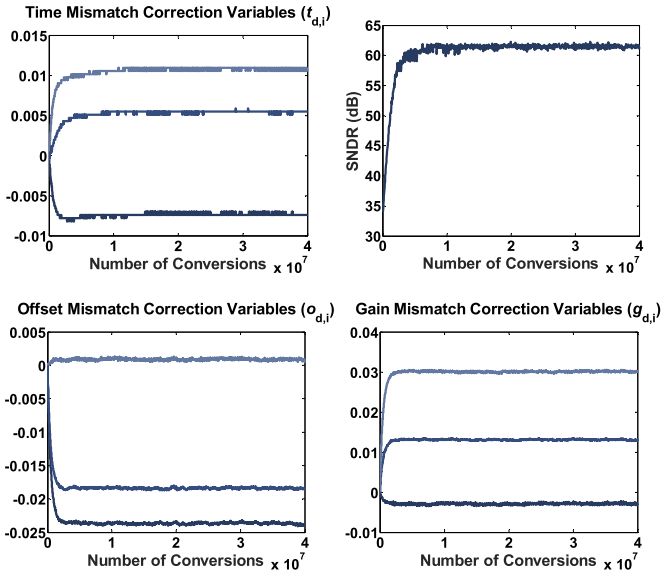

Fig. 15. Convergence of the SNDR and correction coefficients during the calibration.

and digital differences also coincide with each other after the calibration in contrast to their respective PDFs before the calibration.

Additionally, an almost full-scale sinusoidal input with a frequency of $(93/257.7)f_s$ is applied to the TI-ADC in the following simulations. Shown in Fig. 15 are the convergence of the coefficients $g_{d,i}$, $o_{d,i}$, $t_{d,i}$, and the SNDR over time during the calibration. The spurious-free dynamic range (SFDR) and signal-to-noise and distortion ratio (SNDR) are enhanced from 34.5 dB and 33.7 dB to 70.2 dB and 61 dB, correspondingly,

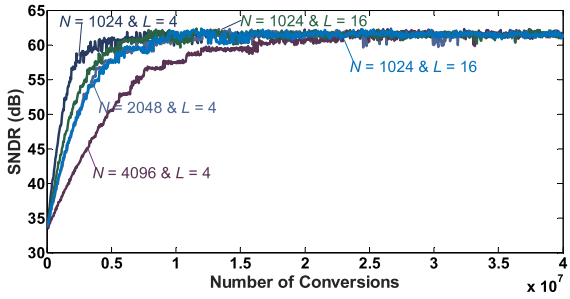

Fig. 16. Conversion of the SNDR during the calibration with different L and N.

after the calibration. The required number of the conversion samples is approximately 4×10^6. The SNDR varies from 60.2 dB to 61.8 dB after the calibration. Fig. 16 illustrates the SNDR with different values of the averaging size for the CDF estimation, N, and the number of points evaluated by the LMS, L. The SNDR convergence is almost immune to the value of L and the amplitude and frequency of the input signal. However, as the value of N is reduced, the convergence rate of the SNDR is increased at the cost of a noisy SNDR. It is imperative to note that the convergence rate of the calibration scheme is restricted by the TMC technique. The OGC method can converge 4 times faster without employing the TMC scheme.

V. Discussions

The OGC scheme is based on a novel concept described in Section III-A. Moreover, the proposed TMC method provides a different perspective on the TI-ADC timing mismatch calibration based on the approach presented in Section III-A despite the fact that the time difference has been used to measure the timing errors [1]. The method of [8] is just suitable for the timing mismatch calibration of SAR ADCs, while the TMC technique can be exploited with any type of ADCs. Because of utilizing the OGC method, the presented method doesn't impose any bound on the maximum offset mismatch in contrast to the zero-crossing detection techniques of [9] (i.e., ZCD1 and ZCD2). However, the method of ZCD2 is almost immune to the offset mismatch. In contrast to [1], [2], [3], [8], the presented method mitigates the offset and gain mismatch through the OGC scheme. Most of the timing mismatch calibration techniques work well (e.g., [1], [2]) *on condition that* the offset and gain of the sub-ADCs are sufficiently matched prior to them. Although the equations of (11), (12), and (14) utilize the simplifications and approximations of Appendix B (to avoid the estimation of the PDFs), the TMC and OGC methods have the capability of enhancing the SNDR of a TI-ADC up to 75 dB. It must be emphasized that the resolution of a TI-ADC is generally less than 11 bits. The presented scheme is briefly compared with some other techniques in Table I.

A. Digital Complexity and Power Consumption

Each replica of the CDF estimation block operates at $1/M$ of the TI-ADC sampling frequency and it doesn't require any multi-bit multiplier as opposed to [2], [4], [5]. Each replica of

TABLE I
COMPARISON OF THE PRESENTED TECHNIQUE WITH SOME OTHER METHODS

	Offset Calibration	Gain Calibration	Immunity to Offset & Gain Mismatch	Sensitivity to Input Signal PDF	Convergence of SNDR *	Digital Complexity @ f_s
This Paper	✓	✓	✓	✓	4×10^6 @ 60 dB	Moderate [(1)]
[1]	×	×	×	×	15×10^4 @ 45 dB	Low
[2]	×	×	✓	×	5×10^4 @ 52 dB	High
[3]	×	×	✓	×	2×10^6 @ 25 dB	Low
[4]	×	✓	✓	×	5×10^4 @ 61 dB	High
[5]	✓	✓	✓	×	2×10^7 @ 70 dB	High
[9]	×	×	✓[(2)]	✓	2×10^6 @ 40 dB	Low

* Convergence rate of SNDR is generally decreased by a factor of 4 for every 6 dB more SNDR.
[(1)] The normalization process is not considered.
[(2)] ZCD2 is almost immune to the offset mismatch due to high pass filtering process in contrast to ZCD1.

this block can also be realized through an up-down counter followed by a bit shift operator. Furthermore, the counter is reset every N counts. Nonetheless, the proposed method requires at least twice more addition operators (mainly due to the digital comparisons) than [1], [3], [9] at the sampling rate.

Additionally, as illustrated in Fig. 8, each replica of the offset calibration loop in (11) is just realized by an accumulator and a bit shift operator. However, the hardware realization of the LMS machine in (12) and (14) need multi-bit multipliers. It must be emphasized that both the OGC and TMC methods work at $1/(MN)$ of the TI-ADC sampling rate; consequently, all the digital multiplications can be implemented serially for the reduction of digital gates and die area. In contrast, the methods of [2], [4], [5] utilize multi-bit multipliers at the sampling rate. Furthermore, the digital timing mismatch correction of [4], [5] lead to complex digital circuits. It is worth to mention that the techniques of [1], [3], [9] operate without the need for any multipliers. In fact, the outputs of the normalizers and the most significant bits (MSBs) of the calibrated digital outputs and the digital differences can be practically truncated to reduce the hardware cost. It is worth mentioning that the normalization process can also be utilized by normalizing D_{th} to the calibrated digital outputs and the digital differences. In this case, the scaled values of D_{th} remain inside the distribution intervals of the calibrated digital outputs and the digital differences. In addition, D_{th} can have specific values (e.g., ±0.75 and ±0.25) for significant reduction of the hardware cost in the required multipliers. For these reasons, the hardware overhead of the multipliers is not significant, and this overhead is not considered in Table I.

B. Input Signal Limitations

The proposed blind calibration technique has some limitations on the statistics and bandwidth of the input signal similar to almost all other calibration methods, e.g., [8], [9]. It is worth mentioning that the input signal of the TI-ADC has an almost full-scale range and a *continuous Gaussian distribution* in almost all applications [23]; nevertheless, the presented method is not sensitive to the frequency and amplitude of the input signal owing to the automatic normalization process introduced in Appendix C. In the proposed calibration mechanism, the PDF of the input signal must not exhibit zero intervals within its distribution range. In addition, the TMC method operates well providing that the bandwidth of the input signal is less than half the TI-ADC sampling frequency. Nonetheless, this method can operate with sinusoid, multi tone sine wave, and modulated sinusoid at incoherent frequencies (i.e., the ratio of the input frequency (or frequencies) to the sampling frequency must not be equal to Y/V where Y and V are integers). Furthermore, the frequency of the input sine waves can exceed Nyquist rate due to the fact that, in the discrete-time domain, a sine wave with a frequency of $f_{\text{in}}/f_{\text{s}}$ is indistinguishable from a sinusoid with a frequency of $(f_{\text{in}} + Y \times f_{\text{s}})/f_{\text{s}}$ where Y is an integer.

In summary, the presented calibration technique can work with various input signals consisting of modulated sine wave, multi tone sinusoid, and ramp. It must be emphasized that the overall convergence rate of the described calibration technique can be affected by the frequency dependency of the TMC method without the normalization process; for instance, the convergence rate of the TMC technique can decrease as the input signal frequency approaches $f_{\text{s}}/2$ or 0.

C. Residual Offset and Gain Errors

The proposed calibration scheme manifests residual offset and gain errors identical to the offset and gain of the first sub-ADC, respectively, after the calibration. Nevertheless, the residual offset and gain errors are not hazardous issue in most ADC applications [20], [23], [24].

D. Selection of the Levels of D_{th}

The LMS algorithm iteratively determines the variables $o_{\text{d,i}}$, $g_{\text{d,i}}$, and $t_{\text{d,i}}$ according to the averages of the update terms $e_{\text{ogc}}(D_{\text{th}})$, $e_{\text{ogc}}(D_{\text{th}}) \times H_{\text{DCAL,i}}(D_{\text{th}})$, and $e_{\text{tm}}(D_{\text{th}}) \times H_{\text{DIFF,i}}(D_{\text{th}})$ over the L values of D_{th}, respectively. Consequently, the values of D_{th} would ideally be placed wherever the update terms have nonzero values. Since the update terms are not exactly known and dependent on the input signal, the values of D_{th} should be spaced equally over the range $[-1, 1]$. Furthermore, because the probability distributions of the digital differences are symmetrical around $D_{\text{th}} = 0$, all the CDFs $P_{\text{diff,i}}(D_{\text{th}})$ $(i = 2, \ldots, M)$ are equal to 0.5. Therefore, the term $e_{\text{tm,i}}(D_{\text{th}})$ $(i = 2, \ldots, M)$ for

$D_{\text{th}} = 0$ is equal to 0. As a consequence, this level doesn't contribute to the timing mismatch detection, and D_{th} should not have a value at zero.

VI. Conclusions

In this paper, a digital blind background calibration technique of the imperfections in TI-ADCs, consisting of the offset, gain, and timing mismatch, has been introduced. The presented method directly operates on the statistics of the input signal to continuously estimate and eliminate the conversion errors resulted from TI-ADC non-idealities during the normal data conversion operation. The SFDR and SNDR are improved by more than 35 dB and 27 dB, respectively, through the proposed calibration technique.

Appendix A

This appendix shows that the mean of $P_{\text{Dx\_est}}(.)$ is identical to $P_{\text{DX}}(.)$. It follows from the basic probability that

$$P\left(CMP_{Dx}\left(D_{th}\left(n\right)\right)=1\right)=P_{DX}\left(D_{th}\left(n\right)\right),$$
$$P\left(CMP_{Dx}\left(D_{th}\left(n\right)\right)=0\right)=1-P_{DX}\left(D_{th}\left(n\right)\right). \quad \text{(A.1)}$$

For this reason, the expectation of $CMP_{\text{Dx}}(D_{\text{th}}(w))$ is as following

$$E\left(CMP_{Dx}\left(D_{th}\left(n\right)\right)\right)=P_{DX}\left(D_{th}\left(n\right)\right). \quad \text{(A.2)}$$

Furthermore, the expectation of $P_{\text{Dx\_est}}(D_{\text{th}}(w))$ is given by

$$E\left[P_{Dx\_est}\left(D_{th}\left(w\right)\right)\right]=E\left[\frac{1}{N}\sum_{n=wN}^{w(N+1)-1}CMP_{Dx}\left(D_{th}\left(n\right)\right)\right]. \quad \text{(A.3)}$$

The expectation of $P_{\text{Dx\_est}}(D_{\text{th}}(w))$ can also be expressed as

$$E\left[P_{Dx\_est}\left(D_{th}\left(w\right)\right)\right]=\frac{1}{N}\sum_{n=wN}^{w(N+1)-1}E\left[CMP_{Dx}\left(D_{th}\left(n\right)\right)\right]. \quad \text{(A.4)}$$

It is evident from (A.2) and (A.4) that the expectation of $P_{\text{Dx\_est}}(D_{\text{th}}(w))$ is equal to $P_{\text{DX}}(D_{\text{th}}(w))$. Moreover, it can be easily shown that the averaging operation reduces the standard deviation of the comparison operation by a factor of $1/N$ [20]. In turn, as N increases the mean of $P_{\text{Dx\_est}}(D_{\text{th}}(w))$ approaches $P_{\text{DX}}(D_{\text{th}}(w))$.

Appendix B

This appendix obtains the relation between the input and output CDFs of a *general linear function* in the form of $D_{\text{o}} = a_0 + (1 + a_1) \times D_{\text{i}}$ where a_0 and a_1 denote the offset and gain errors, respectively. Also, the LMS update equation through the CDF comparison is derived. From the basic probability, it can be shown that

$$p_{DO}\left(D_o\right)=\left|1+a_1\right|^{-1}p_{DI}\left(\left|1+a_1\right|^{-1}\left(D_o-a_0\right)\right). \quad \text{(B.1)}$$

If the term $a_1 \ll 1$, the output PDF, $p_{\text{DO}}(D_{\text{o}})$, can be approximately expressed as following:

$$p_{DO}\left(D_o\right)\approx\left(1-a_1\right)p_{DI}\left(D_o-a_0\right). \quad \text{(B.2)}$$

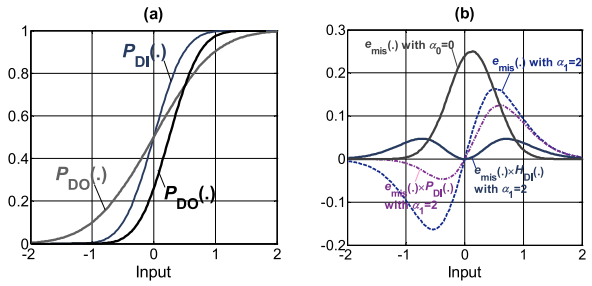

Fig. 17. (a) Input and output CDFs in the presence of offset and gain errors, and (b) distribution of different errors and update terms.

Furthermore, the output CDF $P_{\text{DO}}(D_{\text{o}})$ can be represented by:

$$P_{DO}\left(D_o\right)\approx\left(1-a_1\right)P_{DI}\left(D_o-a_0\right). \quad \text{(B.3)}$$

Besides, the variables a_0 and a_1 can be iteratively updated by the LMS algorithm based on the *estimated mismatch error* $e_{\text{mis}}(D_{\text{o}}) = P_{\text{DES}}(D_{\text{o}}) - P_{\text{DO}}(D_{\text{o}})$ where $P_{\text{DES}}(D_{\text{o}})$ is the desired output CDF. Therefore, the LMS machine multiplies $e_{\text{mis}}(.)$ with the partial derivatives $\partial P_{\text{DO}}(.)/\partial a_0$ and $\partial P_{\text{DO}}(.)/\partial a_1$ to update the parameters a_0 and a_1, respectively. These partial derivatives are also expressed by:

$$\partial P_{DO}\left(D_o\right)/\partial a_0=-\left(1-a_1\right)p_{DI}\left(D_o-a_0\right), \quad \text{(B.4)}$$
$$\partial P_{DO}\left(D_o\right)/\partial a_1=-P_{DI}\left(D_o-a_0\right). \quad \text{(B.5)}$$

Due to the fact that $a_1 \ll 1$, the above expressions can also be approximated as:

$$\partial P_{DO}\left(D_o\right)/\partial a_0\approx-p_{DI}\left(D_o-a_0\right), \quad \text{(B.6)}$$
$$\partial P_{DO}\left(D_o\right)/\partial a_1\approx-P_{DI}(D_o-a_0). \quad \text{(B.7)}$$

As shown below, $e_{\text{mis}}(.)$ is proportional to a_0. Accordingly, (B.6) can be considered as a constant to simplify the implementation of the LMS engine. In fact, the means of $e_{\text{mis}}(.)$ and $e_{\text{mis}}(.)\times P_{\text{DI}}(.)$ are always proportional to a_0 and a_1, respectively. However, in practice, the LMS algorithm iteratively determines a_0 and a_1 according to the averages of the update terms $e_{\text{mis}}(D_{\text{th}})$ and $e_{\text{mis}}(D_{\text{th}}) \times P_{\text{DI}}(D_{\text{th}})$ over L points (i.e., determined by the L-level signal D_{th}), respectively.

Fig. 17(a) shows the CDF of a Gaussian distributed input, $P_{\text{DI}}(.)$, and its respective output CDFs for two cases: 1) $a_0 = 0.5$ and $a_1 = 0$; 2) $a_0 = 0$ and $a_1 = 2$. In Fig. 17(b), the error and update terms are depicted as well. As seen from the figure, the signs of $e_{\text{mis}}(.)$ and the offset, a_0, are identical for all the values of D_{o}. Consequently, the average of $e_{\text{mis}}(.)$ has the same polarity as a_0 regardless of the value of L. In contrast, the sign of $e_{\text{mis}}(.)\times P_{\text{DI}}(.)$ alters at $D_{\text{o}} = 0$, and it has an opposite sign for $D_{\text{o}} < 0$. Therefore, the levels of D_{th} must be chosen such that the average of $e_{\text{mis}}(D_{\text{th}}) \times P_{\text{DI}}(D_{\text{th}})$ over these levels remain proportional to the gain error, a_1, for the proper operation of the LMS algorithm.

It can be argued that if the sign of $P_{\text{DI}}(.)$ is altered at $D_{\text{o}} = 0$, the average of $e_{\text{mis}}(D_{\text{th}}) \times P_{\text{DI}}(D_{\text{th}})$ over all the L levels would remain proportional to the gain error. For this reason, the shifted CDF is firstly defined as:

$$H_{DI}\left(D_o\right)=P_{DI}\left(D_o\right)+\eta \quad \text{(B.8)}$$

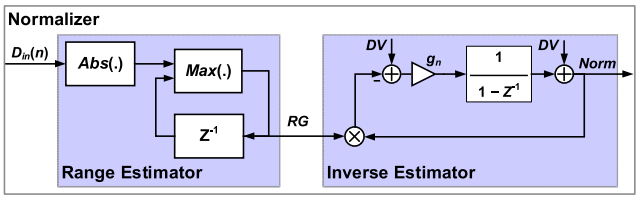

Fig. 18. Block diagram of the normalizer.

where η is a constant. Moreover, the evaluation function is defined by:

$$Eval\,(\eta) = \int_{ll}^{lu} \left(e_{mis}\,(D_o) - H_{DI}\,(D_o, \eta)\right)^2 dD_o \qquad \text{(B.9)}$$

where *ll* and *lu* are the lower and upper limits of the distribution of D_o, respectively. If $Eval(\eta)$ is derived to its minimum, $e_{mis}(.)$ and $H_{DI}(.)$ have the maximum similarity (or difference); thus, their signs alter at almost the same point. The partial derivative of $Eval(\eta)$ with respect η must be obtained and set to zero so as to determine the desired value of η. It can be proved that $Eval(\eta)$ is minimized for

$$\eta = -\int_{ll}^{lu} P_{DI}\,(D_o)\,dD_o \Big/ \int_{ll}^{lu} dD_o. \qquad \text{(B.10)}$$

The above result is obtained considering the fact that the mean of $e_{mis}(D_{th})$ is zero with a symmetrical input PDF and $a_0 = 0$. This result indicates that η must be equal to the mean of $P_{DI}(D_o)$. In this work, η is set to -0.5 since the mean of the CDF of an input signal which has a symmetrical distribution around zero is identical to -0.5. As seen in Fig. 17(b), the average of $e_{mis}(D_{th}) \times H_{DI}(D_{th})$ over any L points is now proportional to a_1. The minimum number of levels, L, for a linear system must be greater than 1 [21], [22]. It is imperative to note that the impact of the timing mismatch on the PDF shape of a digital difference is the same as the gain error (i.e., $a_1 \neq 0$). Thus, the update term in (14) is the product of the input CDF and the estimated timing error.

APPENDIX C

In this appendix, a digital normalizer is presented to firstly estimate its input range and then obtain the inverse of the estimated input range. As a consequence, this block is comprised of two parts: 1) the Range Estimator; 2) the Inverse Estimator. As depicted in Fig. 18, the range estimator extracts the magnitude of the input signal by the absolute operator, *Abs*(.). This signal is then compared with the previous value of the estimated range, *RG*, through the maximum extractor, *Max*(.). After applying a number of samples (i.e., in this work, N samples) to the normalizer, the signal *RG* will be the maximum of the input signal over the applied samples. It is worth mentioning that the range estimator must be updated to have the capability of tracking the variations of its input.

The variable *Norm* is the inverse of *RG* as long as the result of *Norm* $\times$ *RG* is equal to 1. The inverse estimator block applies the difference between *Norm* $\times$ *RG* and the desired value, *DV*, (i.e., *DV* =1) to a discrete-time integrator through a gain block, g_n (in this work, $g_n = 0.1$). The gain g_n determines the accuracy and convergence rate of the inverse estimator (i.e., as the convergence rate decreases by reducing g_n, a more accurate estimate of the inverse is obtained). Then, the integrator iteratively adjusts *Norm* such that its input is made identical to zero. Since the ideal range of the input signal would be equal to 1, the output of integrator is initialized to 1 by adding 1 to the output of the integrator as depicted in Fig. 18.

REFERENCES

[1] H. Wei, P. Zhang, B. D. Sahoo, and B. Razavi, "An 8 bit 4 GS/s 120 mW CMOS ADC," *IEEE J. Solid-State Circuits*, vol. 49, no. 8, pp. 1751–1761, Aug. 2014.
[2] B. Razavi, "Design considerations for interleaved ADCs," *IEEE J. Solid-State Circuits*, vol. 48, no. 8, pp. 1806–1817, Aug. 2013.
[3] M. El-Chammas and B. Murmann, "A 12-GS/s 81-mW 5-bit time-interleaved flash ADC with background timing skew calibration," *IEEE J. Solid-State Circuits*, vol. 46, no. 4, pp. 838–847, Apr. 2011.
[4] J. Matsuno, T. Yamaji, M. Furuta, and T. Itakura, "All-digital background calibration technique for time-interleaved ADC using pseudo aliasing signal," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 60, no. 5, pp. 1113–1121, May 2013.
[5] S. M. Jamal, D. Fu, N. C.-J. Chang, P. J. Hurst, and S. H. Lewis, "A 10-b 120-Msample/s time-interleaved analog-to-digital converter with digital background calibration," *IEEE J. Solid-State Circuits*, vol. 37, no. 12, pp. 1618–1627, Dec. 2002.
[6] J. Li, S. Wu, Y. Liu, N. Ning, and Q. Yu, "A digital timing mismatch calibration technique in time-interleaved ADCs," *IEEE Trans. Circuits Syst. II, Express Briefs*, vol. 61, no. 7, pp. 486–490, Jul. 2014.
[7] H. Jin and E. K. F. Lee, "A digital-background calibration technique for minimizing timing-error effects in time-interleaved ADCs," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 47, no. 7, pp. 603–613, Jul. 2000.
[8] S. Lee, A. P. Chandrakasan, and H. S. Lee, "A 1 GS/s 10b 18.9 mW time-interleaved SAR ADC with background timing skew calibration," *IEEE J. Solid-State Circuits*, vol. 49, no. 12, pp. 2846–2856, Dec. 2014.
[9] C. Y. Wang and J. T. Wu, "A multiphase timing-skew calibration technique using zero-crossing detection," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 56, no. 6, pp. 1102–1114, Jun. 2009.
[10] C.-Y. Wang and J.-T. Wu, "A background timing-skew calibration technique for time-interleaved analog-to-digital converters," *IEEE Trans. Circuits Syst. II, Express Briefs*, vol. 53, no. 4, pp. 299–303, Apr. 2006.
[11] S. M. Jamal, D. Fu, M. P. Singh, P. J. Hurst, and S. H. Lewis, "Calibration of sample-time error in a two-channel time-interleaved analog-to-digital converter," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 51, no. 1, pp. 130–139, Jan. 2004.
[12] S. Vitali, G. Cimatti, R. Rovatti, and G. Setti, "Adaptive time-interleaved ADC offset compensation by nonwhite data chopping," *IEEE Trans. Circuits Syst. II, Express Briefs*, vol. 56, no. 11, pp. 820–824, Nov. 2009.
[13] S. Singh, L. Anttila, M. Epp, W. Schlecker, and M. Valkama, "Frequency response mismatches in 4-channel time-interleaved ADCs: Analysis, blind identification, and correction," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 62, no. 9, pp. 2268–2279, Sep. 2015.
[14] S. Singh, L. Anttila, M. Epp, W. Schlecker, and M. Valkama, "Analysis, blind identification, and correction of frequency response mismatch in two-channel time-interleaved ADCs," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 5, pp. 1721–1734, May 2015.
[15] A. Bonnetat, J.-M. Hodé, G. Ferré, and D. Dallet, "Correlation-based frequency-response mismatch compensation of quad-TIADC using real samples," *IEEE Trans. Circuits Syst. II, Express Briefs*, vol. 62, no. 8, pp. 746–750, Aug. 2015.
[16] A. Bonnetat, J.-M. Hodé, G. Ferré, and D. Dallet, "An adaptive all-digital blind compensation of dual-TIADC frequency-response mismatch based on complex signal correlations," *IEEE Trans. Circuits Syst. II, Express Briefs*, vol. 62, no. 9, pp. 821–825, Sep. 2015.
[17] M. El-Chammas and B. Murmann, "General analysis on the impact of phase-skew in time-interleaved ADCs," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 56, no. 5, pp. 902–910, May 2009.
[18] U. Eduri and F. Maloberti, "Online calibration of a Nyquist-rate analog-to-digital converter using output code-density histograms," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 51, no. 1, pp. 15–24, Jan. 2004.

[19] A. Papoulis and S. U. Pillai, *Probability, Random Variables, and Stochastic Processes*, 4th ed. New York, NY, USA: McGraw-Hill, 2002.
[20] H. Mafi, M. Yavari, and S. S. Behzadi, "Digital background calibration of residue amplifier non-idealities in pipelined ADCs," *Circuits Syst. Signal Process.*, vol. 35, no. 10, pp. 3675–3699, Dec. 2015.
[21] B. Zeinali, T. Moosazadeh, M. Yavari, and A. Rodriguez-Vazquez, "Equalization-based digital background calibration technique for pipelined ADCs," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 22, no. 2, pp. 322–333, Feb. 2014.
[22] H. Mafi, R. Mohammadi, and H. Shamsi, "A statistics-based digital background calibration technique for pipelined ADCs," *Integr., VLSI J.*, vol. 51, no. 9, pp. 149–157, Sep. 2015.
[23] B. Murmann and B. E. Boser, "Digital domain measurement and cancellation of residue amplifier nonlinearity in pipelined ADCs," *IEEE Trans. Instrum. Meas.*, vol. 56, no. 6, pp. 2504–2514, Dec. 2007.
[24] N. Mirzaie, H. Shamsi, and G.-S. Byun, "Resilient design of current steering DACs using a transistor level approach," *Analog Integr. Circuits Signal Process.*, vol. 90, no. 1, pp. 29–41, Jan. 2017.

Hamidreza Mafi received the B.Sc. degree in electrical engineering from Shahid Rajaei University, Iran, in 2007 and M.Sc. degree in electrical engineering Qazvin Azad University, Iran, in 2012. He served with the Air Force of Iran as a Second Lieutenant from 2007 to 2009. He is currently working towards the Ph.D. degree at University of Zanjan, Iran.

He has served as a reviewer for IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS and *Circuit, System, and Signal Processing* (*CSSP*). His research interests include data converters and mixed-signal integrated circuits.

Mostafa Yargholi received the B.Sc. degree in electrical engineering from Iran University of Science and Technology in 2002, and the M.Sc. and Ph.D. degrees in electrical engineering from Tarbiat Modares University, Iran, in 2004 and 2009, respectively. He has been working as Assistant Professor with the Faculty of Engineering, University of Zanjan, Iran, since 2009. His current research interests include RFIC design, analog and mixed-signal integrated circuits, and data converters.

Mohammad Yavari (S'01-M'08) received the B.Sc., M.Sc., and Ph.D. degrees in electrical engineering from the University of Tehran, Tehran, Iran, in 1999, 2001, and 2006, respectively.

He has been with the Department of Electrical Engineering, Amirkabir University of Technology (Tehran Polytechnic), Tehran, since 2006, where he is now an Associate Professor and serves as the Head of the Electronics group. He founded the Integrated Circuits Design Laboratory in AUT in 2007. He spent several research periods with the Institute of Microelectronics of Seville (IMSE-CNM), Seville, Spain. He was with Niktek, from May 2004 to April 2005 and October 2006 to May 2007, as a Principal Design Engineer, where he was involved in the design of high-resolution A/D and D/A converters for professional digital audio applications. He is the author or co-author of more than 140 peer-reviewed papers in international and national journals and conference proceedings on analog integrated circuits. His current research interests include analog and mixed-signal integrated circuits and signal processing, data converters, biomedical circuits and systems, and CMOS RFIC design for wireless communications.

Dr. Yavari was a recipient of the Best Student Research Award of the University of Tehran in 2004, a corecipient of the Best Paper Award of the Iranian Conference on Electrical Engineering in 2014. He has been an Associate Editor of the *International Journal of Circuit Theory and Applications* since 2014.