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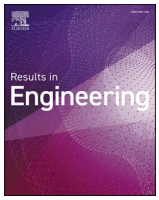

A systematic time-based approach for analysis and compensation of excess loop delay in continuous-time sigma-delta modulators exceeding one clock cycle

Reza Kohandel, Mohammad Yavari *

Integrated Circuits Design Laboratory, Department of Electrical Engineering, Amirkabir University of Technology (Tehran Polytechnic), 424 Hafez Ave., Tehran 15875-4413, Iran

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ABSTRACT

In this paper, we propose a new time-domain method for calculating the coefficients in continuous-time sigma-delta modulators (CT ΣΔMs) in the presence of excess loop delay (ELD). Additionally, we present a two-step method to compensate for the effect of dynamic element matching (DEM) in multibit digital-to-analog converters (DACs). Our method intuitively investigates the loop-filter outputs and yields systematic equations suitable for computer aided design (CAD) softwares. The equations are easily applicable to modulators with an arbitrary feedback pulse shape at each stage and can be extended to higher-order modulators. The generality and flexibility of these equations enable their use for altering the modulator's feedback pulse shape and recalculating modulator coefficients. Furthermore, we extended our approach for ELD compensation in modulators utilizing the DEM block for feedback DAC linearization, allowing for DEM block delays exceeding one clock cycle. Simulation results validate the accuracy of the analytical calculations.

1. Introduction

Continuous-time sigma-delta modulators (CT ΣΔMs) offer higher speed and lower power consumption in comparison to their discrete-time counterparts [1]. However, their maximum sampling speed is limited by the excess loop delay (ELD), which refers to the delay from the quantizer input to the digital-to-analog converter (DAC) output. ELD adversely affects the noise shaping performance of the noise transfer function (NTF). This leads to a reduction in signal-to-noise ratio (SNR) and cause peaking in the signal transfer function (STF) which can potentially destabilize the modulator [2]. More delay can increase loop-filter's order and out-of-band gain of NTF. To maintain stability, the ELD must not exceed one period of the sampling clock [3]. Additionally, incorporating a dynamic element matching (DEM) block in multi-bit CT ΣΔMs, as depicted in Fig. 1(a), to address DAC nonlinearity, exacerbates ELD, further limiting the sampling speed.

To enhance modulator performance, several ELD compensation methods have been proposed [4–35]. The conventional scheme, illustrated in Fig. 1(b), employs a fast path around the quantizer [5] utilizing an adder. Using additional adder would increase the power consumption. Therefore, to minimize modulator power consumption, the fast signal path can be injected into the last integrator input through a digital differentiator and capacitor-based voltage DAC (CV-DAC) [6–7]. Various circuit techniques have been developed to implement fast feedback loop with minimal delay and feedback coefficient error [8–10, 27]. Traditional methods theoretically fully compensate for ELD smaller than one clock cycle without altering the STF of the modulator, although with practical limitations. To overcome the sampling speed limit imposed by the quantizer and DAC finite acquisition time, the fast path can be implemented using a sample and hold circuit, as depicted in Fig. 1 (c) [11,12]. This enables the modulator to accommodate delays exceeding one clock cycle in the outermost feedback path, although with some degradation in SNR due to additional in-band noise. However, this solution can increase power consumption due to the need for fast-settling sample-and-hold, especially in high-speed applications. Variations of this approach have been explored in [13,14].

The fast feedback loop also can be shifted to digital domain after quantizer [15,16], where logic elements can operate at higher frequencies, although this may increase the signal level at quantizer input, potentially leading to saturation. Also, in [17], it is tried to nullify the second-highest coefficient in loop filter's numerator to alleviate the need to the coefficient's recalculation in presence of ELD. However, it fails to

* Corresponding author.
E-mail address: myavari@aut.ac.ir (M. Yavari).

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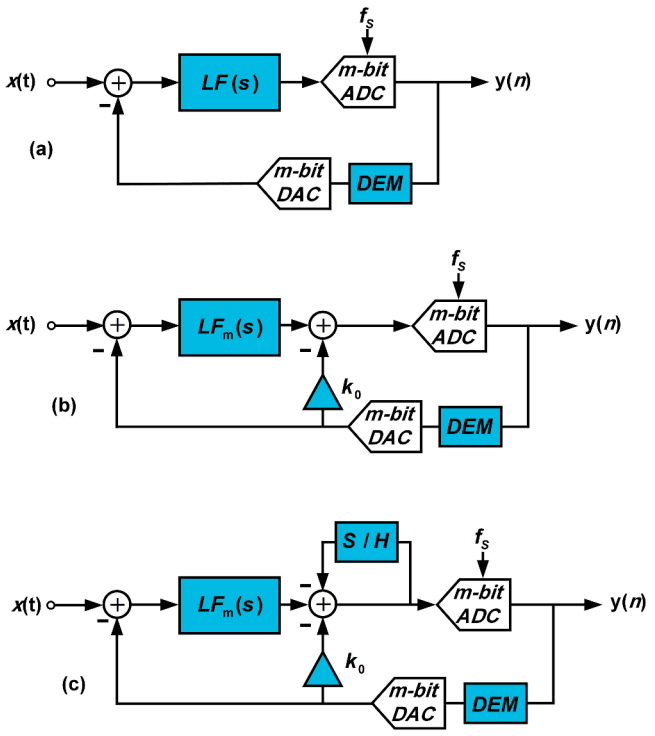

Fig. 1. (a) General form of CTDSMs. (b) Traditional ELD Compensation [1]. (c) Compensation using sample and hold for ELD more than one clock cycle [11].

retrieve SNR as in [13]. Other approaches include a switching method that can alter the transfer function with a clock [18], a digitally controlled threshold scheme [19], and a predictive comparator using sign-LMS algorithm for estimating the coefficients [20]. The latter approach enables compensation of up to two sampling periods in low pass ΣΔM. However, for higher-order compensation, the prediction block would add complexity. Also, methods introduced in [21–24] are limited to rectangular DAC pulse shape and hardware-intensive algorithm. Furthermore, some compensation methods have been proposed for delays exceeding one clock cycle in [11–14], but they lack a systematic procedure.

To reduce power consumption, recent work utilizes successive approximation register (SAR) based analog-to-digital converter (ADC) as the quantizer [25–27]. However, one-bit-a-time conversion in SAR ADC introduces more delays. In [25], they utilize bitwise approach to decrease the delay. However, it is not supporting the cascade of integrators with feed-forward (CIFF) architecture. In addition, [26] utilizes a time-interleaving quantizer. They used a different approach for most significant bits (MSBs) and least significant bits (LSBs) which is the combination of conventional method and digital method.

Among the various compensation methods, the traditional approach is widely used in high-speed applications [8–10,15,28,29] due to its ability to match the response of non-ideal modulator to the ideal one. However, a significant challenge is the calculation of the feedback coefficients and fast path gain. The impulse invariance technique is commonly used for determination of modulator parameters [3,30], while considering the effect of ELD. A main drawback of this method is that the feedback pulse shape must be fully determined in s-domain, and also for every new pulse shape, the coefficients must be recalculated using transformation between the z- and s- domains [31], which is not feasible for all feedback waveforms. In practice, the circuit non-idealities alter the ideal pulse shape, complicating coefficient calculations, especially for higher order modulators. Due to these complexities associated with frequency-based methods, time-based approaches have been proposed. It is demonstrated that the coefficients of a CT ΣΔM's loop-filter depends solely on the area and delay of the DAC pulse [31]. This insight suggests that using pulses with same area and delay would not alter the NTF. Based on this principle, a time-domain method based on Taylor series expansion for ELD compensation has been introduced [31].

In this paper, we investigate the traditional ELD compensation technique in time-domain, aiming to derive systematic equations for calculating modified modulator coefficients and further we extend our analysis to propose a two-step ELD compensation method. Despite its apparent complexity, our equations can be easily calculated in software programs. Two main DAC pulse shapes commonly used in the literature are non-return-to-zero (NRZ) and return-to-zero (RZ) pulses [1]. The NRZ pulse shape is u(t) - u(t-T_s), indicating that it is zero for $t > T_s$. However, the RZ DAC pulse shape is u(t) - u(t-0.5T_s), which exhibits a discontinuity at $t = 0.5T_s$. While NRZ and RZ pulses are predominantly used in modulators, alternative pulse shapes such as sine-shaped and exponential decaying pulses have been explored to mitigate sensitivity to jitters [32–35]. Therefore, for generality, we design our method to be applicable to the modulators with arbitrary feedback pulse shapes. By using arbitrary pulse shapes, the effect of circuit non-idealities on the feedback waveform can be taken into the account. As a result, the equations can be adopted for feedback waveform transformation. This adaptability is particularly advantageous for selecting various feedback pulses that may not be easily expressible in the s-domain, facilitating their use with the impulse invariance technique. Subsequently, we extend our approach to a more generalized structure as proposed in [11, 31] and illustrated in Fig. 1(c), which clarify the theoretical conditions necessary for maintaining an ideal SNR.

The remainder of the paper is organized as follows. In Section 2, we describe our approach intuitively and demonstrate the sequence of compensation steps. Section 3 focuses on the analytical extraction of equations for compensation parameters. Building on the insights gained in the previous sections, Section 4 extends the conventional ELD compensation method to accommodate blocks with delays exceeding one clock cycle in the feedback path. The validity of derived equations is assessed through simulations in Section 5. Section 6 provides a discussion on the results obtained, offering insights and interpretations. Finally, Section 7 serves as conclusion of the paper, summarizing the key concepts.

2. Time domain approach to ELD compensation

Both noise-shaping and oversampling techniques are used in CT ΣΔMs to reduce the quantization noise significantly [1,36]. Quality of noise-shaping in a ΣΔM is primarily determined by the transfer function of loop filter and its output values at sampling instances [1,3]. ELD alters these values from the ideal case, thereby degrading the performance of modulator and its SNR. The main purpose of compensation methods is to match the ideal and non-ideal loop filter outputs at sampling instances. In most of CT ΣΔMs, the loop filter is implemented using OTA-RC Structures [1,3,37].

While many publications achieve this purpose by investigating the frequency domain transfer function of the loop filters, our approach is different. We accomplish this task by comparing loop filters output samples in time domain. This approach leverages two key strategies that significantly reduce the complexity of procedure and make the extraction of equations more straight-forward. Firstly, we decompose the loop filter of the modulator to single-input chains of integrators (COIs), which are compensated independently. Secondly, we implement a progressive correction of integrators output in each chain, which thereby simplifying the error behavior in subsequent integrators of the chain (as analytically investigated in Section 3). Ultimately, the compensated loop filter is obtained by combining the modified COIs. In the following, we describe this procedure conceptually.

Consider the loop filter depicted in Fig. 2(a). For simplicity, we can represent this loop filter as a combination of cascaded COIs as illustrated in Fig. 2(b). Additionally, we assume a rectangular NRZ DAC as shown in

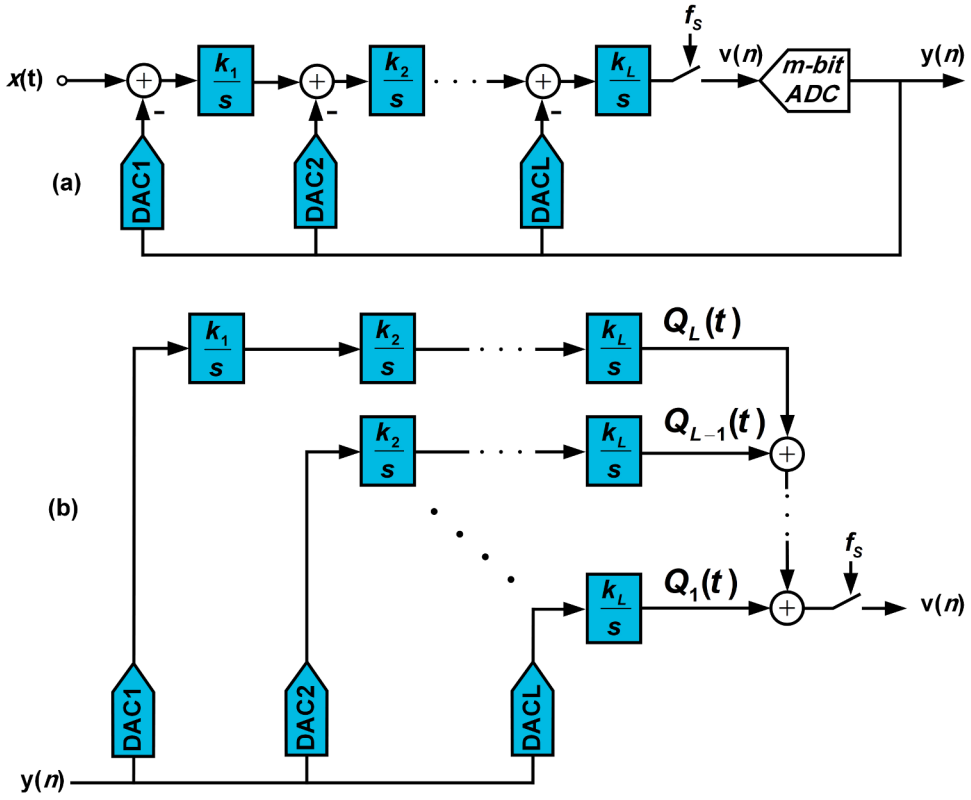

Fig. 2. (a) An L-th order ΣΔ modulator. (b) Decomposition of modulator to single input chains of integrators.

Fig. 3(a), to simplify the analysis. However, in Section 3, equations will be extracted based on an arbitrary DAC pulse shape. Applying the first strategy mentioned previously, our proposed procedure involves compensating each COI individually.

Fig. 3(b) illustrates the impulse-response of a 1st-order COI (containing one integrator) in both the ideal case and at the presence of ELD. Due to the loop delay (t_d), the first sample is reduced and does not match with the ideal case. However, the subsequent samples of the delayed loop step response align exactly with the ideal case. By applying a direct path from the DAC output to the COI output with an appropriate gain, the error in the first sample of the chain can be corrected. This adjustment ensures the proper noise-shaping performance and retrieves the SNR, as shown in Fig. 4(a).

Expanding on this concept, the output of a 2nd-order COI in both the ideal case and with ELD is presented in Fig. 3(c). In addition to the first sample error observed in 1st-order COI, there is now an offset error for all other samples due to history of 2nd integrator. To address this, we

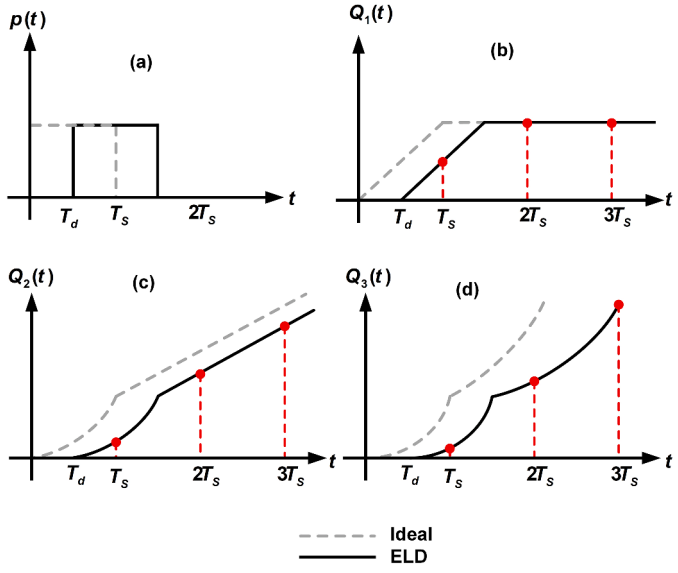

Fig. 3. Input and output signal of integrators. (a) NRZ input pulse. (b) 1st order COI output. (c) 2nd order COI output. (d) 3rd order COI output.

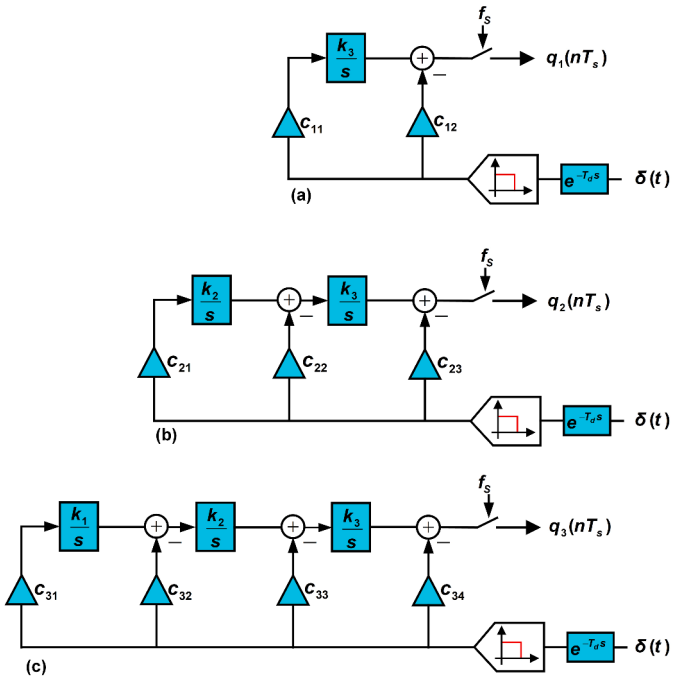

Fig. 4. Compensated COIs. (a) 1st order. (b) 2nd order. (c) 3rd order.

introduce a correction path to second integrator input with an appropriate gain of c_{22}, as depicted in Fig. 4(b). This correction compensated for the offset error in sample after the first sample. Subsequently, we correct the error in first sample by introducing another path to the chain output with a gain of c_{23}. It is important to note that the addition of the path containing c_{22} affects the error of the first sample, necessitating the recalculation of c_{23}.

Now, let us consider the 3rd order chain as a more general case. Fig. 3 (d) displays the output of the chain in both ideal and non-ideal cases. Unlike lower-order chains, the output errors at sampling instances increase over time and cannot be treated as a simple offset error. To address this complexity, we employ our 2nd strategy in the compensation procedure for chains with orders greater than two. In this case, we first compensate for the offset error at the 2nd integrator output of this COI for samples beyond $n > 1$ using a path containing c_{32}, as depicted in Fig. 4(c). Analytical equations derived in the rest of this section demonstrate that adding c_{32} transforms the increasing error of 3rd integrator into a constant error, similar to 2nd order COIs. This constant error can further be corrected with an additional path containing c_{33}, as shown in Fig. 4(c).

Finally, we correct the error of the first sample by using a direct path from DAC output to the chain output with an appropriate gain of c_{34}. Following these steps and super-positioning the modified COIs result in the compensated loop filter, as illustrated in Fig. 5, where we have:

$$\begin{aligned} k_{C1} &= c_{31} \\ k_{C2} &= c_{21} + c_{32} \\ k_{C3} &= c_{11} + c_{22} + c_{33} \\ k_{C4} &= c_{12} + c_{23} + c_{34} \end{aligned} \tag{1}$$

It is worth mentioning that Fig. 4(c) represents the compensated chain of three integrators, while Fig. 5 illustrates the compensated loop filter of modulator with a feedback structure. In ideal case, all k_{ci} are equal to unity.

3. Extraction of equations

We define $I^{n}_{T0,T1}(g(t))$ as the n-th order definite integral of g(t) over [T_0, T_1], i.e.:

$$I^{n}_{T_0,T_1}(g(t)) = \int_{T_0}^{T_1}\int_{T_0}^{t_{n-1}} \cdots \int_{T_0}^{t_1} g(t_0)dt_0 \ldots dt_{n-2}dt_{n-1} \tag{2}$$

Consequently, for g(t) = C, where C is a constant value, it can be shown that:

$$I^{n}_{T_0,T_1}(C) = CI^{n}_{0,T_1-T_0}(1) = C\frac{(T_1 - T_0)^n}{n!} \tag{3}$$

Now consider the chain of M ideal integrators depicted in Fig. 6(a), which receives a time-limited signal at its input, similar to the feedback pulse shape in ΣΔM shown in Fig. 3(a). Additionally, the compensated chain is illustrated in Fig. 6(b). Our objective is to determine the coefficients c_1 to c_{M+1} such that the output of two chains become equal at sampling instances, $t = nT_S$. It is important to note that the input pulse causes a discontinuity at the output of integrators. For $t \le T_S$, the output of each integrator can be calculated by directly integrating of the input

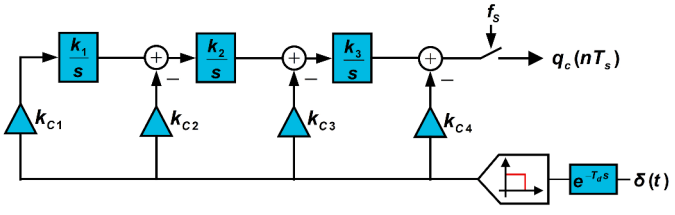

Fig. 5. Combination of compensated COIs.

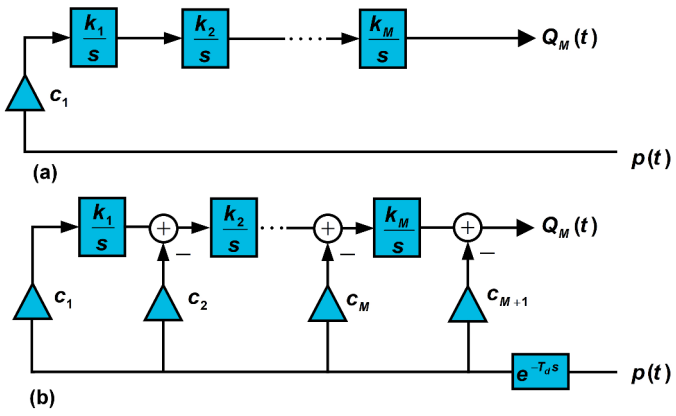

Fig. 6. General form of m-th order (a) ideal COI, and (b) modified COI.

signal. However, for $t > T_S$, additional considerations are required. Let us denote $Q_i(T_S)$ to be the output of i th integrator at time T_S, i.e.:

$$Q_i(T_s) = c_1\left(\prod_{j=1}^{i} k_j\right) I^{i}_{0,T_s}(p(t)) \tag{4}$$

The output of 1st integrator reaches its maximum value at time T_S and remains constant thereafter its input is zero for $t > T_S$. However, this constant value continues to contribute to the output of subsequent integrators, causing their outputs to increase over time. Therefore, at any time greater than T_S, the output of 2nd integrator comprises two components. The first component is the 2nd order integration of input pulse over [0, T_S], and the second is the integration of the constant output of 1st integrator. Mathematically, this can be expressed as:

$$Q_2(t) = \begin{cases} c_1k_1k_2I^{2}_{0,t}(p(t)) & t \le T_S \\ Q_2(T_S) + k_2I^{1}_{T_S,t}(Q_1(T_S)) & t > T_S \end{cases} \tag{5}$$

where $Q_2(t)$ represents the output value of 2nd integrator over time. The output of 3rd integrator, denoted as $Q_3(t)$, can be calculated by integrating (5). Therefore, we have:

$$Q_3(t) = \begin{cases} c_1k_1k_2k_3I^{3}_{0,t}(p(t)) & t \le T_S \\ Q_3(T_S) + k_3I^{1}_{T_S,t}(Q_2(T_S)) & \\ \quad + k_2k_3I^{2}_{T_S,t}(Q_1(T_S)) & t > T_S \end{cases} \tag{6}$$

Intuitively, for $t > T_S$, the output of 3rd integrator comprises three components:

1. Direct 3rd order integration of input pulse.
2. 2nd order integration of first integrator output at instance $t = T_S$.
3. 1st order integration of 2nd integrator output at instance $t = T_S$.

Given that $Q_i(T_S)$ is a constant value according to (3), we can modify (6) as follows:

$$Q_3(t) = \begin{cases} c_1k_1k_2k_3I^{3}_{0,t}(p(t)) & t \le T_S \\ Q_3(T_S) + k_3Q_2(T_S)\dfrac{(t - T_S)^1}{1!} & \\ \quad + k_2k_3Q_1(T_S)\dfrac{(t - T_1)^2}{2!} & t > T_S \end{cases} \tag{7}$$

Finally, by substitution of $Q_i(T_S)$ from (4), we have:

$$Q_3(t)=\begin{cases} c_1k_1k_2k_3I^3_{0,t}(p(t)) & t\le T_S \\ c_1k_1k_2k_3I^3_{0,T_S}(p(t)) & \\ \quad +k_1k_2k_3I^2_{0,T_S}(p(t))\dfrac{(t-T_S)^1}{1!} & t>T_S \\ \quad +k_1k_2k_3I^1_{0,T_S}(p(t))\dfrac{(t-T_S)^2}{2!} & \end{cases} \tag{8}$$

By expanding the (8) to m-th order COI, we have:

$$Q_m(t)=\begin{cases} c_1\left(\prod_{j=1}^{m}k_j\right)I^m_{0,t}(p(t)) & t\le T_S \\ c_1\prod_{j=1}^{m}k_j\left(\sum_{p=1}^{m}I^p_{0,T_S}(p(t))\dfrac{(t-T_S)^{m-p}}{(m-p)!}\right) & t>T_S \end{cases} \tag{9}$$

As previously mentioned, in a CT ΣΔM, the output values at sampling instances determine the noise-shaping ability. Hence, our intuitive approach focuses on correcting the loop filter outputs at the sampling points. The sampled output of integrators can be obtained by replacing $t = nT_S$ into (9), i.e.:

$$Q_m(nT_s)=\begin{cases} c_1\left(\prod_{j=1}^{m}k_j\right)I^m_{0,T_S}(p(t)) & n=1 \\ c_1\prod_{j=1}^{m}k_j\left(\sum_{p=1}^{m}I^p_{0,T_S}(p(t))\dfrac{((n-1)T_s)^{m-p}}{(m-p)!}\right) & n>1 \end{cases} \tag{10}$$

Going through Eqs. (4) to (10) considering a delayed input pulse $p(t-T_d)$, where $T_d < T_S$, leads to an analytical equation for sampled output of the integrators in non-ideal case as follows:

$$Q^d_m(nT_s)=\begin{cases} c_1\left(\prod_{j=1}^{m}k_j\right)I^m_{0,T_S-T_d}(p(t)) & n=1 \\ c_1\prod_{j=1}^{m}k_j\left(\sum_{p=1}^{m}I^p_{0,T_S}(p(t))\right. & \\ \quad \left.\times\dfrac{((n-1)T_S-T_d)^{m-p}}{(m-p)!}\right) & n>1 \end{cases} \tag{11}$$

Using (10) and (11), we can calculate the error at different nodes and sampling instances:

$$E_m(n)=Q_m(nT_s)-Q^d_m(nT_s) \tag{12}$$

As mentioned in Section II, we initiate compensation for samples $n > 1$. Using (12), errors at the output of integrators 1 to 3 for $n > 1$ are given by:

$$E_1(n>1)=0 \tag{13}$$

$$E_2(n>1)=c_1k_1k_2I^1_{0,T_S}(p(t))\times T_d \tag{14}$$

$$E_3(n>1)=c_1k_1k_2k_3\left[I^2_{0,T_S}(p(t))\times T_d+I^1_{0,T_S}(p(t))(n-1)T_ST_d-I^1_{0,T_S}(p(t))\frac{T_d^2}{2}\right] \tag{15}$$

According to (13), for $n > 1$, a delay less than T_S has no effect on the 1st integrator output since the error is equal to zero, while (14) shows that the delay leads to a constant error for 2nd integrator. Furthermore, the second term in (15) indicates that error at the 3rd integrator output increases linearly with time.

We will investigate this error after compensating 2nd integrator output to prove our 2nd strategy mentioned in Section II. To begin our compensation procedure, we aim to determine the compensating coefficient c_2 at 2nd integrator input. To preserve generality, we assume $p_2(t)$ as the feedback pulse shape at 2nd integrator input. Integrating this pulse multiplied by c_2 over T_S results in a constant value at the output of 2nd integrator, which should be equal to the offset error in (14), Therefore, we have:

$$\begin{aligned} k_2c_2I^1_{0,T_S}(p_2(t))=E_2(n>1)&=c_1k_1k_2I^1_{0,T_S}(p_1(t))\times T_d \\ c_2&=c_1k_1\frac{I^1_{0,T_S}(p_1(t))}{I^1_{0,T_S}(p_2(t))}\times T_d \end{aligned} \tag{16}$$

Adding c_2 affects the 3rd integrator output, or more generally, adding any coefficient c_i alters the subsequent integrators output. Therefore, to account for the effect of compensating coefficients, relation (11) must be modified as (17).

$$Q^d_m(nT_s)=\begin{cases} \sum_{i=1}^{m}c_i\prod_{j=i}^{m}k_jI^{m+1-i}_{0,T_S-T_d}(p_i(t)), & n=1 \\ \sum_{i=1}^{m-1}c_i\prod_{j=i}^{m}k_j & \\ \times\left(\sum_{p=1}^{m-i+1}I^p_{0,T_S}(p_i(t))\dfrac{((n-1)T_s-T_d)^{m-i-p+1}}{(m-i-p+1)!}\right), & n>1 \end{cases} \tag{17}$$

Where to calculate the output of the m-th integrator, the effects of coefficients c_1 to c_{m-1} have been considered. Recalculation of (15) using (17) and substitution of c_2 from (16) results in:

$$E_3(n>1)=c_1k_1k_2k_3\left[I^2_{0,T_S}(p_1(t))\times T_d+I^1_{0,T_S}(p_1(t))\frac{T_d^2}{2}-\frac{I^1_{0,T_S}(p_1(t))}{I^1_{0,T_S}(p_2(t))}I^2_{0,T_S}(p_2(t))T_d\right] \tag{18}$$

The value of above equation does not vary over time, which serves as the proof of our 2nd strategy that the compensation path at any integrator input changes the increasing error of the subsequent integrator to a constant offset, i.e. $E_m(n > 1) = E_m(2)$. Therefore, c_M can be calculated as:

$$\begin{aligned} k_mc_mI^1_{0,T_S}(p_m(t))&=E_m(2) \\ c_m&=\frac{E_m(2)}{k_mI^1_{0,T_S}(p_m(t))} \end{aligned} \tag{19}$$

where $E_m(2)$ is the result of substituting of (10) and (17) into (12), Eq.

(19) can be rewritten as (20).

$$c_m = \left(c_1 \prod_{j=1}^{m-1} k_j \left(\sum_{p=1}^{m} I^{p}_{0,T_S}(p_1(t)) \frac{{T_s}^{m-p}}{(m-p)!} \right) - \sum_{i=1}^{m-1} c_i \prod_{j=i}^{m-1} k_j \sum_{p=1}^{m-i+1} I^{p}_{0,T_S}(p_i(t)) \frac{(T_s - T_d)^{m-i-p+1}}{(m-i-p+1)!} \right) \times \frac{1}{I^{1}_{0,T_S}(p_m(t))} \tag{20}$$

Using relations (19) and (20), the coefficients c_1 to c_M can be calculated in a progressive process. The Addition of these coefficients corrects the output of chain for $t > 2T_S$. The final step is determining the fast loop coefficient, c_{M+1}, such that it compensates the chain output error at the instance $t = T_S$. To do so, c_{M+1} must be equal to the difference between chain outputs in the ideal case and ELD case at $t = T_S$, considering all preceding compensation coefficients, according to (21).

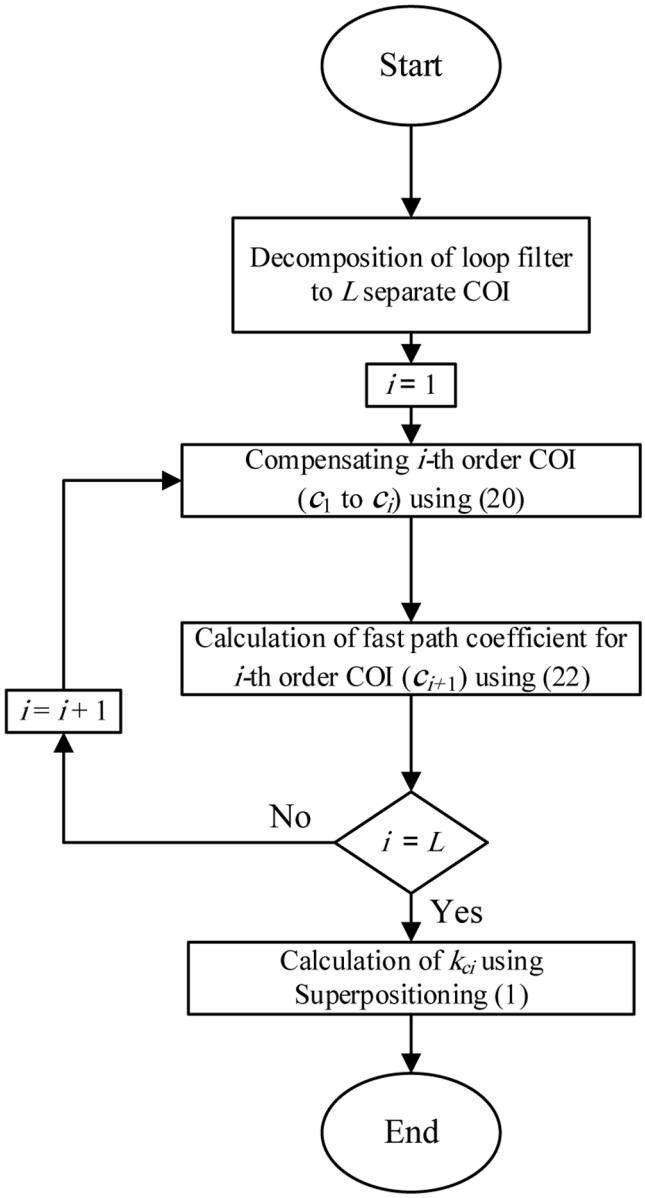

Fig. 7. Flowchart of the compensation procedure.

Substitution of the relations (10) and (17) into (21) results in (22). By (20) and (22), all unknown parameters of Fig. 6(b) can be calculated.

$$c_{M+1} = Q_M(T_s) \quad - Q^{d}_{M}(T_s) \tag{21}$$

$$c_{M+1} = c_1 \prod_{j=1}^{M} k_j I^{M}_{0,T_S}(p_1(t)) - \sum_{i=1}^{M} c_i \prod_{j=i}^{M} k_j I^{M+1-i}_{0,T_s-T_d}(p_i(t)) \tag{22}$$

According to these equations, to calculate the coefficients, we only need time information of feedback pulses. Therefore, we can compensate the modulators in which the feedback pulse cannot be represented in frequency domain (a case where traditional method is not applicable). Additionally, the time information can be easily calculated considering the non-idealities that affect the feedback pulse shape.

Another point of flexibility in this procedure is the possibility of choosing different pulse shape for each feedback path. Furthermore, the equations can be used to change the feedback pulse shape in a modulator. This means that if there is an ideal modulator for which the coefficients are determined for a standard NRZ DAC, we can easily calculate the coefficients of an equivalent modulator with a feedback pulse shape different from the main modulator, simply by using the time information of new pulses in (20).

In summary, the compensation procedure involves the following steps, illustrated in Fig. 7:

1. Decomposition of the modulator's loop filter to separate COIs, as shown in Fig. 2.
2. Calculation of coefficients c_1 to c_M shown in Fig. 6 using (20) for the 1st COI.
3. Calculation of coefficient c_{M+1} shown in Fig. 6 using (22) for 1st COI.
4. Repeating steps 2 and 3 for all other COIs.
5. Combining the compensated COIs to obtain the modified filter, shown in Fig. 5 using (1).

4. Extended ELD compensation

Digital correction methods, such as DEM, can cause more delays in the loop, which destabilizes the modulator, particularly in high-speed applications where T_s can be smaller than the DEM block delay. Although the classic ELD compensation technique is a good way to

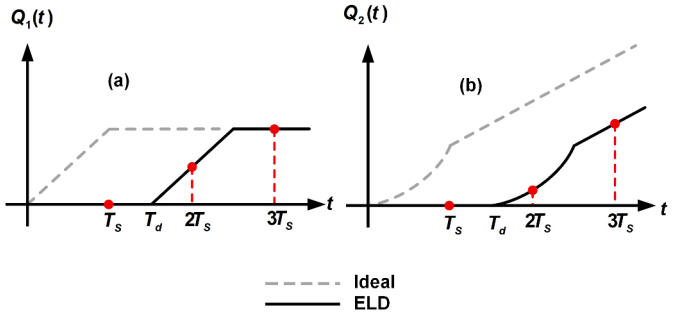

Fig. 8. (a) 1st integrator, and (b) 2nd integrator output in a 2nd order COI with an input signal delayed more than one clock cycle.

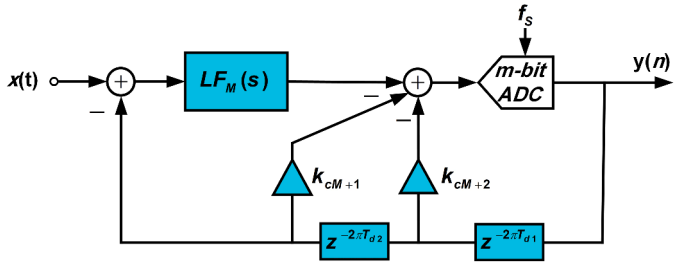

Fig. 9. Extended ELD compensation structure.

restore the SNR, it fails to compensate for the modulators that$T_d > T_s$. Therefore, employing some methods capable of compensating for the modulator with ELD exceeding one clock cycle is crucial. The method introduced to compensate the ELD more than one clock cycle in Fig. 1(c) cannot retrieve SNR as it is in the classic compensation method. In this section, we extend the analysis of the last section to propose a two-step method that is as effective as the classic ELD compensation at retrieving SNR and also compensating for delays longer than a clock cycle.

As mentioned in Section 3, c_{M+1} in Fig. 6(b) is responsible for correcting the chain output error at instance $t = T_s$. Hence, the quantizer output must be available in less than a clock cycle to compensate for loop filter's first sample.

Although the coefficients c_1 to c_M alter the calculation of c_{M+1}, their main purpose is the correction of the chain's output for $t \geq 2T_S$. Therefore, it seems they can be injected into the chain after a delay of more than one clock cycle.

Now consider the 2nd order COI, regarding a delay of more than one clock cycle at its input pulse. The output of integrators in this condition is illustrated in Fig. 8. In this case, the outputs at sample $n = 1$ is absolutely zero since there is no pulse at the chain's input. For subsequent samples, the output behavior is similar to the case discussed in Section 3. Again, we can compensate errors at $t \geq 3T_S$ and $t = 2T_S$ by injection of a delayed input pulse with appropriate gains to the 2nd integrator input and chain's output, respectively. Although the effect of the delay can be fully compensated for samples $n \geq 2$, it is inevitable to have a path with a delay less than one cycle to create the first sample at the chain output. This procedure results in a structure that can be assumed to be a general case of the method proposed in [11] and is shown in Fig. 9. Based on the aforementioned approach, to have a fully compensated chain (equivalently a fully compensated modulator without any degradation in performance) T_{d1} and T_{d2} must meet the following conditions.

$$\begin{aligned} &T_{d1} < T_S \\ &T_S < T_{d1} + T_{d2} < 2T_S \end{aligned} \tag{23}$$

An important property in structure of Fig. 9 is that the output of the fast loop is directly injected to the quantizer input (the point with the highest immunity to noise), while the pulse of the outermost feedback to the modulator input (the point at which errors directly appear at the modulator output) by the slow path.

This property can be beneficial in high-resolution ΣΔM in which DEM is used to compensate for DAC nonlinearity. The slow path in Fig. 9 can accommodate a more relaxed DEM in a way that the maximum

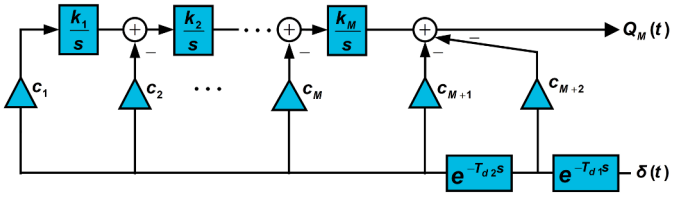

Fig. 10. Compensated COI for delay more than one clock cycle.

sampling rate of the modulator is limited only by quantizer-DAC delay. This is in contrast to traditional structures in which the maximum rate limit is determined by the total delay of quantizer, DAC, and DEM block. However, to overcome the speed limit imposed by the quantizer and considering the highest noise-shaping performance at the quantizer input, in [11] the fast loop has been implemented by a sample and hold circuit bypassing the quantizer. Additionally, [13] uses time information available through interleaved channel coupling to realize the fast loop. In the rest of this section, we will derive systematic equations to calculate the compensation coefficients based on our intuitive approach. Again, we just discuss compensating a general COI and final modulator can be achieved by super-positioning of the compensated COIs.

Consider the chain in Fig. 10, where the conditions specified in (23) are satisfied. Our objective is to determine c_2 to c_M, c_{M+1}, and c_{M+2} such that the chain's output matches that of the ideal chain shown in Fig. 6(a) at instances $t > 2T_S$, $t = 2T_S$, and $t = T_S$, respectively. Once again, we can compute the output values of integrators in the ideal case using (10). However, for delays $T_S < T_d < 2T_S$, we adjust (17) as in the relation (24).

$$Q_m^d(nT_s) = \begin{cases} 0, & n = 1 \\ \sum_{i=1}^{m} c_i \prod_{j=i}^{m} k_j I_{0,2T_S-T_d}^{m+1-i}(p_i(t)), & n = 2 \\ \sum_{i=1}^{m-1} c_i \prod_{j=i}^{m} k_j \\ \times \left(\sum_{p=1}^{m-i+1} I_{0,T_S}^{p}(p_i(t)) \frac{((n-1)T_s - T_d)^{m-i-p+1}}{(m-i-p+1)!} \right), & n > 2 \end{cases} \tag{24}$$

Utilizing this equation, we can compute the compensation coefficients for setup depicted in Fig. 10. Since c_2 to c_M are responsible for rectifying errors at samples $n > 2$, we have:

$$\begin{aligned} c_m = \Bigg(& c_1 \prod_{j=1}^{m-1} k_j \left(\sum_{p=1}^{m} I_{0,T_S}^{p}(p_1(t)) \frac{(2T_S)^{m-p}}{(m-p)!} \right) \\ & - \sum_{i=1}^{m-1} c_i \prod_{j=i}^{m-1} k_j \sum_{p=1}^{m-i+1} I_{0,T_S}^{p}(p_i(t)) \frac{(2T_S - T_d)^{m-i-p+1}}{(m-i-p+1)!} \Bigg) \times \frac{1}{I_{0,T_S}^{1}(p_m(t))} \end{aligned} \tag{25}$$

$$c_m = \frac{E_m(3)}{k_m I_{0,T_S}^{1}(p_m(t))} \tag{26}$$

$$\begin{aligned} c_{M+1} &= E_M(2) \\ c_{M+1} &= c_1 \prod_{j=1}^{M} k_j \left(\sum_{p=1}^{M} I_{0,T_S}^{p}(p_1(t)) \frac{T_s^{m-p}}{(M-p)!} \right) \\ &\quad - \sum_{i=1}^{M} c_i \prod_{j=i}^{M} k_j I_{0,2T_s-T_d}^{M+1-i}(p_i(t)) \end{aligned} \tag{27}$$

$$\begin{aligned} c_{M+2} &= E_M(1) = Q_M(T_S) \\ c_{M+2} &= c_1 \left(\prod_{j=1}^{M} k_j \right) I_{0,T_S}^{M}(p_1(t)) \end{aligned} \tag{28}$$

where $E_m(3)$ can be calculated using Eqs. (10), (12), and (24). After substituting the result into (26), we obtain the relation (25) for calculating c_2 to c_M. Additionally, c_{M+1} and c_{M+2} are responsible for error correction at samples $n = 2$ and $n = 1$, respectively as we have in (27) and (28). Eqs. (25) to (28) comprehensively define the compensation coefficients in Fig. 10. These equations hold true for $T_S < T_d < 2T_S$. Additionally, relation (28) highlights that T_d does not influence the calculation of c_{M+2} and it only needs to satisfy condition (23).

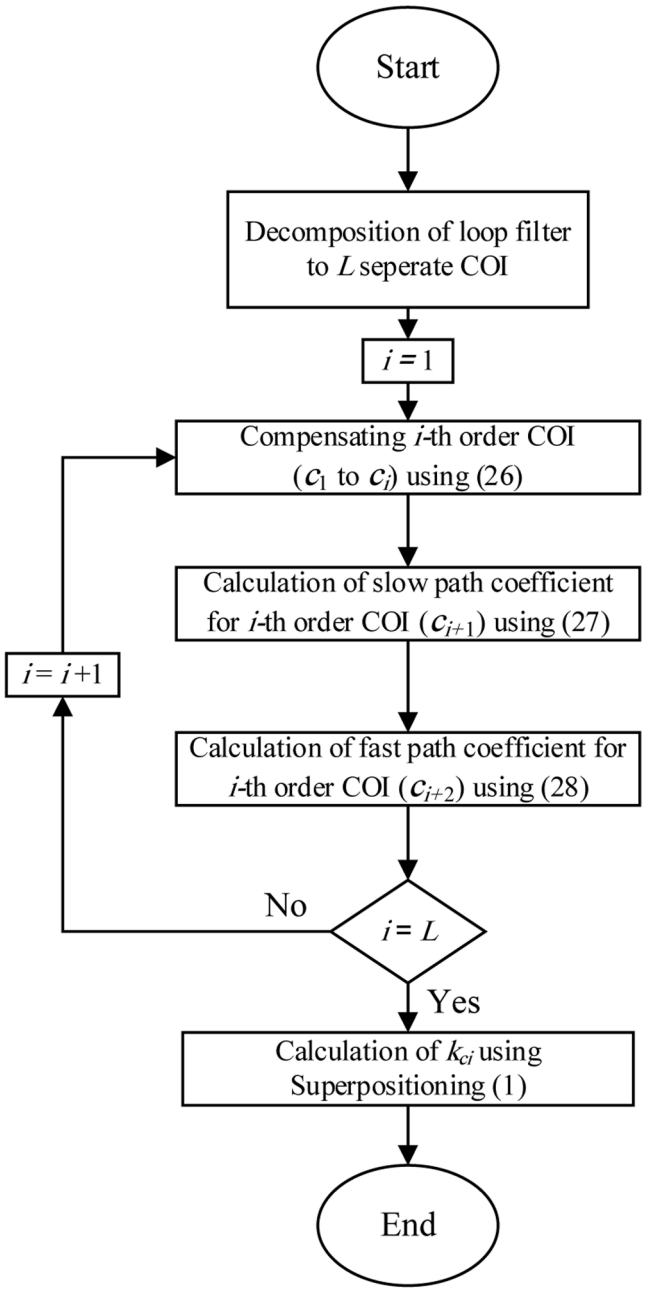

Fig. 11. Flowchart of the compensation procedure for extended ELD compensation.

In summary, the compensation procedure entails the following steps, as illustrated in Fig. 11.

1. Decompose the modulator filter to separate COIs, as depicted in Fig. 2.
2. Compute coefficients c_1 to c_M for 1st order COI shown in Fig. 10 using relation (25).
3. Determine coefficient c_{M+1} for 1st order COI shown in Fig. 10 using (27).
4. Calculate coefficient c_{M+2} for 1st order COI shown in Fig. 10 using (28).
5. Repeat steps 2 to 4 for all other COIs.
6. Combine the compensated COIs to obtain the modified filter, as illustrated in Fig. 9.

5. Simulation results

To validate the accuracy of the derived equations, both compensation schemes were applied to the loop filter of a typical modulator. The ideal and compensated filters were then simulated in MATLAB/Simulink, and the output signals were compared. Throughout this section, $T_S = 1$ is assumed.

As an example, we consider a 3rd order modulator with the structure depicted in Fig. 2(a). A 3rd-order modulator gives us a good balance between complexity and generality. Analyzing a 3rd-order modulator inherently covers the behavior of lower-order modulators. Higher-order modulators can be viewed as combinations of the lower-order stages following our step-by-step method.

In Fig. 2(a), k_1 to k_3 are equal to {0.43, 0.91, 1.55}. Simulation results of the ideal modulator in Simulink exhibit a SNR of 86.22 dB for a −3 dBFS input sine wave is depicted in Fig. 12. By decomposing the loop filter into COIs as shown in Fig. 2(b) and compensating each COI using Eqs. (20) and (22), considering $T_d = 0.75$, the results are:

$$c_{1i} = \{1, 1.1625\}$$

$$c_{2i} = \{1, 0.6825, 0.3967\}$$

$$c_{3i} = \{1, 0.3225, 0.1101, 0.0426\}$$

By summing these parameters based on (1), we can obtain the compensation coefficients for Fig. 5 as follows:

$$k_{ci} = \{1, 1.3225, 1.7926, 1.6018\}$$

Fig. 13 illustrates the loop filter impulse response in four steps, where the unity gain of feedback paths is replaced by k_{c1} to k_{c4} sequentially. As depicted in Fig. 13(b), replacing k_{c2} transforms the increasing error of the third integrator into a constant offset. Finally, in the last step, the output of the compensated filter precisely matches the ideal filter at the sampling times, as demonstrated in Fig. 13(d).

Now, let us consider the selected modulator to be compensated with the scheme depicted in Fig. 9 for $T_{d1} + T_{d2} = 1.5$. By utilizing Eqs. (25) to (28), we obtain:

$$c_{1i} = \{1, 0.775, 1.55\}$$

$$c_{2i} = \{1, 1.365, 0.8816, 0.7053\}$$

$$c_{3i} = \{1, 0.645, 0.4402, 0.2401, 0.1011\}$$

$$k_{ci} = \{1, 1.645, 2.8052, 1.8967, 2.3564\}$$

Once more, the compensating paths are incorporated into the loop filter sequentially, and the output signal is visualized in Fig. 14. The precise matching of ideal and compensated filters output at the sampling instances serves to validate the accuracy of the proposed equations. Finally, the systematic simulated spectra of both the ideal and the compensated modulators are depicted in Fig. 12. SNDR value in the compensated modulator is close to the ideal modulator with an error of 0.24 dB This demonstrates that the SNDR value can be retrieved after compensating $1.5T_S$ delay without increasing the OSR or the order of the modulator.

6. Discussions

Considering the general model of the 3rd order modulator, depicted in Fig. 15(a) with a feedback structure, in the ideal case, k_{c2} and k_{c3} are set to unity, while k_{c4} and k_{c5} are zero. However, as the delay increases, the value of k_{c2} and k_{c3} deviate from unity. In the case of traditional ELD compensation, where the ELD is less than one clock period, k_{c5} becomes non-zero value. For extended compensation case, both k_{c4} and k_{c5} takes a non-zero value. Table 1 lists the coefficients for five different cases, considering a modulator with k_1 to k_3 equal to {0.43, 0.91, 1.55}, and T_S

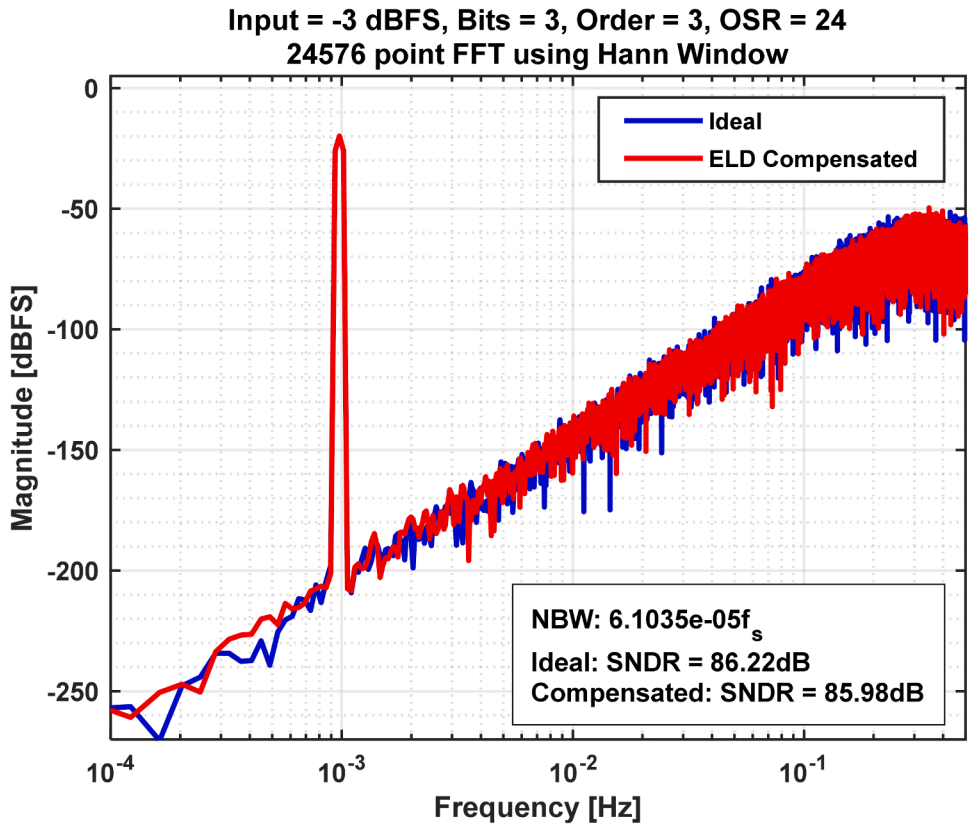

Fig. 12. Simulated spectrum of selected 3rd-order modulator using Simulink with −3 dBFS input signal for both ideal case and ELD compensated.

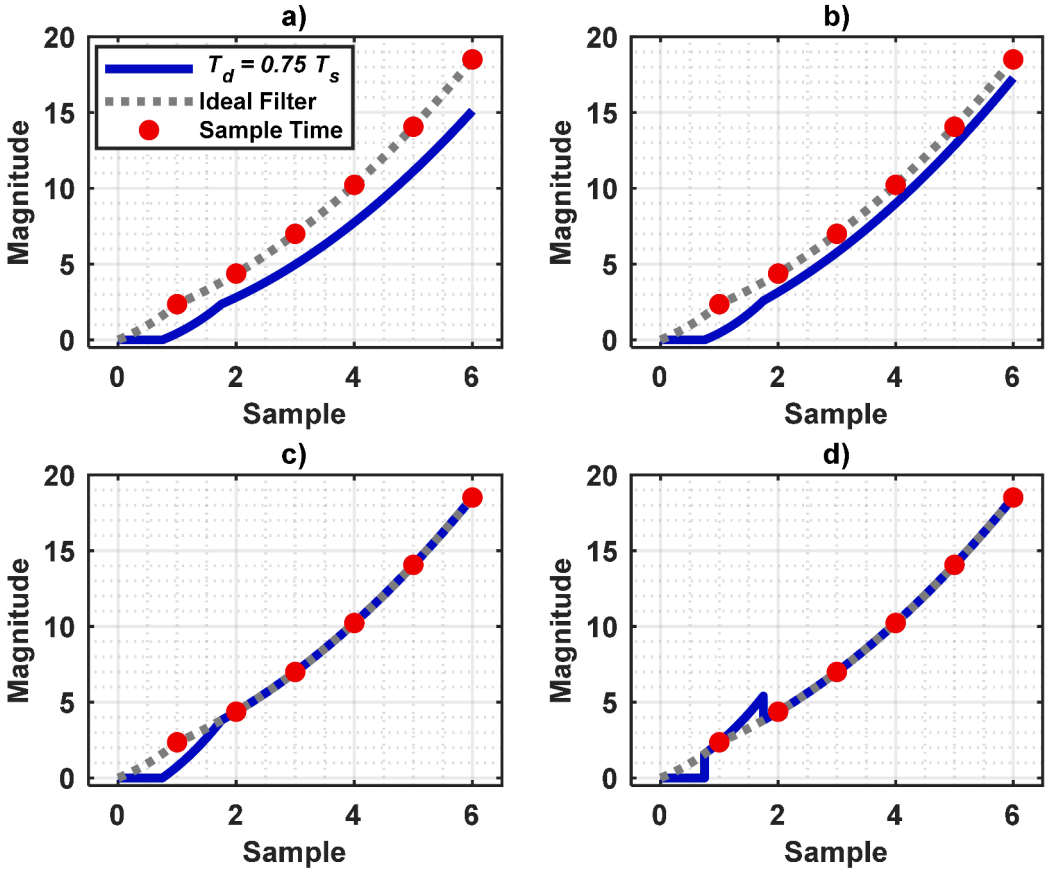

Fig. 13. Loop filter output (a) before compensation, (b) after adding 2nd integrator input, (c) after adding 3rd integrator input, and (d) after adding fast path.

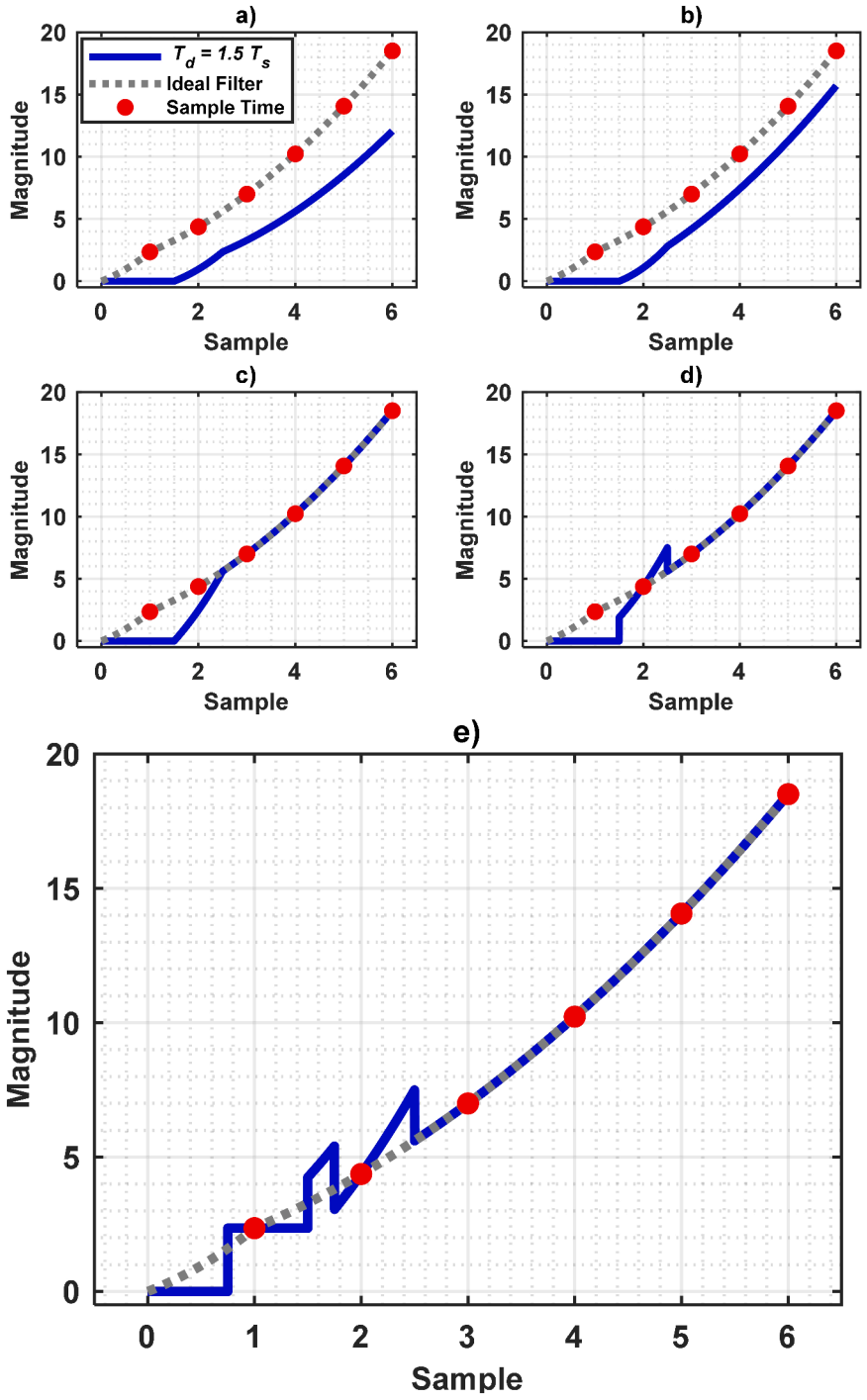

Fig. 14. Loop filter output (a) before compensation, (b) after adding 2nd integrator input, (c) after adding 3rd integrator input, (d) after adding slow path (e) after adding fast path.

= 1.

As previously discussed, the primary purpose of the investigated compensation techniques is to maintain the NTF performance identical to that of the ideal case. The STF of a CT ΣΔM can be calculated by the multiplying the feed-forward transfer function from the input of the modulator to the quantizer by the NTF. By substituting $s = j2\pi f$ in the former and $z = exp(j2\pi f/f_S)$ in the latter components of the STF, its magnitude can be plotted against frequency. For the modulator shown in Fig. 15(a), the STF is expressed as in (29).

$$STF(f) = \frac{k_1 k_2 k_3}{s^3} NTF(z)\Big|_{\substack{s = j2\pi f \\ z = \exp(j2\pi f/f_S)}} \tag{29}$$

Since the feed-forward transfer function is independent of k_{ci}, and the NTF is expected to remain identical in both ideal and compensated modulators, the compensation procedure does not impact the STF of a ΣΔ modulator with the feedback structure.

The modulator depicted in Fig. 15(a) can be recognized as a feed-forward structure, as illustrated in Fig. 15(b), while preserving the same NTF. This preservation can be validated by computing the open-

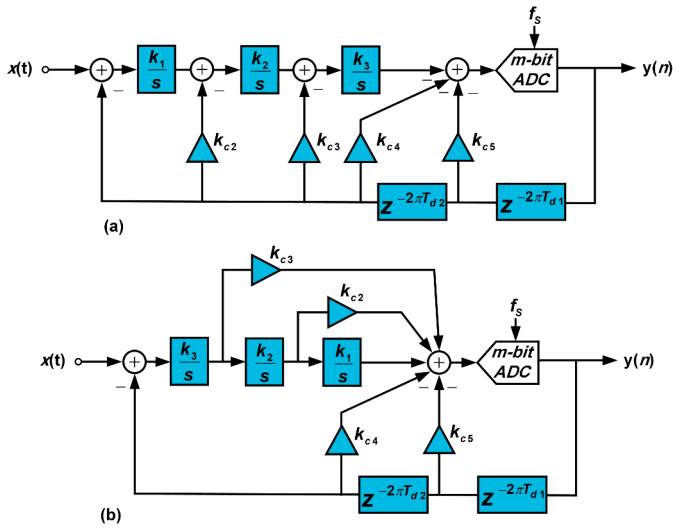

Fig. 15. General model of 3rd-order ΣΔ modulator with (a) feedback and (b) feed-forward structures.

Table 1
Compensation coefficients of 3rd order modulator for different values of ELD.

T_{d1}	$T_{d1}+T_{d2}$	k_{c2}	k_{c3}	k_{c4}	k_{c5}
0.25	0	1.107	1.240	0	0.433
0.75	0	1.323	1.793	0	1.602
< 1	1.25	1.538	2.443	0.881	2.356
< 1	1.75	1.753	3.192	3.058	2.356

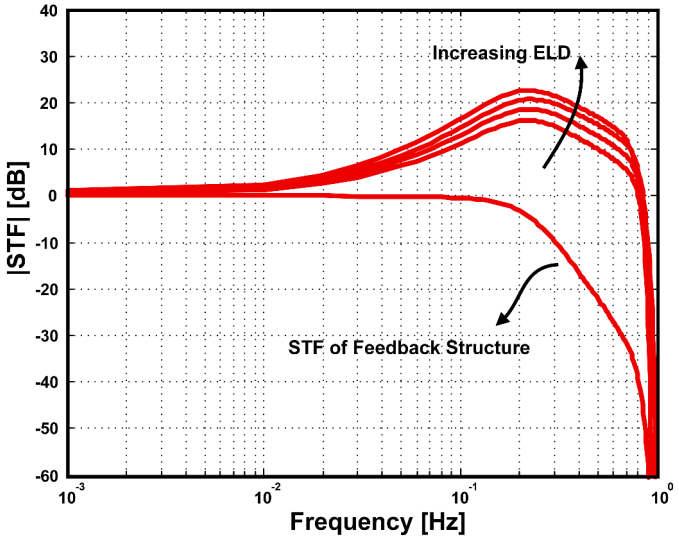

Fig. 16. STF variations of feed-forward modulator in ideal case, $T_d = 0.25$, $T_d = 0.75$, $T_d = 1.25$ and $T_d = 1.75$.

loop transfer function from the quantizer output to its input in both configurations. In this case, the STF can be approximated as:

$$STF(f) = \left(\frac{k_{c3}k_3}{s} + \frac{k_{c2}k_2k_3}{s^2} + \frac{k_1k_2k_3}{s^3}\right) \times NTF(z)\Big|_{\substack{s = j2\pi f \\ z = \exp(j2\pi f/f_S)}} \tag{30}$$

The magnitude of the STF in the feed-forward modulator is influenced by the values of k_{c2} and k_{c3}. To explore the variations in the STF within a feed-forward configuration, the corresponding STFs for the scenarios outlined in Table 1 have been plotted as shown in Fig. 16. This figure also includes the STF of feedback structure for comparison. Notably, the STF of the feed-forward modulator exhibit a peaking in magnitude, that increases in alignment with ELD.

7. Conclusions

Most existing studies evaluate their compensation method on specific modulators tailored to certain applications. This variability poses a challenge in comparing different compensation techniques. Nevertheless, we try to highlight the strengths and weaknesses of available methods.

In this paper, we have investigated the traditional ELD compensation technique in time domain to propose a systematic procedure for calculating the loop filter parameters. Traditional calculation methods based on adding fast path around quantizer can theoretically retrieve SNR value properly for delays less than a clock cycle. Prior works mostly rely on the frequency domain representation of modulator and the feedback DAC pulse shape [1,3,22,30,31]. As a result, these methods are only applicable to certain structures, and the complexity of calculations increases with variations in impulse response of the feedback DAC.

The limitations of frequency domain methods and the necessity to adjust the loop filter coefficients have led to increased interest in alternative approaches such as adaptive solution [19,20] and time-domain methods [21–31]. While high-order ELD compensation using an adaptive scheme [20] offers potential advantageous, it also increases complexity. On the other hand, time-domain methods are generally less complex and can be easily used for systematic analysis. Additionally, [31] demonstrates that for DAC pulses with the identical area and delay, there is no requirement to recalibrate the loop filter coefficients. However, it may encounter limitations when dealing with pulses exhibiting discontinuities like RZ. Furthermore, it only can compensate for one clock cycle. Additionally, a Bitwise approach like [25,26], relies on traditional methods or digital domain compensation methods, which could not be applicable to certain architectures or modulators with different types of quantizers.

The equations derived in this paper offer more versatility compared to previous methods, as they are applicable to any arbitrary feedback pulse shape. All that is needed is the feedback pulse time information, allowing for consideration of the non-idealities affecting the pulse shape. The proposed procedure enables the choice of different pulse shapes for each feedback path and facilitates the alteration of the feedback pulse shape in a modulator. For instance, if there is an ideal modulator designed for a standard NRZ DAC, the coefficients can be easily recalculated for an equivalent modulator with a different feedback pulse shape. Subsequently, we extended our intuitive approach to structures accommodating more than one clock cycle of ELD, a capability not achievable with traditional ELD compensation technique shown in Fig. 1(b). This feature has been utilized in prior works such as [11–14], albeit without any systematic design procedure or proper retrieval of in-band SNR similar to traditional method. Furthermore, designing a fast-settling sample-and-hold circuit for high-speed applications would be power-intensive, as illustrated in Fig. 1(c).

Moreover, our proposed procedure is highly systematic and suitable for integration with existing software design tools. In comparison to optimization-based approach like [23], our method offers greater flexibility in feedback pulse selection even for custom DAC pulses or feedbacks with different pulse shapes. Our approach is faster, and requires less hardware resources. Finally, there is no limitation on the order and architecture of the modulator.

CRediT authorship contribution statement

Reza Kohandel: Writing – original draft, Validation, Software, Methodology, Investigation, Formal analysis, Conceptualization. **Mohammad Yavari:** Writing – review & editing, Visualization,

Supervision, Project administration, Methodology, Investigation, Funding acquisition, Formal analysis, Conceptualization.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

No data was used for the research described in the article.

References

[1] S. Pavan, R. Schreier, G.C. Temes, Understanding Delta-Sigma Data Converters, 2nd Edition, Wiley/IEEE Press, New York, 2017.

[2] M. Pietzko, J. Wagner, A. Abdelaal, J.G. Kauffman, M. Ortmanns, Influence of excess loop delay on the STF of continuous-time delta-sigma modulators, in: 2021 IEEE International Symposium on Circuits and Systems (ISCAS), Daegu, Korea, 2021.

[3] M. Ortmanns, F. Gerfers, *Continuous-time Sigma-Delta A/D Conversion*, Springer, 2005.

[4] M. Keller, A. Buhmann, J. Sauerbrey, M. Ortmanns, Y. Manoli, A comparative study on excess-loop-delay compensation techniques for continuous-time ΣΔ modulators, IEEE Trans. Circuits Syst. I, Reg. Papers 55 (11) (2008) 3480–3487. Dec.

[5] B. Benabes, M. Keramat, R. Kielbasa, A methodology for designing continuous-time sigma–delta modulators, in: Proc. Eur. Des. Test Conf. 1, 1997, pp. 46–50.

[6] G. Mitteregger, et al., A 14 b 20 mW 640 MHz CMOS CT ΔΣ ADC with 20 MHz signal bandwidth and 12 b ENOB, in: Proc. IEEE Int. Solid-State Circuits Conf, 2006, pp. 131–140. Feb.

[7] S. Kim, S.-I. Na, Y. Yang, S. Kim, A 2-MHz BW 82-dB DR continuous-time delta–sigma modulator with a capacitor-based voltage DAC for ELD compensation, IEEE Trans. on Very Large Scale Integration (VLSI) Systems 26 (10) (2018) 1999–2006. Oct.

[8] C. Zhang, et al., Current-mode multi-path excess loop delay compensation for GHz sampling CT ΣΔ ADCs, in: IEEE International Symposium on Circuits and Systems (ISCAS), Baltimore, MD, 2017, pp. 1–4. May.

[9] M. Zhou, et al., A 2 GHz 0.98 mW 4-bit SAR-Based Quantizer with ELD Compensation in an UWB CT ΣΔ Modulator, in: IEEE International Symposium on Circuits and Systems (ISCAS), May 2018, pp. 1–5.

[10] C.-Y. Ho, C. Liu, C.-L. Lo, H.-C. Tsai, T.-C. Wang, Y.-H. Lin, A 4.5 mW CT Self-Coupled ΔΣ Modulator With 2.2 MHz BW and 90.4 dB SNDR Using Residual ELD compensation, IEEE J. Solid-State Circuits 50 (12) (Dec. 2015) 2870–2879.

[11] V. Singh, N. Krishnapura, S. Pavan, Compensating for quantizer delay in excess of one clock cycle in continuous-time ΔΣ modulators, IEEE Trans. Circuits Syst. II, Exp. Briefs 57 (9) (Sept. 2010) 676–680.

[12] V. Singh, et al., A 16 MHz BW 75 dB DR CT ΔΣ ADC compensated for more than one cycle excess loop delay, IEEE J. Solid-State Circuits 47 (8) (Aug. 2012) 1884–1895.

[13] Y. Hu, H. Venkatram, N. Maghari, U.-K. Moon, Continuous-time ΔΣ ADC utilizing time information for two cycles of excess loop delay compensation, IEEE Trans. Circuits Syst. II, Exp. Briefs 62 (11) (2015) 1063–1067.

[14] S. Tan, L. Sundström, M. Palm, S. Mattisson, P. Andreani, A 5 GHz CT ΔΣ ADC with 250 MHz signal bandwidth in 28 nm-FDSOI CMOS, in: IEEE Nordic Circuits and Systems Conference (NORCAS): NORCHIP and International Symposium of System-on-Chip (SoC), Helsinki, Finland, 2019, pp. 1–4. Oct. 2019.

[15] H. Hu, M. Li, Z. Dai, F. Ye, J. Ren, A 15MHz BW continuous-time ΔΣ modulator with high speed digital ELD compensation, in: IEEE International Conference on ASIC (ASICON), Guiyang, 2017, pp. 686–689.

[16] P. Fontaine, A.N. Mohieldin, A. Bellaouar, A low-noise low-voltage CT ΔΣ modulator with digital compensation of excess loop delay, in: *IEEE International Digest of Technical Papers, Solid-State Circuits Conference*, 2005.

[17] C.E. Lokin, D. Schinkel, R.A.R. Van Der Zee, B. Nauta, Compensating processing delay in excess of one clock cycle in noise shaping loops without altering the filter topology, IEEE Access 9 (2021) 108101–108111.

[18] Y.-K. Cho, A single op-amp resonator-based continuous-time sigma–delta modulator with time-division switching for excess loop delay compensation, IEEE Trans. Circ. Syst. II: Expr. Briefs 71 (4) (2024) 1789–1793.

[19] S. Ho, C.-L. Lo, J. Ru, J. Zhao, A 23 mW, 73 dB dynamic range, 80 MHz BW continuous-time delta-sigma modulator in 20 nm CMOS, IEEE J. Solid-State Circuits 50 (4) (2015) 908–919.

[20] K. El-Sankary, H.H. Alamdari, E.I. El-Masry, An adaptive ELD compensation technique using a predictive comparator, IEEE Trans. on Circ. Syst. II: Expr. Briefs 56 (8) (2009) 619–623.

[21] S. Pavan, Excess loop delay compensation in continuous-time delta-sigma modulators, IEEE Trans. Circuits Syst. II, Exp. Briefs 55 (11) (2008) 1119–1123.

[22] J. Talebzadeh, I. Kale, A general formula for impulse-invariant transformation for continuous-time delta-sigma modulators, in: Conference on Ph.D. Research in Microelectronics and Electronics (PRIME), 2017, pp. 261–264.

[23] T. Brückner, C. Zorn, J. Anders, J. Becker, W. Mathis, M. Ortmanns, A GPU-accelerated web-based synthesis tool for CT sigma-delta modulators, IEEE Trans. Circ. Syst. I Regular Papers 61 (5) (2014) 1429–1441.

[24] J. Wagner, R. Ritter, M. Ortmanns, Using to rapidly obtain ELD compensated CT ΣΔ modulators, in: IEEE International Symposium on Circuits and Systems (ISCAS), Montreal, QC, 2016, pp. 1498–1501. www.sigma-delta.de.

[25] M. Pietzko, J. Ungethüm, J.G. Kauffman, Q. Li, M. Ortmanns, Bitwise ELD compensation in ΔΣ modulators, in: 2022 IEEE International Symposium on Circuits and Systems (ISCAS), 2022.

[26] M. Pietzko, J. Ungethüm, J.G. Kauffman, M. Ortmanns, Delay error shaping in ΔΣ modulators using time-interleaved high resolution quantizers, IEEE Trans. on Circuits and Systems I: Regular Papers 70 (7) (2023) 2700–2710.

[27] Z. Xu, K. Xing, Y. Zhu, R.P. Martins, C.-H. Chan, An ELDC-free 4th-order CT SDM facilitated by 2nd-Order NS CT-SAR and AC-Coupled Negative-R, IEEE J. Solid-State Circuits 59 (3) (2024) 753–764.

[28] J. Bell, M.P. Flynn, A simultaneous multiband continuous-time ΔΣ ADC with 90-MHz aggregate bandwidth in 40-nm CMOS, in: European Solid State Circuits Conference (ESSCIRC), Cracow, Poland, 2019, pp. 1–4.

[29] T.-P. Bui, et al., A 5th-order Configurable-Frequency Direct Delta-Sigma Converter for Mobile Application, in: International Conference on Advanced Technologies for Communications (ATC), Hanoi, Vietnam, 2019, pp. 292–296.

[30] J. Cherry, W. Snelgrove, Excess loop delay in continuous-time delta-sigma modulators, IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process. 46 (4) (1999) 376–389.

[31] S. Pavan, Continuous-time delta-sigma modulator design using the method of moments, IEEE Trans. on Circ. Syst. I Regular Papers 61 (6) (2014) 1629–1637.

[32] S. Luschas, H.-S. Lee, High-speed modulators with reduced timing jitter sensitivity, IEEE Trans. Circ. Syst. II: Analog Digital Signal Process. 49 (11) (2002) 712–720.

[33] D. Feng, F. Maloberti, S.-W. Sin, S.-P. U, R.P. Martins, Jitter-resistant capacitor based sine-shaped DAC for continuous-time sigma-delta modulators, in: 2014 IEEE International Symposium on Circuits and Systems (ISCAS), 2014, pp. 1348–1351.

[34] A. Ashry, D. Belfort, H. Aboushady, Phase Noise Effect on Sine-Shaped Feedback DACs Used in Continuous-Time ΣΔ ADCs, IEEE Trans. on Circ Syst I: Regular Papers 62 (3) (2015) 717–724.

[35] N. Beilleau, C. Ouffoue, H. Aboushady, Sinusoidal RF DACs for undersampled LC bandpass ΣΔ modulators, in: 2007 50th Midwest Symposium on Circuits and Systems, 2007, pp. 1477–1480.

[36] F. Colodro, J.L. Mora, F. Barrero, M.R. Arahal, J.M. Martinez-Heredia, Analysis and simulation of a novel speed estimation method based on oversampling and noise shaping techniques, Results in Eng 21 (Mar. 2024) 1–9.

[37] D. Sharma, V. Nath, CMOS operational amplifier design for industrial and biopotential applications: comprehensive review and circuit implementation, Results in Eng 22 (2024) 1–14.