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MIXED SIGNAL LETTER

An efficient threshold voltage generation for SAR ADCs

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Abstract In this paper, a new architecture for successive-approximation register (SAR) analog-to-digital converters (ADCs) is presented. In the proposed scheme, the threshold voltage for each comparison is divided into two parts. This results in appreciably less switching energy and less total capacitance without a substantial increase in digital complexity compared to the conventional SAR ADC. Analytical calculations and circuit level simulation results in the context of a 10-bit 100 kS/s ADC are provided to verify the usefulness of the proposed SAR ADC scheme revealing 87 % less switching power and 40 % less total capacitance in comparison with the conventional SAR ADC.

Keywords Analog-to-digital converters · Successive-approximation register ADCs · Charge redistribution DACs · SAR logic

1 Introduction

In mixed-signal systems, the analog-to-digital converters (ADCs) are needed to serve as the link between the analog and digital worlds. There are several ADC structures such as flash, pipeline, and successive-approximation register (SAR), and each ADC configuration is suitable for some specific applications. SAR ADCs have a moderate speed and moderate resolution with low power consumption. Therefore, they are one of the most suitable architectures for applications such as biomedical sensor interfaces and wireless sensor networks.

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SAR ADCs are composed of three major parts including one comparator, one digital-to-analog converter (DAC), and a digital controller. Many efforts have been performed to improve the performance of these building blocks. With respect to the conventional switching technique, the split-capacitor scheme [1] and the energy-saving technique [2], without any reduction in total capacitance, achieve 37 and 56 % reduction in switching energy, respectively. However, these switching schemes improve the switching power consumption at the cost of increased digital switching complexity and power. The monotonic switching scheme [3] achieves 81 % reduction in switching power and 50 % reduction in total capacitance. In [4] by designing the comparator in time domain, the power consumption of the ADC is reduced. In the recently published paper [5], by using dual power supply for digital and analog sections, the total power consumption of the ADC is reduced. There are several other schemes such as [6] and [7] in which the switching power of DAC has been appreciably reduced. However, these schemes are parasitic sensitive. Besides, in these techniques, the digital section is much more complex than the conventional one.

One of the most important parts of a SAR ADC is the capacitive DAC where a significant proportion of the power consumption and silicon die area is consumed. In this paper, by focusing on DAC section, a new SAR ADC scheme is proposed. In the proposed structure, by dividing the threshold voltage into two parts, the power consumption and the total capacitance of DAC are appreciably reduced without a significant increase in the digital switching complexity. The rest of this paper is organized as follows. Section 2 briefly explains the conventional SAR ADC operation. In Sect. 3, the operation of the proposed SAR ADC is presented. Circuit level simulation results are provided in Sect. 4 and finally Sect. 5 concludes the paper.

2 Conventional SAR ADC

The detailed function of a conventional SAR ADC is explained in [8] and it is briefly reviewed here. Figure 1 shows the circuit of a conventional SAR ADC where the binary search algorithm is used in switching procedure. At the sampling time, the bottom plate of all capacitors is switched to V_{in} and their top plate is connected to the ground, and hence, the input signal is sampled. In the holding phase, the switch S_{R1} is open and the bottom plate of all capacitors is connected to the ground. So, in this phase, the top plate voltage of all capacitors (V_+) becomes $-V_{\text{in}}$. In the first comparison, the bottom plate of the largest capacitor (C_N) is switched to V_{REF} making the top plate voltage of the capacitors to become ($-V_{\text{in}} + V_{\text{REF}}/2$). Therefore, in the first comparison, the input signal is compared with $V_{\text{REF}}/2$. If $V_{\text{in}} > V_{\text{REF}}/2$, the most significant bit (MSB), B_1, is 1 and in addition to C_N, the bottom plate of C_{N-1} is also switched to V_{REF}. Hence, V_+ becomes ($-V_{\text{in}} + 3V_{\text{REF}}/4$). But, if $V_{\text{in}} < V_{\text{REF}}/2$, B_1 is 0 and the bottom plate of C_N is reconnected to the ground and the bottom plate of C_{N-1} is switched to V_{REF} resulting in V_+ as ($-V_{\text{in}} + V_{\text{REF}}/4$). Therefore, depending on the first bit, in the second comparison, V_{in} is compared with $3V_{\text{REF}}/4$ or $V_{\text{REF}}/4$. The ADC repeats this procedure until the least significant bit (LSB), B_{N}, is decided. After sampling and holding phases, the input signal is estimated in N cycles by comparing it with N threshold voltages where N is the ADC's resolution.

As is clear, in each comparison, with respect to the previous cycle, the threshold voltage is changed by adding or subtracting a binary weighted fraction of the reference voltage to or from the previous threshold voltage. When a binary weighted fraction of V_{REF} is added to or subtracted from the threshold voltage, an Up or a Down transition is happen, respectively. Since in a conventional SAR ADC for any transition in the threshold voltage, some charges are consumed from the reference voltage, all transitions are power consuming. On the other hand, the energy consumption of Up and Down transitions is not equal and the later consumes much more power than the former [1]. For some cases, a Down transition consumes five times more energy than an Up transition [1]. In addition to these points, since the DAC energy consumption is related to charging and discharging of the DAC capacitors, it is obvious that the switching power consumption is proportional to the total DAC capacitance. In the proposed SAR ADC presented in the next section, by dividing the threshold voltage into two parts, firstly, the number of power consuming transitions is roughly reduced by 50 %. Secondly, all Down transitions are omitted. Finally, the total capacitance is roughly 40 % reduced. Therefore, the total switching power consumption of the proposed SAR ADC is significantly reduced.

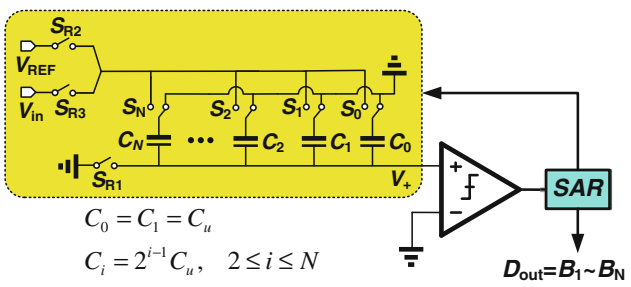

Fig. 1 Conventional SAR ADC

3 Proposed SAR ADC scheme

In a conventional SAR ADC, the required threshold voltage to generate the ith bit (B_{i}) is $V_t[i] = (\alpha/2^i)V_{REF}$ where B_1 is the MSB and $1 \le \alpha \le 2^i - 1$. By dividing the threshold voltage as the sum of two parts, V_X and V_Y, we have:

$$V_t[i] = V_X[i] + V_Y[i]. \tag{1}$$

It is proved later that considering $V_X[i]$ and $V_Y[i]$ as the following equations makes a good efficiency in the generation of threshold voltages:

$$V_X[i] = \begin{cases} 0 & i = 1 \\ V_X[i-1] & 2 \le i \le N \& B_{i-1} = 0 \\ V_t[i-1] & 2 \le i \le N \& B_{i-1} = 1 \end{cases} \tag{2}$$

$$V_Y[i] = (1/2^i)V_{REF} \quad 1 \le i \le N. \tag{3}$$

As it will be explained later, the generation of V_X and V_Y, could be more efficient than V_t which is used in a conventional SAR ADC. The circuit of the proposed SAR ADC, which utilizes V_X and V_Y threshold voltages, is depicted in Fig. 2. As is seen, the circuit consists of two capacitive networks CNX and CNY that are corresponding

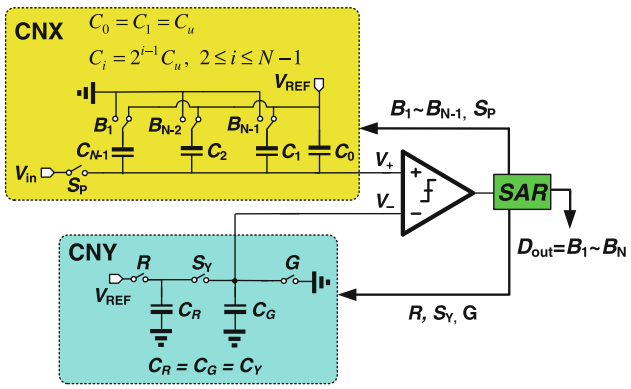

Fig. 2 Proposed SAR ADC

to V_X and V_Y threshold voltages, respectively. The operation of the proposed SAR ADC is as follows.

In the proposed scheme, each cycle is composed of three phases. These phases are Reset (Φ_{Res}), Regeneration (Φ_{Reg}) and Comparison (Φ_{Comp}), respectively. In the first bit cycle generation, at the sampling phase (the first reset phase), the input signal is sampled at CNX network. So at this time, the switch S_P is closed and the top plate of all capacitors in CNX network is charged to V_{in}. Besides, their bottom plate is connected to V_{REF}. Thus, the voltage at the positive node of the comparator (V_+) is set to V_{in}. This value of V_+ doesn't change until the first bit is produced. So, at Φ_{Reg} and Φ_{Comp} there is no change in CNX network.

In the other hand, in CNY network, at the first bit cycle generation, at Φ_{Res}, the capacitor C_R is charged with V_{REF}. Also, the capacitor C_G and the parasitic capacitor at the negative input of the comparator (C_P) are reset to the ground. After this phase, the CNY network is completely disconnected from the reference voltage, and hence, this capacitive network doesn't consume any more power. At Φ_{Reg}, the capacitors C_R and C_G are charge shared. So, the voltage on each of these two capacitors becomes $V_{\mathrm{REF}}/2$. At Φ_{Comp}, only the capacitor C_G is connected to the negative input of the comparator, and so, the voltage at the comparator negative input at Φ_{Comp} is $V_{\mathrm{REF}}/2$. Hence, at this phase, V_{in} is compared with $V_{\mathrm{REF}}/2$. If $V_{\mathrm{in}} > V_{\mathrm{REF}}/2$, the first bit ($B_1$) is 1 and if $V_{\mathrm{in}} < V_{\mathrm{REF}}/2$, B_1 is 0. This is the end of the first bit cycle. At the beginning of the second bit cycle, if $B_1 = 1$, the bottom plate of the largest capacitor in CNX network is switched to the ground and if $B_1 = 0$ there is no change in CNX network. After this, there is no change in CNX network until the second bit is generated. In CNY network, in the second bit cycle, at Φ_{Res}, only switch G is closed. So, at this phase, C_G and C_P are connected to the ground, and hence, these two capacitors are completely discharged. At this phase, the other switches in CNY network are open, and so, the voltage of C_R is not changed from the end of the previous cycle. At Φ_{Reg}, the switch S_Y is closed and the capacitors C_R and C_G are charge shared again resulting in a voltage of $V_{\mathrm{REF}}/4$ on each capacitor. At Φ_{Comp}, all switches are open and C_G is connected to the comparator negative input. So, at this phase, the corresponding comparison is performed. The function of the circuit in the other bit cycles is similar to the second bit generation. So, this procedure is repeated until the LSB is produced.

The flow chart of the proposed SAR ADC is shown in Fig. 3. As is seen, because of some differences between the first and the other Φ_{Res}, the function of CNY network at the first Φ_{Res} is remarked by Res 1 and in the other Φ_{Res} is remarked by Res 2. The function of CNY network at Φ_{Reg} and Φ_{Comp} for all cycles are remarked by Reg and Comp, respectively. In Table 1, the switching procedure of CNY network at each phase is illustrated where the closed switches in different phases are clarified. In Fig. 4, the timing diagram of the proposed SAR ADC for 10 bit resolution is illustrated. As it is clear, only three signals (R, G and S_Y) are required to control the switching procedure in CNY network. So, the digital section of the proposed SAR ADC is not much more complex and power consuming than the conventional SAR ADC.

It is worth mentioning that at Φ_{Reg}, C_P is also charge shared with C_G and C_R capacitors resulting in an error in charge dividing. To alleviate this problem, it is necessary to make C_P sufficiently smaller than the capacitors C_G and C_R. This can be satisfied by careful design of the comparator and considering a larger value for C_G and C_R respected to the C_P. It is also worth to mention that the value of capacitors C_G and C_R is determined by kT/C noise consideration, and hence, large capacitance is needed especially at higher resolutions. So, the detrimental effect of comparator input capacitance on charge sharing between the capacitors C_G and C_R is well minimized.

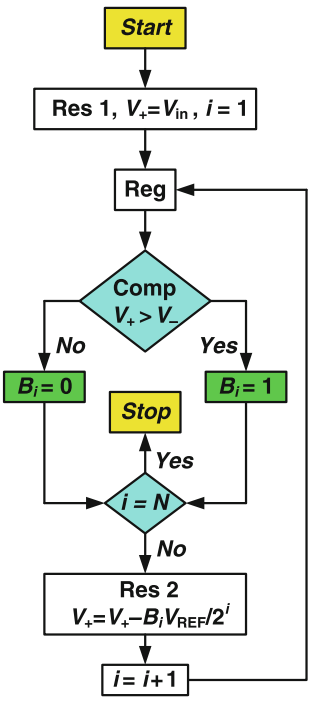

Fig. 3 Flow chart of the proposed SAR ADC

Table 1 Switching procedure in CNY network

Function name	Closed switches
Res1	G, R
Res 2	G
Reg	S_Y
Comp	None

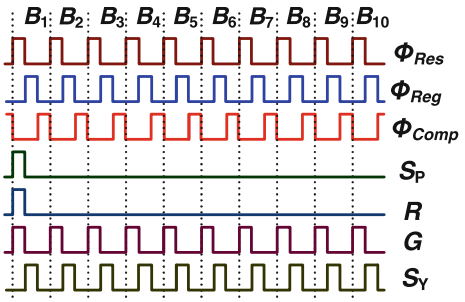

Fig. 4 Timing diagram of the proposed SAR ADC for 10 bit resolution

3.1 Switching energy of the proposed SAR ADC

As depicted in Fig. 2, the CNX network is similar to the conventional SAR DAC, but, the total capacitance is 50 % reduced and all Down transitions are omitted. So, roughly 50 % of transitions in a conventional switching procedure are eliminated. Also to generate the MSB, there is no transition in CNX network. So, with respect to the conventional DAC, the power consumption of CNX network is significantly reduced. In CNY network, only at the first Φ_{Res}, the capacitor C_R is charged with V_{REF} and after this phase, this network is disconnected from V_{REF}. Therefore, the total power consumption in CNY network is $C_Y V_{REF}^2$ where C_Y is the capacitance of C_R and C_G.

The switching energy in CNX network in each bit cycle could be calculated as follows. After the ith cycle, depending on the generated bit, the voltage of V_+ may be changed. This voltage at the end of $(i-1)$th cycle and at the beginning of the ith cycle are remarked by $V_+(t_i^-)$ and $V_+(t_i^+)$, respectively. It is obvious that $V_+(t_i^+) \le V_+(t_i^-)$. Therefore, as explained in [1], we have:

$$i = 1 \Rightarrow E(i) = 0 \tag{4}$$

$$\begin{aligned} 2 \le i \le N \Rightarrow E(i) &= V_{REF}\left[Q_i(t_i^+) - Q_i(t_i^-)\right] \\ &= C_{Ti} V_{REF}\left[V_+(t_i^-) - V_+(t_i^+)\right] \\ &= C_{Ti} V_{REF}[V_X(i) - V_X(i-1)], \end{aligned} \tag{5}$$

where $E(i)$ is the energy consumption of CNX network in the ith bit cycle. C_{Ti} is the total capacitance in CNX network which are connected to V_{REF} at the beginning of the ith bit cycle. $Q_i(t_i^-)$ and $Q_i(t_i^+)$ are the charge stored on C_{Ti} at the end of the $(i-1)$th bit cycle and at the beginning of ith bit cycle, respectively. $V_X(i)$ and $V_X(i-1)$ are defined in relation (2). According to Eqs. (2) and (5), if $B_{i-1} = 0$, the voltages $V_X(i-1)$ and $V_X(i)$ are equal, and therefore, there is no power consumption in CNX network.

A behavioral simulation of the switching power in the proposed SAR ADC for 10 bit resolution has been performed with MATLAB and the normalized switching power is depicted in Fig. 5. As is seen, the energy consumption of the proposed SAR ADC for every output code is much less than the average power of the conventional SAR ADC. The average switching power of the proposed scheme for 10 bit resolution and $C_Y = 40\ C_u$ is $167.75 C_u V_{REF}^2$ where C_u is the unit capacitance. So, in comparison with the conventional switching scheme which consumes $1365.3 C_u V_{REF}^2$, the proposed switching procedure is more than 87 % power efficient. From the systematic view, the proposed ADC and several well known techniques are compared in Table 2. It is worth to mention that in this comparison, all schemes are considered as a single-ended design. As is seen, for 10 bit resolution, the total switching power and capacitance of the proposed ADC are appreciably lower than the conventional, split capacitor [1] and energy saving schemes [2]. Although the total capacitance in the proposed ADC is slightly more than the monotonic switching scheme [3], but the total switching power consumption of the proposed technique is also lower than the monotonic switching.

3.2 Circuit implementation

A design example of the proposed SAR ADC with 10 bit resolution, 100 kS/s sampling rate, and a single-ended structure has been implemented in the circuit level to verify

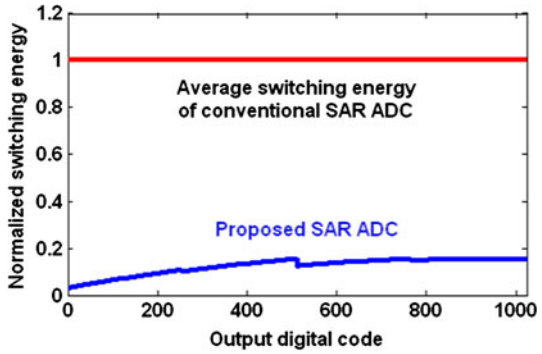

Fig. 5 Power consumption of the proposed SAR ADC scheme against digital output code for 10-bit resolution in comparison with the conventional one

Table 2 Comparison of the proposed SAR ADC with several schemes for 10 bit resolution

Switching scheme	Number of switches	Total capacitor (C_u)	Switching energy consumption ($C_u V_{\text{REF}}^2$)
Conventional	25	1,024	1365.3
Split capacitor [1]	43	1,024	852.3
Energy saving [2]	41	1,024	563.8
Set and down [3]	20	512	255.5
This work	22	592	167.75

its usefulness. The design has been performed in a 0.18 μm CMOS technology with 1 V power supply to save the power consumption. In the following, the circuit details are explained. It is worth mentioning that by using a four-input comparator, the proposed SAR ADC can be also implemented in the differential structure. Although the fully-differential structure improves several parameters such as the common-mode noise rejection and reduces the total distortion, it consumes more power and occupies more area. Therefore, in moderate resolutions, the single-ended structure can be utilized to reduce the overall power dissipation and silicon die area as well [9].

3.2.1 Comparator

The rail-to-rail comparator circuit proposed in [9] was used in this design and it is shown in Fig. 6. This topology was selected to achieve a rail-to-rail input signal range. As is seen, this comparator consists of two pMOS and nMOS input differential pairs making the possibility to increase the input signal swing up to the supply voltage. At Φ_{Comp}, when a differential input signal is applied to the comparator, the two differential pairs convert the input voltage into the current, and then, these currents are summed to run the regenerative stage. Two inverters are used to achieve full scale swing at the output nodes. Transistors M_3 and M_4 are used to reset the comparator, and hence, to reduce the comparator's hysteresis.

The main issue of using such a rail-to-rail comparator is that the comparator offset voltage may depend on the input common-mode voltage. This is because the added transconductance of nMOS and pMOS input differential pairs depends on the input common-mode voltage. At lower input common-mode voltage, the nMOS differential pair will be in the cut-off region, and on the other hand, when the input common-mode is higher, the pMOS differential pair cannot provide any current to the regenerative latch. Therefore, the input offset voltage of the comparator depends on the input common-mode voltage. To alleviate this problem, the comparator input differential pairs are designed such that the input offset voltage to be less than the needed resolution in the worst case. Besides, special layout techniques such as the common-centroid style and adding dummy devices can also be utilized. As an alternative, a constant input transconductance topology can be employed to achieve independent offset voltage on the input common-mode voltage.

It is worth mentioning that when a conventional SAR ADC implemented as single-ended with the structure shown in Fig. 1, the input common-mode voltage of the comparator is not changed. However, using such ADC in a differential structure to sample the differential input signal, the input common-mode voltage of the comparator is not fixed and it is changed during conversion. This is also happen in the proposed SAR ADC shown in Fig. 2 although it is implemented as single-ended. As mentioned above, to alleviate this problem, a constant input transconductance comparator or designing the comparator with the worst-case input offset voltage to be less than the required resolution is needed.

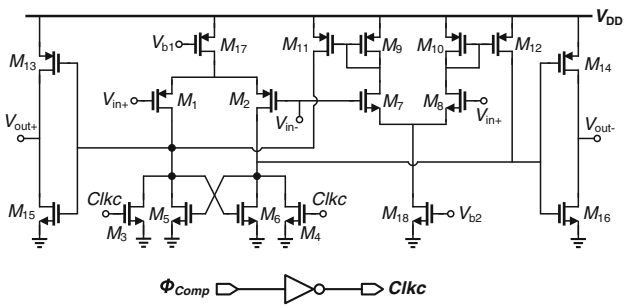

Fig. 6 Comparator circuit

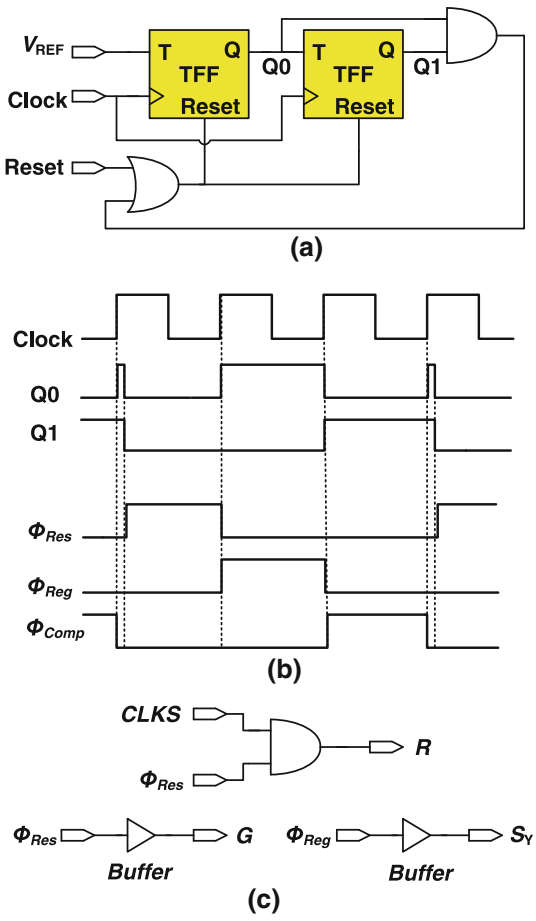

Fig. 7 **a** Logic schematic to generate Φ_{Res}, Φ_{Reg}, and Φ_{Comp} in CNY network. **b** Timing diagram, and **c** Logic of controller signals in CNY network

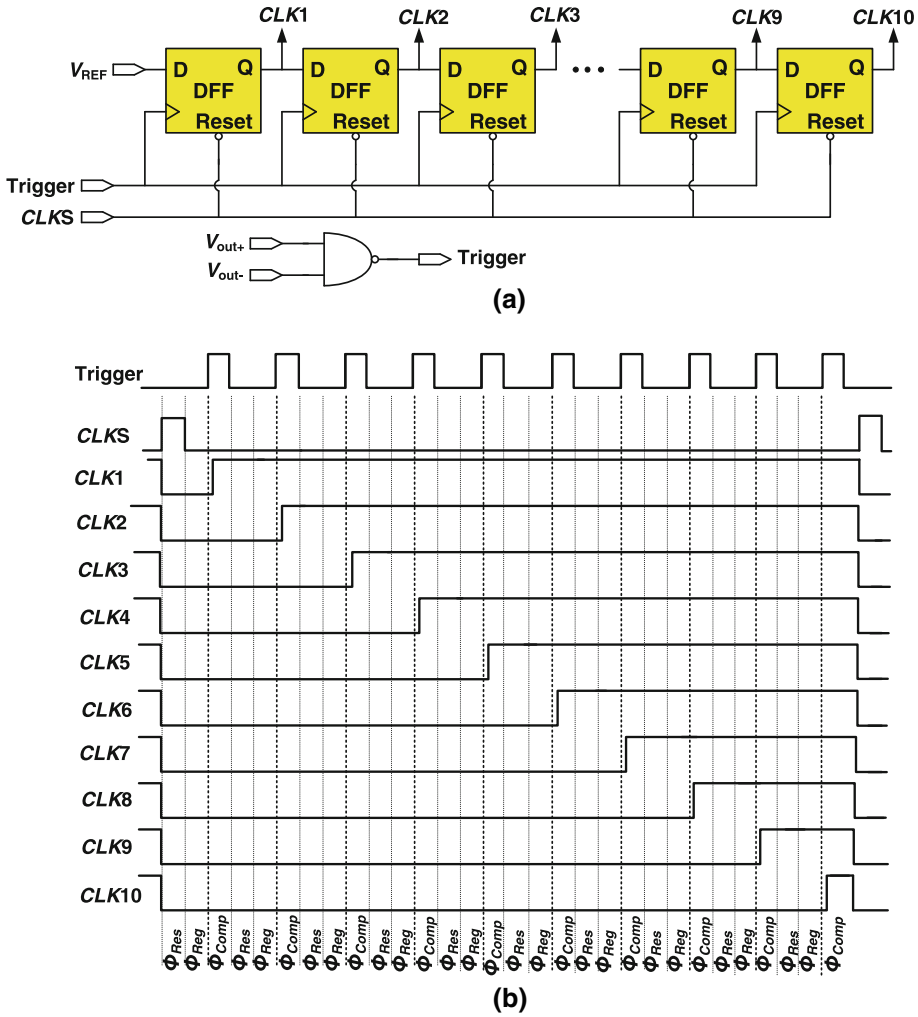

Fig. 8 Clock generation in CNX network: **a** Logic schematic, and **b** Timing diagram

3.2.2 *Successive approximation register*

The digital section is designed to control the function of the ADC. This section is divided into two parts: the digital controller of CNY and CNX networks. The digital controller of CNY network has a synchronous function. As it was mentioned before, there are three phases controlling the function of CNY network which are Φ_{Res}, Φ_{Reg} and Φ_{Comp}. Although it is not essential to allocate the equal time interval to these three phases, but for logic simplicity, the duty cycle of all these phases are equally considered. In Fig. 7, the logic schematic used to generate these phases and controller signals in CNY network is depicted. This logic consists of a two bit counter with the output value between 0 and 3 and each output number is equivalent to a phase. The numbers 0, 1, and 2 are corresponding to Φ_{Res}, Φ_{Reg} and Φ_{Comp}, respectively and number 3 is used to reset the counter. As illustrated, according to these phases, the controller signals of CNY network are produced. It is worth mentioning that the control signals used in CNY network are non-overlapping to avoid charging and discharging by V_{REF} and ground for capacitors C_R and C_G at the beginning of Reg.

According to the logic of CNY network, the digital controller of CNX network is designed. The logic of this section is very similar to which is used in [3]. In Fig. 8, the timing diagram and the logic schematic to generate the timing signals in CNX network are depicted. At the first Φ_{Res}, the controller signal of the sampling switch (*CLKS*) is high. So, at this phase, V_{in} is sampled at all capacitors in CNX network. When *CLKS* is high, the bottom plate of these capacitors is connected to V_{REF} and their top plate is switched to V_{in}. As is seen, at this time CLK_1 to CLK_{10} are low. After the first comparison, CLK_1 is high and B_1 (MSB) is determined. Depending on this bit, the bottom plate of the largest capacitor (C_{N}) is switched to ground or remains connected to V_{REF}. So, if MSB is 1, it is switched to the ground and if MSB is 0, it remains connected to V_{REF}. This is the end of the first bit generation cycle in CNX network. After this time, there is no change in CNX network until the second comparison is done. After the second comparison, CLK_2 is high and the second bit (B_2) is determined.

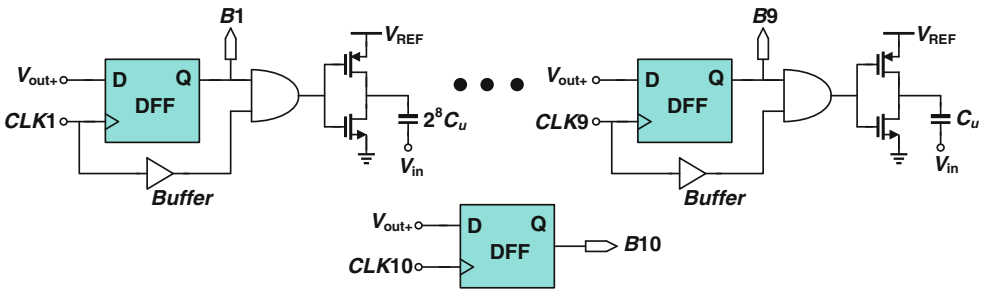

Fig. 9 Control logic in CNX network

Depending on this bit, the bottom plate of the corresponding capacitor is connected to the ground or remains connected to V_{REF}. This is the end of the second bit generation. This procedure is repeated for B_3 to B_N bits generation cycles. It is obvious that after B_N bit generation there is no need to switch any capacitor in CNX network. To implement the above procedure, the logic presented in [3] was used and it is shown in Fig. 9. As is seen, at the sampling phase, CLK_1 to CLK_{10} are low and the bottom plate of all capacitors in CNX network is switched to V_{REF}.

After each comparison, at the rising edge of the corresponding clock, the positive output voltage of the comparator derives the static flipflop and hence the relevant bit is determined. Also, as is seen, if the produced bit is 1, the bottom plate of the relevant capacitor is switched to the ground and if this bit is 0, the bottom plate of the corresponding capacitor remains connected to V_{REF}.

3.2.3 Switches

The input signal sampling switch (S_P) is implemented by the bootstrapping switch proposed in [10]. In CNY network, switches S_Y and G are implemented by nMOS transistors and switch R is implemented by a pMOS transistor. These switches are designed to have small parasitics as well as small on-resistance. This is necessary to minimize the parasitic capacitance at the comparator's negative input.

4 Simulation results

The designed ADC with 10 bit resolution and 100 kS/s sampling frequency was simulated with HSPICE using a 0.18 μm BSIM3v3 level 49 mixed-signal CMOS technology. The reference voltage is 1 V and the input voltage swing is 0.9 V peak to peak. The value of C_u is determined by some considerations such as kT/C noise, mismatch, and parasitic effects. In this design, the value of the unit capacitor in CNX network is 23 fF. In CNY network, the value of C_Y is 890 fF. So, the total DAC capacitance is as follows:

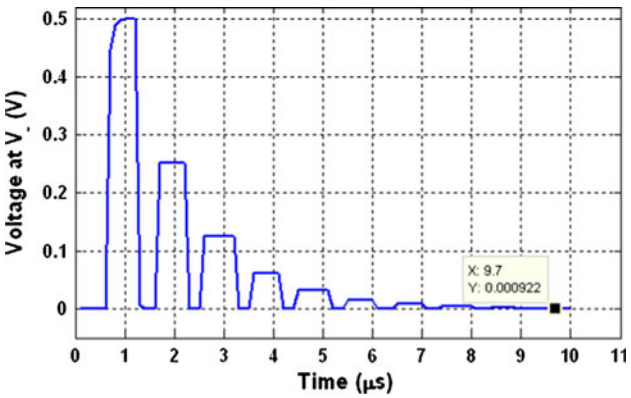

Fig. 10 Transient waveform of $V\_$

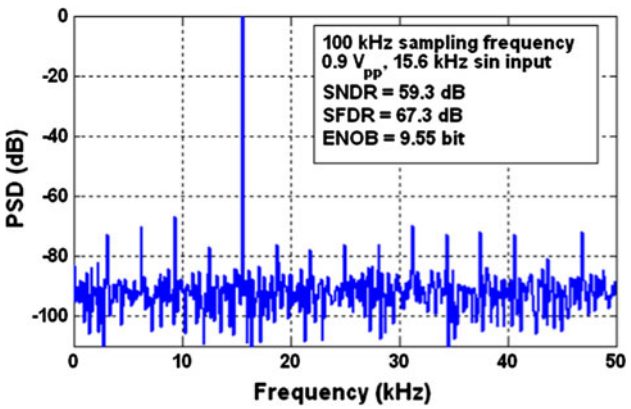

Fig. 11 Output PSD of the simulated ADC

$$C_{tot} = C_{totX} + C_{totY} = 13.55\,pF. \quad (6)$$

As it was mentioned before, it is required to reduce the parasitic effects in CNY network. To do so, firstly, the value of C_G and C_R is considered sufficiently large compared to the total parasitic capacitance at the comparator's negative input. Secondly, the dimension of the switches used in CNY network is selected as low as possible to decrease their parasitic capacitances. To show the accuracy of the CNY network output, which is applied to the comparator's negative input ($V\_$), the transient

Table 3 Comparison of the simulated SAR ADC with several references

References	Tech. (μm)	Sampling rate	Input swing V_{pp}	Power (μW)	ENOB (bit)	FoM (fJ/conversion-step)	C_{TOT} (pF)
[2]	0.18	500 kS/s	–	7.75	7.5	86	5.12
[4]	0.18	100 kS/s	0.8 V	3.8	9.4	56	16.84
[5]	0.13	1 kS/s	1 V	0.053	9.12	94.5	14.37
[9]	0.18	400 kS/s	1 V	6.15	7.31	97	6.15
[11]	0.5	1 kS/s	0.63 V	0.15	8.04	280	40.96
[12]	0.18	100 kS/s	0.6 V	1.1	8.4	40	54.2
[13]	0.18	100 kS/s	0.6 V	1.3	8.7	31	9.45
[14]	0.18	1 kS/s	0.5 V	5.1	8	19,921	–
[15]	0.13	1 MS/s	–	147.6	8.39	437	15
[16]	0.18	500 kS/s	–	42	9.4	124	–
[17]	0.18	370 kS/s	0.4 V	32	2.6	14,264	0.7
[18][a]	0.18	40 kS/s	1 V	32.6	9.4	1,206	–
[19][a]	0.18	70 kS/s	1.8 V	300	9.6	5,522	52
[20]	0.18	150 kS/s	0.5 V	30	8.27	647	20.48
[21]	0.25	1.8 MS/s	1.6 V	–	–	–	76.8
[22]	0.18	137 kS/s	1.5 V	13.4	8.65	243	102
[23]	0.18	100 kS/s	1 V	25	10.55	165	–
[24]	0.35	1 MS/s	2.4 V	2,700	9.77	3,090	–
[25]	0.18	2.5 MS/s	0.5 V	3,100	9	2,421	–
This work[a]	0.18	100 kS/s	0.9 V	6.21	9.55	82.8	13.55

[a] Simulation results

waveform of V_- during switching procedure is depicted in Fig. 10. As is seen, the value of V_- is as accurate as required. On the other hand, the procedure used to produce the comparator's positive input (V_+) is similar to the conventional SAR ADC. Therefore, the parasitic effects on V_+ are not as important as on V_-. Also, the waveform of V_+ is signal dependant and for any change in V_{in}, the waveform of V_+ is also altered.

The simulated ADC output power spectral density (PSD) is shown in Fig. 11 where a 0.9 V peak to peak, 15.6 kHz sinusoidal input signal is applied to the ADC and 1,024 points FFT is utilized. The achieved signal-to-noise plus distortion ratio (SNDR) and spurious free dynamic range (SFDR) are 59.3 dB and 67.3 dB, respectively, resulting in a 9.55 effective number of bits (ENOB). The total power consumption is 6.21 μW.

The simulated ADC is compared with several SAR ADCs in Table 3 using the following figure of merit (FoM):

$$FoM = \frac{Power}{2^{ENOB} \times f_s}, \quad (7)$$

where f_s is the sampling rate. In this Table, the area and power of all designs are considered as single-ended. As is seen, the simulated ADC achieves a good figure of merit among the published ones verifying the usefulness of the proposed SAR ADC scheme. It should be noted that although the reported results for the presented SAR ADC are based on HSPICE simulation results while most of the other ADCs are implemented on chip, but its outstanding FoM verifies its performance as a good candidate for power and area efficient SAR ADCs.

5 Conclusions

In this paper, a new SAR ADC scheme by dividing the threshold voltage into two parts was presented. By using this technique, the total capacitance and switching power are reduced without a significant increase in digital switching complexity and power. A 10 bit resolution and 100 kS/s sampling rate ADC was simulated using the proposed scheme with HSPICE in a 0.18 μm CMOS technology. The simulated ADC SNDR and SFDR are 59.3 and 67.3 dB, respectively, with 6.21 μW total power consumption and 13.55 pF total capacitance in the capacitive DAC.

References

1. Ginsburg, B. P., & Chandrakasan, A. P. (2005). An energy-efficient charge recycling approach for a SAR converter with capacitive DAC. in *IEEE International Symposium on Circuits and Systems (ISCAS)* (pp. 184–187), May 2005.
2. Chang, Y.-K., Wang, C.-K. (2007). A 8-bit 500-KS/s low power SAR ADC for bio-medical applications. in *IEEE Asian Solid-State Circuits Conference (A-SSCC)* (pp. 228–231), Nov. 2007.

3. Liu, C.-C., & Chang, S.-J. (2010). A 10-bit 50-MS/s SAR ADC with a monotonic capacitor switching procedure. *IEEE Journal of Solid-State Circuits, 45*(4), 731–740.
4. Agnes, A., Bonizzoni, E., Malcovati, P., & Maloberti, F. (2010). An ultra-low power successive approximation A/D converter with time-domain comparator. *Analog Integrated Circuits and Signal Processing, 64*(2), 183–190.
5. Zhang, D., Bhide, A., & Alvandpour, A. (2011). A 53-nW 9.12-ENOB 1-kS/s SAR ADC in 0.13-μm CMOS for medical implant devices. in *European Solid-State Circuits Conference (ESSCIRC)* (pp. 467–470) Sept. 2011.
6. Yu, W., Lin, J., & Temes, G. C. (2010). Two-step split-junction SAR ADC. *Electronics Letters, 46*(3), 211–212.
7. Lin, J., Yu, W., & Temes, G. C. (2010). Multi-step capacitor-splitting SAR ADC. *Electronics Letters, 46*(21), 1426–1428.
8. McCreary, J., & Gray, P. R. (1975). All-MOS charge redistribution analog-to digital conversion techniques Part-I. *IEEE Journal of Solid-State Circuits, SC-10*(6), 371–379.
9. Hong, H.-C., & Lee, G.-M. (2007). A 65-fJ/conversion-step 0.9-V 200-kS/s rail-to-rail 8-bit successive approximation ADC. *IEEE Journal of Solid-State Circuits, 42*(10), 2161–2168.
10. Abo, A. (1999). *Design for reliability of low-voltage, switched-capacitor circuits*. Ph.D. Dissertation, University of California, Berkeley, CA, Spring 1999.
11. Ay, S. U. (2011). A sub-1 volt 10-bit supply boosted SAR ADC design in standard CMOS. *Analog Integrated Circuits and Signal Processing, 66*(2), 213–221.
12. Kim, B., Yan, L., Yoo, J., & Yoo, H.-J. (2011). A 40 fJ/c-s 1 V 10 bit SAR ADC with dual sampling capacitive DAC topology. *Journal of Semiconductor Technology and Science, 11*(1), 23–32.
13. Lee, S.-K., Park, S.-J., Suh, Y., Park, H.-J., & Sim, J.-Y. (2009). A 1.3 μW 0.6 V 8.7-ENOB successive approximation ADC in a 0.18 μm CMOS. in *VLSI Symposium Technology Digest Papers* (pp. 242–243) June 2009.
14. Marjonen, J., Vermesan, O., & Rustad, H. (2011). An 8-bit, 10 kHz, 5.1 μW, 0.18 μm CMOS SAR ADC for RFID applications with sensing capabilities. *Analog Integrated Circuits and Signal Processing, 66*(3), 389–405.
15. Zeng, Z., Dong, C.-S., & Tan, X. (2010). A 10-bit 1 MS/s low power SAR ADC for RSSI application. in *IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT)* (pp. 569–571) Nov. 2010.
16. Pang, W.-Y., Wang, C.-S., Chang, Y.-K., Chou, N.-K., & Wang, C.-K. (2009). A 10-bit 500-KS/s low power SAR ADC with splitting comparator for bio-medical applications. in *IEEE Asian Solid-State Circuits Conference (A-SSCC)* (pp. 149–152) Nov. 2009.
17. Özgün, R., Lin, J., Tejada, F., Pouliquen, P., & Andreou, A. G. (2011). A low-power 8-bit SAR ADC for a QCIF image sensor. in *IEEE International Symposium on Circuits and Systems (ISCAS)* (pp. 841–844) May 2011.
18. Chow, H.-C., & Chen, Y.-H. (2007). 1 V 10-bit successive approximation ADC for low power biomedical applications. in *European Conference on Circuit Theory and Design (ECCTD)* (pp. 196–199) Aug. 2007.
19. Chow, H.-C., Chen, B.-W., Chen, H.-C., & Feng, W.-S. (2005). A 1.8 V, 0.3 mW, 10-bit SA-ADC with new self-timed timing control for biomedical applications. in *IEEE International Symposium on Circuits and Systems* (pp. 736–739) May 2005.
20. Sauerbrey, J., Schmitt-Landsiedel, D., & Thewes, R. (2003). A 0.5 V 1-μW successive approximation ADC. *IEEE Journal of Solid States Circuits, 38*(7), 1261–1265.
21. Rivetti, A., Anelli, G., Anghinolfi, F., Mazza, G., & Rotondo, F. (2001). A low-power 10-bit ADC in a 0.25-μm CMOS: design considerations and test results. *IEEE Transactions on Nuclear Science, 4*, 1225–1228.
22. Kim, H., Min, Y.-J., Kim, Y., & Kim, S. (2008). A low power consumption 10-bit rail-to-rail SAR ADC using a C-2C capacitor array. in *IEEE International Conference on Electron Devices and Solid-State Circuits*, Dec. 2008.
23. Verma, N., & Chandrakasan, A. P. (2006). A 25 μW 100kS/s 12b ADC for wireless micro-sensor applications. in *IEEE ISSCC Dig. Technical Papers* (pp. 222–223) Feb. 2006.
24. Confalonleri, P., Zarnprogno, M., Girardi, F., Nicollini, G., & Nagari, A. (2004). A 2.7mW 1MSps 10b analog-to-digital converter with built in reference buffer and 1LSB accuracy programmable input ranges. in *Proceeding of the 30th European Solid State Circuits Conference* (pp. 255–258) Sept. 2004.
25. Long, S.-L., Wu, J.-H., Xia, X.-J., & Shi, L.-X. (2008). A 1.8-V 3.1 mW successive approximation ADC in system-on-chip. *Analog Integrated Circuits and Signal Processing, 56*(3), 205–211.

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