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A Simple Structure for MASH ΣΔ Modulators with Highly Reduced In-Band Quantization Noise

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Abstract A new topology of multi-loop sigma-delta (ΣΔ) modulators is proposed which utilizes two analog inter-stage paths to improve the noise-shaping ability of the modulator by one order and simultaneously optimizing one pair of noise transfer function zeros. Furthermore, an improved version of this modulator is presented which is simpler to implement. So, by using minimum extra circuit and without increasing the number of active blocks, the in-band quantization noise is significantly reduced, and hence, the modulator signal-to-noise and distortion ratio (SNDR) is highly increased. As an example, a multistage noise-shaping (MASH) 2-1 ΣΔ modulator based on the improved proposed structure is more examined. Some implementation considerations including the timing issue and first-stage quantization noise extraction are verified. Theoretical analysis and simulation results in both system and circuit levels are presented to confirm the usefulness of the proposed structure. The modulator is implemented in a 90-nm CMOS technology using Spectre-RF. For 10 MHz signal bandwidth, 85.2 dB SNDR and 87 dB dynamic range are achieved, while the power consumption is 31.6 mW from a single 1 V power supply.

Keywords MASH ΣΔ modulators · Zero optimization · Noise-shaping · Switched-capacitor circuits · CMOS operational amplifiers

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1 Introduction

Sigma-delta ($\Sigma\Delta$) modulators are one of the most common analog-to-digital converters (ADCs) traditionally used in high accurate and low bandwidth applications. With no need for precise components, they can be designed to provide high signal-to-noise ratio (SNR) while consuming less power than the Nyquist rate alternatives. Recent improvements in CMOS technology scaling have made $\Sigma\Delta$ modulators also a good candidate for wideband applications like wired, wireless and mobile communication systems [35,46]. In such applications, it is of interest to enhance the SNR in the desired bandwidth without increasing the power consumption and/or the circuit complexity.

Oversampling and noise shaping are the two effective techniques to achieve high performance in sigma-delta modulators. In high-speed applications, the oversampling ratio (OSR) cannot be large. This is because of the limited increase in sampling frequency which is imposed by the technology maximum speed and acceptable power consumption [50]. So, to achieve the required high accuracies in wideband applications, the in-band quantization noise should be reduced by employing some other approaches to compensate the effect of OSR shortage. Increasing the number of quantization bits and the modulator noise-shaping order are the two common strategies that can be employed. However, the former complicates the digital-to-analog converter (DAC) linearization technique and increases the power consumption of the flash analog-to-digital converter (ADC) exponentially [49]. The latter makes instability problem in single-loop modulator structures which results in modulator performance degradation in wideband applications [5,37]. To deal with this issue, stabilization strategies have been proposed [15,24]. In addition, a cascaded sigma-delta structure may be adopted wherein digital correction filters are applied to cancel the quantization noise of the previous stages [37,54]. Multistage noise-shaping (MASH) $\Sigma\Delta$ modulators enable high-order noise shaping without any stability problem by using low- order modulators in each stage. The order of the modulator is usually determined by the number of integrators. Hence, increasing the modulator order results in more power consumption. An approach called noise coupling has been presented in [22,23,48] to increase the order of the noise shaping without increasing the number of the integrators. Utilizing this technique necessitates employing an extra DAC and an active adder before the quantizer to extract the quantization noise and inject it to the modulator again. However, there have been several attempts to simplify the circuit of the noise-coupling modulators, for example by using some delays in the loop filter [33].

Another effective approach to achieve high resolution in wideband low OSR applications is the noise transfer function (NTF) zero optimization. In this technique, by spreading the NTF zeros inside the desired bandwidth, the in-band quantization noise is reduced without increasing the number of integrators. The NTF zero optimization can be done by using local or global resonation strategies [12,14,20,35,41]. Employing the local resonation approach [12,14] for MASH $\Sigma\Delta$ modulators ($\Sigma\Delta$Ms) may affect the digital cancelation filters making their realization complicated [41]. The other zero optimization strategy called the global resonation has been presented in [20,35,41] for a MASH 2-2 $\Sigma\Delta$ modulator. In this technique, inter-stage feedback

paths are employed to optimize the NTF zeros so that the digital cancelation filters in the conventional MASH modulator do not change. Therefore, in some cases, the global resonation strategy is a better choice for MASH $\Sigma\Delta$Ms.

Recently, a novel class of MASH $\Sigma\Delta$ modulators with highly reduced in-band quantization noise has been proposed by the authors [19]. The proposed structure attains one-order higher noise-shaping ability over the modulator's order just by employing two extra analog inter-stage paths. Besides, one pair of NTF zeros is optimized only by adjusting a single coefficient. So, with a minimal extra circuit, both the noise-shaping order enhancement and NTF zero optimization are simultaneously achieved resulting in a highly reduced in-band quantization noise. So, the proposed topology is more efficient for wideband applications.

In a point of view, the proposed structure is comparable with the noise-coupling modulator. Both of them get one-order higher noise shaping over the modulator's order. But, the main priority of the former is simply achieving the zero optimization at once. This is established, whereas a usual zero optimization technique cannot be commonly applied for noise-coupled $\Sigma\Delta$ modulators. In [59], two new architectures are presented for the first- and second-order noise-coupled modulators with an NTF zero optimization. But, for the second-order one, an extra DAC is needed compared with its counterpart with no zero optimization. Furthermore, this approach is not constant for a typical noise-coupled $\Sigma\Delta$ modulator. In fact, although this technique can be extended for any order of noise shaping, the modulator structure depends on its order which may be complicated for higher-order ones. In addition, this approach is a local NTF zero optimization technique, which as mentioned before can complicate the digital cancelation filter of the MASH structure.

In this paper, firstly the theoretical analysis of the previously proposed modulator is provided in details which is missed in [19]. The authors will then discuss the difficulties associated with the circuit-level implementation of this modulator which result in a power consumption increment and/or a malfunction in timing. Therefore to deal with these practical issues, a novel structure is proposed which has a simpler circuit-level implementation. As a design prototype, a MASH 2-1 is implemented in a 90-nm CMOS process based on the newly proposed modulator. Some implementation considerations including the modulator timing issue and first-stage quantization noise extraction are presented. System- and circuit- level simulation results confirm the effectiveness of the proposed modulator.

The paper is organized as follows. In Sect. 2, the proposed MASH $\Sigma\Delta$ modulator is introduced. Analytical calculations are used to evaluate the effectiveness of the proposed modulator. Also, an improved version of the proposed modulator, its theoretical analysis and a MASH 2-1 modulator based on this structure are presented in this section. The implementation challenges of the proposed MASH 2-1 modulator including the timing diagram, first-stage quantization noise extraction and several behavioral simulation results of this modulator are presented in Sect. 3. Section 4 describes the circuit-level implementation of each individual building block used in the proposed MASH 2-1 modulator. Circuit-level simulation results with Spectre-RF and conclusions are presented in Sects. 5 and 6, respectively.

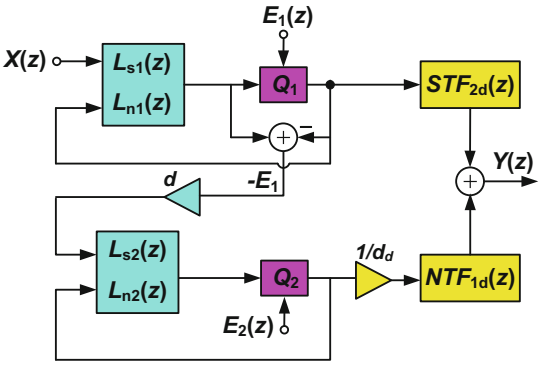

Fig. 1 Conventional MASH ΣΔ modulator

2 Proposed MASH ΣΔ Modulator

2.1 Conventional MASH Structure

The conventional two-stage MASH ΣΔ modulator is shown in Fig. 1 where $L_{si}(z)$ and $L_{ni}(z)$ denote the signal and noise loop filters of the ith stage, respectively [44]. Coefficients d and d_d indicate the inter-stage gain of the modulator and its digital estimation, respectively. Considering a linear model for quantizer, the overall output of the modulator is given by:

$$\begin{aligned} Y(z) = {} & \mathrm{STF}_1(z)\mathrm{STF}_{2d}(z)X(z) + \frac{1}{d_d}\mathrm{NTF}_{1d}(z)\mathrm{NTF}_2(z)E_2(z) \\ & + \left[\mathrm{NTF}_1(z)\mathrm{STF}_{2d}(z) - \frac{d}{d_d}\mathrm{STF}_2(z)\mathrm{NTF}_{1d}(z)\right]E_1(z) \end{aligned} \tag{1}$$

where $\mathrm{STF}_i(z)$, $\mathrm{NTF}_i(z)$ and $E_i(z)$ denote the signal and noise transfer functions and the quantization error of the ith stage, respectively. $\mathrm{NTF}_{id}(z)$ and $\mathrm{STF}_{id}(z)$ are the digital estimates of $\mathrm{NTF}_i(z)$ and $\mathrm{STF}_i(z)$, respectively.

It is worth mentioning that to have an accurate model for the quantization noise, it should be analyzed with a nonlinear approach [15,16,24]; however applying an additive noise (linear model) is a prevalent approximation to simplify the analysis [14,27,35,44,50,59].

By assuming a perfect matching between the analog transfer functions and their digital estimations and $d = d_d$, the output of the modulator will be as follows:

$$Y(z) = \mathrm{STF}_1(z)\mathrm{STF}_2(z)X(z) + \frac{1}{d}\mathrm{NTF}_1(z)\mathrm{NTF}_2(z)E_2(z) \tag{2}$$

It is clear that in a MASH ΣΔ modulator, the quantization noise of the preceding stage is used as the input to the succeeding stage. Ideally, the overall output of the modulator just includes the input signal and the shaped quantization error of the last single-stage modulator. The shaping order of this quantization noise is equal to the

order of the overall cascaded modulator. The quantization errors of all other stages are canceled by the subsequent digital signal processing logic. Nonetheless, MASH ΣΔ modulators require very accurate analog circuits in order to prevent the leakage of the first-stage quantization noise into the modulator's overall output.

2.2 Proposed MASH ΣΔ Modulator

The block diagram of the previously proposed MASH ΣΔ modulator [19] is shown in Fig. 2. In this structure, the first-stage quantization noise is fed to the second stage like the conventional MASH modulator. In the first stage, a typical single-stage ΣΔ modulator is used. A unity signal transfer function (STF) structure [46] is utilized to implement the second-stage modulator. In this modulator, the first delaying integrator is separated from the rest of the loop filter. Two inter-stage feedback paths return a ratio of the second-stage quantization noise to the first-stage quantizer input. Thus, the second-stage output is as follows:

$$Y_2(z) = -\mathrm{STF}_2(z) \times d \times E_1(z) + \mathrm{NTF}_2(z)E_2(z) \tag{3}$$

where $\mathrm{NTF}_2(z)$ is given by:

$$\mathrm{NTF}_2(z) = \frac{1}{1 + H_2(z) \times z^{-1}/(1 - z^{-1})} \tag{4}$$

By substituting $\mathrm{STF}_2(z) = 1$ in (3), the output of the first integrator in the second-stage modulator is obtained as:

$$V(z) = \frac{z^{-1}}{1 - z^{-1}}\left[-d \times E_1(z) - Y_2(z)\right] = -\frac{z^{-1}}{1 - z^{-1}}\mathrm{NTF}_2(z)E_2(z) \tag{5}$$

As shown in Fig. 2, a ratio of $V(z)$ and its one full cycle delayed version is injected to the first-stage quantizer input. So, these signals are shaped by the first-stage modulator NTF. The first-stage modulator output is given by:

$$Y_1(z) = \mathrm{STF}_1(z)X(z) + \left[E_1(z) + \frac{1}{d}(h - z^{-1})V(z)\right]\mathrm{NTF}_1(z) \tag{6}$$

So, by substitution of (5) for $V(z)$ in (6) and considering $\mathrm{STF}_{2d}(z) = \mathrm{STF}_2(z) = 1$, the overall output of the proposed modulator is obtained as follows:

$$\begin{aligned} Y(z) &= \mathrm{STF}_{2d}(z)Y_1(z) + \frac{1}{d_d}\mathrm{NTF}_{1d}(z)Y_2(z) \\ &= \mathrm{STF}_1(z)X(z) + \left[\mathrm{NTF}_1(z) - \frac{d}{d_d}\mathrm{NTF}_{1d}(z)\right]E_1(z) \\ &\quad + \left[\frac{1}{d_d}\mathrm{NTF}_{1d}(z)\mathrm{NTF}_2(z) - \frac{1}{d}\mathrm{NTF}_1(z)\mathrm{NTF}_2(z)\frac{hz^{-1} - z^{-2}}{1 - z^{-1}}\right]E_2(z) \end{aligned} \tag{7}$$

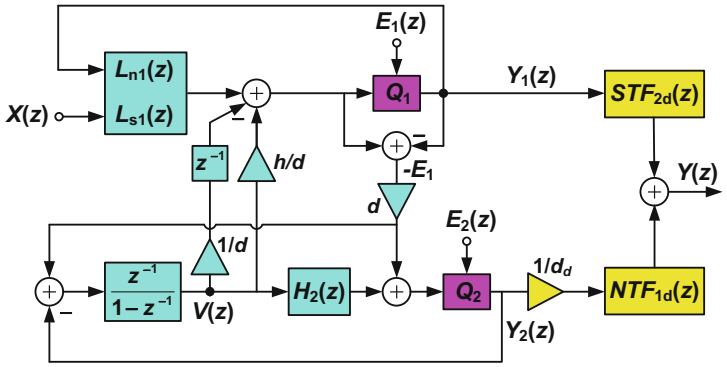

Fig. 2 Block diagram of the proposed MASH ΣΔ modulator

Therefore, ideally with well-matched analog transfer functions and their digital estimations and $d = d_d$, the overall output of the modulator is given by:

$$Y(z) = \mathrm{STF}_1(z)X(z) + \frac{1}{d}\frac{\mathrm{NTF}_1(z)\mathrm{NTF}_2(z)\left[1-(1+h)z^{-1}+z^{-2}\right]}{1-z^{-1}}E_2(z) \quad (8)$$

As is seen, the first-stage quantization error is removed like the conventional MASH modulator. By using $h = 1$, the second-stage quantization error is shaped by one order higher than the modulator's order. Moreover as is clear from (8), the place of the optimized NTF zeros is a function of h. So, by choosing a proper value for h, depending on the OSR, one pair of NTF zeros is optimized without affecting the digital cancelation filters. In fact, with an optimal $h(h_{\mathrm{opt}})$, one of the overall NTF zeros on DC is canceled, and instead two zeros are added inside the desirable bandwidth. Therefore, by using the proposed simple strategy, the in-band quantization noise of the modulator is significantly reduced.

One more advantage of the proposed topology over the conventional MASH modulator is that since the second-stage quantization error is not correlated with any other signal in the first-stage modulator, it behaves as a dither signal there.

The proposed modulator requires only two simple extra analog inter-stage paths as well as an adder to sum the signals entering the first-stage quantizer. By using the unity STF structure in both stages of the modulator, this adder can be merged by the same adder required before the first-stage quantizer. Furthermore, the effect of the analog circuit non-idealities is decreased [46].

To implement the circuit of the proposed modulator, the adder before the first-stage quantizer can be realized with either an active or passive circuit. However, lower speed and higher power consumption of the active adder make the passive structure a much better choice, especially when the timing is a challenging factor in the proposed ADC (detailed explanations are provided in Sect. 3.1). On the other hand, passive implementation of this adder causes a large signal attenuation as two extra inter-stage paths are ended to it (this will be shown in Sect. 4.1.1). Therefore, we propose a novel

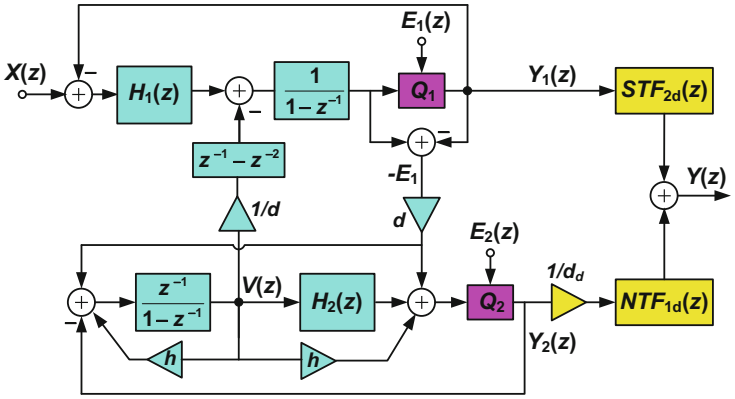

Fig. 3 Block diagram of the proposed improved MASH ΣΔ modulator

topology which provides the same performance as the previous structure but with a simpler circuit-level implementation.

2.3 Improvement of the Proposed MASH ΣΔ Modulator

An improved version of the previously proposed structure shown in Fig. 2 is depicted in Fig. 3. In this modulator, the last non-delaying integrator of the first stage is separated from the rest of the loop filter ($H_1(z)$). In the second stage, a unity STF ΣΔ modulator is used where the first delaying integrator is taken apart from the other of the loop filter ($H_2(z)$) like the second stage of the previously proposed structure. The modulator of Fig. 3 is obtained by eliminating the inter-stage feedback path with coefficient h/d from the modulator of Fig. 2 and instead adding two analog paths in the second-stage modulator. In addition, the inter-stage feedback path with one sample delay is transferred to the input of the last integrator in the first-stage modulator. The circuit implementation of this new improved structure is simpler than the previous one since the two inter-stage feedback paths in the previously proposed modulator of Fig. 2 are ended to the input of the first-stage quantizer, whereas in the proposed structure shown in Fig. 3, none of the employed extra paths enters this quantizer. Therefore, the adder before the first-stage quantizer can be simply realized with a passive circuit. Superiority of using the passive adder over the active one in this case is explained in Sects. 3.1 and 4.1.1.

In modulator of Fig. 3, the output of the second stage is given by:

$$Y_2(z) = -\mathrm{STF}_2(z) \times d \times E_1(z) + \mathrm{NTF}_2(z)E_2(z) \tag{9}$$

Because of using a unity STF structure in the second-stage modulator, $\mathrm{STF}_2(z) = 1$, the first integrator output in the second stage is determined by:

$$V(z)=\frac{z^{-1}}{1-(1+h)z^{-1}}\left[-d\times E_1(z)-Y_2(z)\right]=-\frac{z^{-1}}{1-(1+h)z^{-1}}\mathrm{NTF}_2(z)E_2(z) \tag{10}$$

This signal is delayed by function of $z^{-1}-z^{-2}$, and then, it is injected to the first-stage modulator. Consequently, the output of this stage becomes:

$$Y_1(z)=\mathrm{STF}_1(z)X(z)+\mathrm{NTF}_1(z)\left[E_1(z)+\frac{1}{d}\times\frac{z^{-2}}{1-(1+h)z^{-1}}\mathrm{NTF}_2(z)E_2(z)\right] \tag{11}$$

By assuming $\mathrm{STF}_{2d}(z)=\mathrm{STF}_2(z)=1$, $\mathrm{NTF}_{1d}(z)=\mathrm{NTF}_1(z)$ and $d=d_d$, the ideal overall output of the modulator is given by:

$$Y(z)=\mathrm{STF}_1(z)X(z)+\frac{1}{d}\times\frac{\mathrm{NTF}_1(z)\mathrm{NTF}_2(z)\left[1-(1+h)z^{-1}+z^{-2}\right]}{1-(1+h)z^{-1}}E_2(z) \tag{12}$$

where $\mathrm{NTF}_2(z)$ is as follows:

$$\mathrm{NTF}_2(z)=\frac{1-(1+h)z^{-1}}{1-z^{-1}+z^{-1}H_2(z)} \tag{13}$$

As is seen from (12), the noise-shaping ability of the overall modulator increases by one order, and simultaneously by choosing an optimal value for h, the optimization of one pair of NTF zeros is achieved. In fact, in the overall NTF of the modulator, the pole on $1/(1+h)$ is canceled by a zero on the same place emerged in $\mathrm{NTF}_2(z)$ (see (13)), and instead two optimized complex-conjugate zeros are added inside the desired bandwidth. So, the modulators shown in Figs. 2 and 3 have the same performance, while the modulator of Fig. 3 is easier to implement.

To find the optimal value of h, we can consider a typical Lth order NTF with two optimized zeros. For $L\geq 2$, such a NTF is as follows [14]:

$$\mathrm{NTF}(z)=(1-z^{-1})^{L-2}(1-\delta z^{-1}+z^{-2}) \tag{14}$$

where $\delta=2\cos(2\pi f_0/f_s)$. f_s is the sampling frequency, f_0 denotes the optimal place of the in-band NTF zeros, and it is approximately determined by $f_0=\sqrt{(2L-3)/(2L-1)}f_{BW}$where f_{BW} indicates the signal bandwidth. Therefore, the optimal value of h in the proposed structure is obtained as follows:

$$h=2\cos\left(\frac{2\pi f_0}{f_s}\right)-1 \tag{15}$$

As an example, a MASH 2-1 $\Sigma\Delta$ modulator based on the improved proposed structure is shown in Fig. 4. The ideal output of this modulator is given by:

$$Y(z)=X(z)+\frac{1}{d}\left(1-z^{-1}\right)^2\left[1-(1+h)z^{-1}+z^{-2}\right]E_2(z) \tag{16}$$

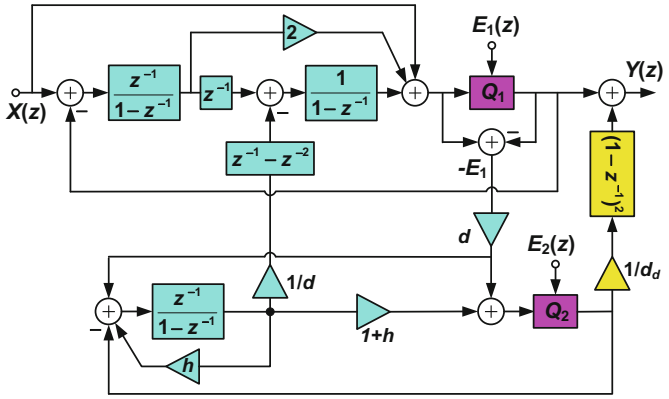

Fig. 4 The proposed MASH 2-1 ΣΔ modulator

So, by using three analog integrators, a fourth-order noise shaping with one pair of optimized NTF zeros is achieved. It is worth mentioning that MASH 2-1 modulator in Fig. 4 achieves a similar result to the one shown in Fig. 3 in [19]; however, it has a simpler practical design. To make this simplicity more clear, one should notice that the first-stage adder in both of these modulators can be implemented by a passive circuit. However, because the number of input branches entering into the first-stage adder is decreased in the improved version MASH 2-1 modulator shown in Fig. 4, the signal attenuation in this passive adder is smaller than that for modulator shown in Fig. 3 in [19]. Consequently, in this modulator, the latch voltage references are less attenuated, and hence, the latch design is simpler and its power consumption will be lower than that for modulator shown in Fig. 3 in [19]. In addition, in the first-stage adder of MASH 2-1 in [19], the coefficient $h/d = 0.22$ is much smaller than the other adder input coefficients (which are 1 and 2), and so, its implementation by capacitance ratios needs more unit capacitors compared to the improved version that requires the implementation of a path with coefficient $h = 0.89$ entering into the third integrator. The implementation of this path is explained with more details in Sect. 4.1.

It is worth mentioning that both proposed structures for two-stage cascaded modulators shown in Figs. 2 and 3 are capable to be extended to higher-order MASH structures. In this case, only the last two-stage modulators can be coupled together by a structure like the presented ones. As a result, the noise-shaping ability of the whole modulator is increased by one order, and simultaneously, the zero optimization for one pair of NTF zeros is achieved.

3 System-Level Design and Simulation Results

System-level design of the proposed modulator involves two main practical challenges. Firstly, employing a proper timing diagram which provides the optimum operating time for the circuit of the modulator especially for those blocks that cause a bottleneck in the timing issue. Secondly, the extraction of the first-stage quantization noise that should

be done by subtracting the input and output of the first-stage quantizer without causing any uncertainty to the modulator. These issues and the proposed practical solutions as well as the system-level simulation results are presented in this section.

3.1 Practical Timing Issue

In the conventional MASH ΣΔ modulator shown in Fig. 1, the first-stage quantization noise is extracted as the subtraction of two paths: the input and output of the first-stage quantizer. Using a unity STF structure to implement the modulator of both stages makes a critical path in this structure. This condition is established for the sturdy MASH (SMASH) presented in [45] and also the proposed ΣΔ modulators. Figure 5 shows the critical path along with front-end loop path in the proposed MASH 2-1 modulator. The name critical is selected because it is delay free. It means that, the adder and quantizer of the first-stage, the inter-stage DAC (DAC_2) and the second-stage adder, all should operate in half a clock period. The third adder in the critical path employed for extracting E_1 is not a concern here since it will be merged with the second-stage adder and the third integrator as will be discussed later in Sect. 3.2. Timing diagram of the proposed modulator can be chosen like the one presented in [34], as shown in Fig. 6. As is seen, the timing diagram of two mentioned paths is considered in this figure. In both cases, the first-stage adder should have a fast operation time (small t_{add1}). After this analog addition, the first-stage quantization is performed during time t_c. Then, in the inter-stage critical path, the inter-stage DAC and the second-stage adder must operate during t_{dac2} and t_{add2}, respectively. At this time, in the front-end loop path, the dynamic element matching (DEM) process followed by the front-end DAC operation should be done in t_{DEM} and t_{dac1}, correspondingly. The values of t_c, t_{dac1} and t_{dac2} are anticipated to be small because the quantization

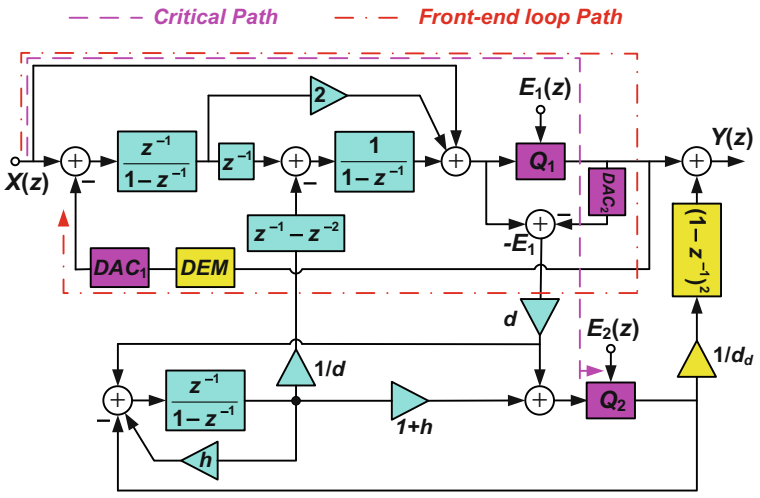

Fig. 5 The critical path in proposed MASH 2-1 ΣΔ modulator

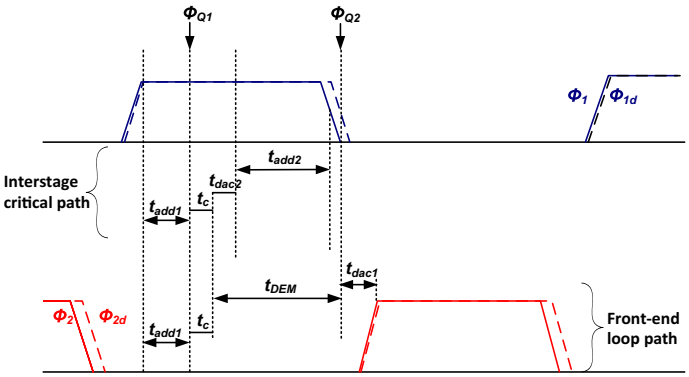

Fig. 6 Timing diagram of the proposed modulator

can be done with comparators based on very fast regenerative latches. Also, DACs can operate very fast. So, the impasse for timing issue is caused by the time needed by the adders. Hence, the first-stage adder is considered to be implemented by a passive circuit which operates faster than the active one.

With this timing diagram, there is more time for DEM process compared with the case that the first-stage quantization noise can be extracted from a single analog node and there is no critical path. In this case, the quantizer, DEM algorithm and DAC_1, all should operate in the non-overlapping clock between the sampling and integrating phases [47].

3.2 First-Stage Quantization Noise Extraction

The passive adder structure is sensitive to parasitic effects. It means that its output signal is attenuated by an unknown factor depends on the parasitic capacitances (this is explained with more details in Sect. 4.1.1). For extracting $E_1(z)$, based on the direct subtraction of the first-stage quantizer input and output, as shown in Fig. 4, the first-stage passive adder output should be directly sampled. But as mentioned, in practice, this signal is attenuated by a vague coefficient. So, it cannot be accurately compensated. Consequently, $E_1(z)$ can't be exactly extracted by this method. Therefore, extraction of $E_1(z)$ is done at the input of the second loop using the modulator input signal, outputs of the first and second integrators and the output of the first-stage quantizer. Figure 7 shows a conceptual block diagram like the one presented in [26]. In fact, the third integrator adds the three inputs of the first-stage passive adder and subtracts the quantizer output from them besides its main duty. This process for extracting the first-stage quantization error is repeated at the input of the second-stage active adder to realize the unity STF structure.

3.3 Comparison and Behavioral Simulation Results

A resonation-based MASH 2-2 $\Sigma\Delta$ modulator with a global resonation has been presented in [35] to optimize one pair of NTF zeros. Figure 8 shows the block diagram

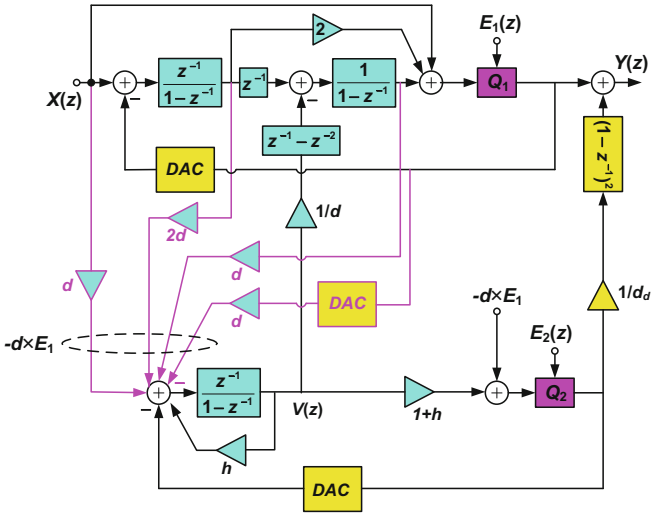

Fig. 7 First-stage quantization noise extraction

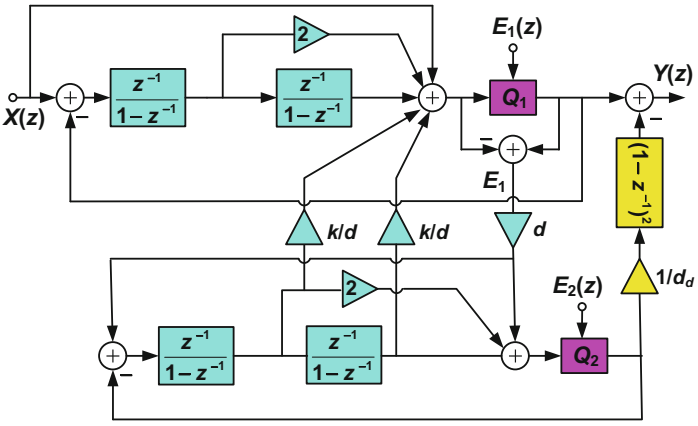

Fig. 8 Resonation-based MASH 2-2 [35]

of this modulator. The proposed MASH 2-1 modulator shown in Fig. 7 has a noise-shaping ability similar to this modulator while has one less integrator. Moreover, the proposed MASH 2-1 modulator has a further preference into the resonation-based MASH 2-2 modulator presented in [35]. To verify this superiority, consider the relations (16), mentioned above, and (17) which remarks the overall output of the MASH 2-2 modulator presented in [35]:

$$Y_{[13]}(z) = X(z) + \frac{1}{d}(1 - z^{-1})^2 \left[1 - (2 - k)z^{-1} + z^{-2}\right] E_2(z) \tag{17}$$

As is obvious, for particular places of optimum in-band NTF zeros, the optimal amount of $h(h_{\text{opt}})$ is much larger than that of $k(k_{\text{opt}})$. The proposed MASH 2-1 in Fig. 7

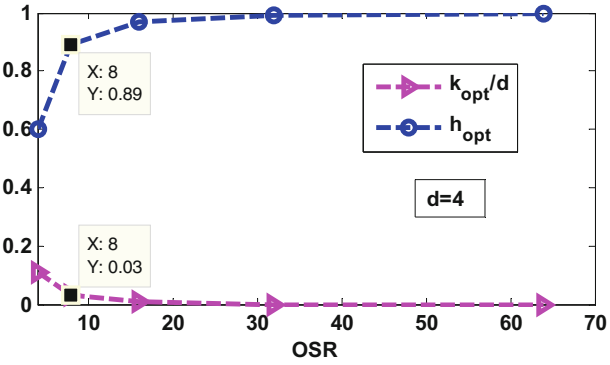

Fig. 9 Values of h_{opt} and k_{opt}/d versus OSR

employs extra paths with constant coefficients $1/d$ and h_{opt} instead of k_{opt}/d in the resonation-based MASH 2-2. Therefore, for implementing these coefficients in circuit level, it is required to implement the capacitance ratios of $1/d$ and h_{opt} in the proposed structure, while the coefficient k_{opt}/d should be implemented for the resonation-based modulator. Since $d > 1$ and $k_{opt} < h_{opt} \leq 1$, the switched-capacitor implementation of extra paths in the proposed modulator is so simpler than the ones in [35]. Figure 9 shows the k_{opt}/d and h_{opt} coefficients for different values of OSR. As is seen, higher OSRs lead to smaller amounts of k_{opt} and larger values of h_{opt}. Consequently, this advantage of the proposed modulator becomes more significant when high OSRs are used.

The proposed MASH 2-1 $\Sigma\Delta$ modulator shown in Fig. 7, the conventional unity STF MASH 2-1 and the resonation-based MASH 2-2 modulator presented in [35] are simulated using MATLAB and Simulink. Circuit non-idealities comprising the limited output swing and finite DC gain of the amplifiers were considered in Simulink based on the models presented in [29]. The number of quantization bits, the supposed OSR and the inter-stage gain (d) were 4, 8 and 4, respectively. Figure 10 shows the simulated output power spectrum where a -0.7 dBFS sinusoidal input signal was employed. The sharper slope of the proposed modulator spectrum shows one-order higher noise-shaping ability compared with the conventional modulator. Also, emerging the notch near the signal bandwidth of this modulator indicates its zero optimization capability. By adjusting $h_{\text{opt}} = 0.89$, 98.8 dB SNDR is obtained for the proposed MASH 2-1 structure, while 79 dB and 98.2 dB SNDR are achieved for the conventional MASH 2-1 and resonation-based MASH 2-2 modulators, respectively. Thus, the SNDR is improved by 19.8 dB compared to the conventional MASH 2-1 modulator.

The simulated SNDR versus the input signal amplitude is illustrated in Fig. 11. As is seen, the overload level factor of the proposed MASH 2-1 is a little, around a few tenths of dB, lower than the conventional MASH 2-1. This happens since the first-stage quantizer of the proposed MASH 2-1 should also process a feedback signal returned from the second-stage modulator. Hence, it is overloaded with a lower input signal amplitude compared with the conventional MASH structure. But, this reduction is not significant because the returned feedback signal is the delayed version of the second-stage quan-

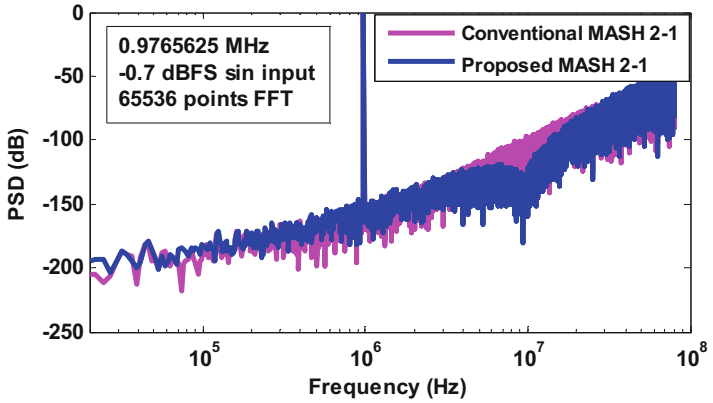

Fig. 10 System-level output spectrum of the proposed and conventional MASH 2-1 modulators

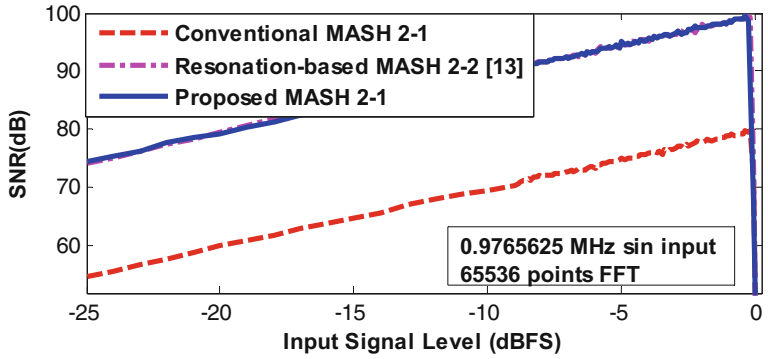

Fig. 11 SNDR versus the input signal amplitude

tization noise which is first order shaped, and hence, it is a small signal. According to the relations (10) and (13), $V(z) = -z^{-1}E_2(z)$ in the proposed MASH 2-1 modulator, and so, the returned feedback signal is $-(z^{-1} - z^{-2})V(z) = z^{-2}(1 - z^{-1})E_2(z)$. Therefore, the proposed strategy doesn't deteriorate the stability of the conventional modulator. The resonation-based MASH 2-2 modulator has approximately the same overload level factor as the proposed structure.

Figure 12 shows the SNDR variations against the amplifier DC gain in the proposed MASH modulator. For the first and second integrator amplifiers, a minimum DC gain of 65 dB is required to prevent the modulator performance degradation significantly. DC gain of 35 dB is sufficient for the third integrator amplifier because the error of this stage is shaped by the preceding stages. Note that to find the minimum required DC gain of each integrator amplifier, the following amplifiers are considered ideal and the previous ones are set to their minimum required DC gains achieved by simulations.

Figure 13 depicts the differential output swing of all integrators. Thanks to using the unity STF structure, the maximum required swing is less than 0.2 of the reference voltages which can be simply realized.

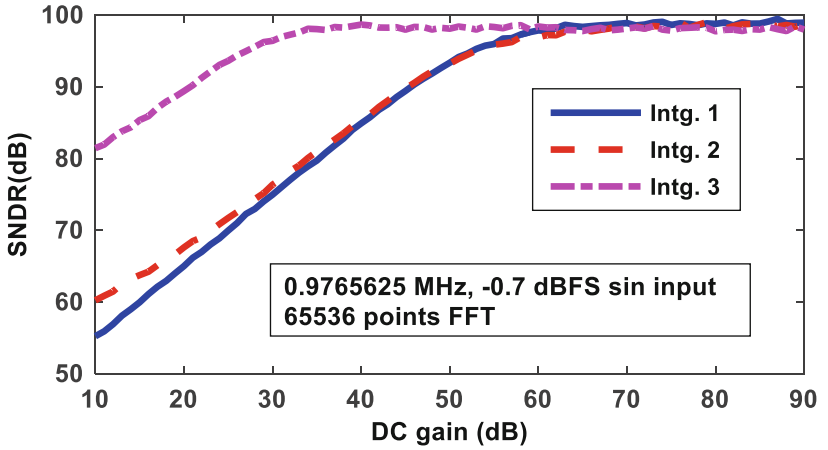

Fig. 12 SNDR versus amplifier DC gain of integrators

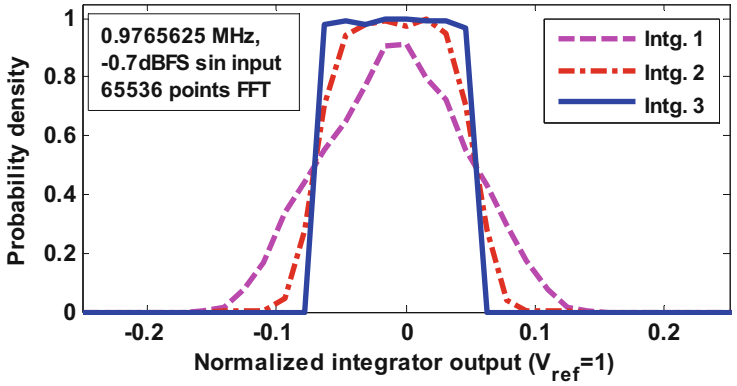

Fig. 13 Output swing of integrators

Monte Carlo simulations, with 1000 iterations and assuming 0.2 % mismatch among different capacitor ratios, have been done to validate the correct electrical performance of the modulator when there is mismatch between modulator coefficients. As shown in Fig. 14, the SNDR change due to this incompatibility is negligible which indicates the insensitivity of the proposed modulator to the coefficients mismatch.

3.4 Linearization of Multi-bit DAC

As mentioned before, using multi-bit quantizers in $\Sigma\Delta$ modulators increases the modulator accuracy. In this case, a multi-bit DAC with the same resolution of the quantizer but with the overall modulator accuracy is needed. However, the mismatch among the DAC unit elements limits the modulator linearity. Therefore, a linearization technique such as the data weighted averaging (DWA) algorithm [2] should be used to reduce the DAC nonlinearity error. In the proposed MASH 2-1 structure, only the effect of the

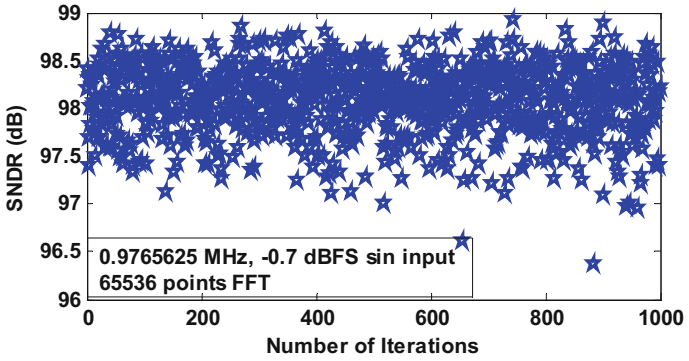

Fig. 14 Monte Carlo simulation results of SNDR for 1000 iterations by considering 0.2 % coefficient mismatch

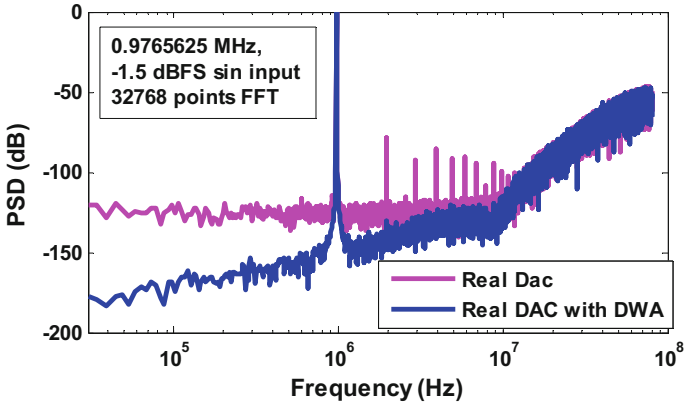

Fig. 15 Simulated output spectrum of the modulator by considering 0.2 % mismatch among the DAC unit elements with and without employing the DWA technique

first-stage DAC nonlinearity is important because it appears in the modulator input-referred noise without any noise shaping, while the errors of the second-stage and inter-stage DACs are decreased by second-order noise shaping when they are referred to the modulator input. So, the DWA algorithm is employed for the first-stage DAC. Figure 15 shows the system-level simulated output spectrum of the modulator presuming 0.2 % mismatch among the DAC unit elements with and without employing the DWA technique. As is seen, using DWA algorithm decreases the signal tones due to the DAC nonlinearities significantly. This way, 74.6 dB SNDR of the modulator with real DAC is increased to 94.6 dB when the DWA technique is employed which is just about 1.4 dB lower than the case when an ideal DAC is used. It is worth mentioning that DAC capacitors mismatch of less than 0.2 % can be easily provided in 90-nm CMOS technology considering the unit capacitance of 0.22 pF which is calculated in Sect. 4.1.4.

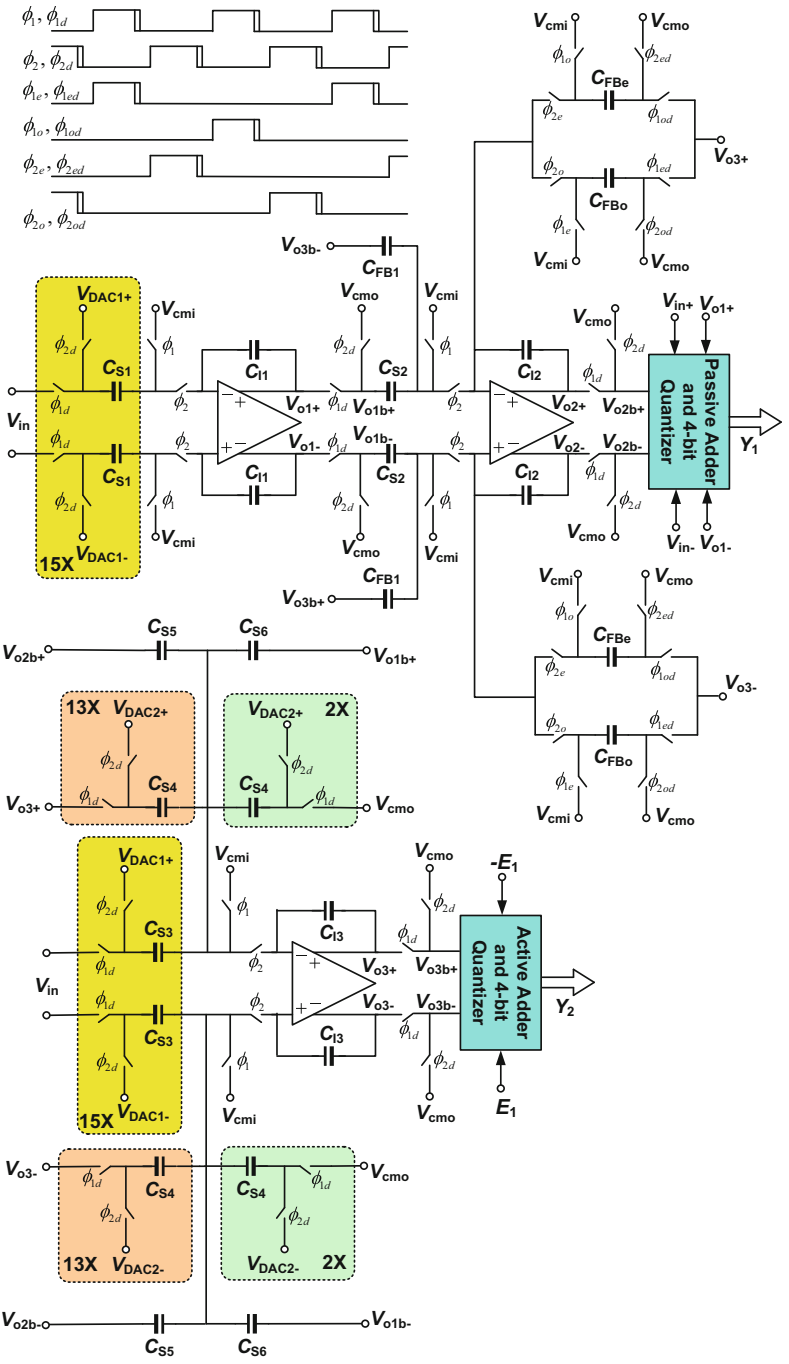

Fig. 16 Switched-capacitor circuit implementation of the proposed MASH 2-1 modulator

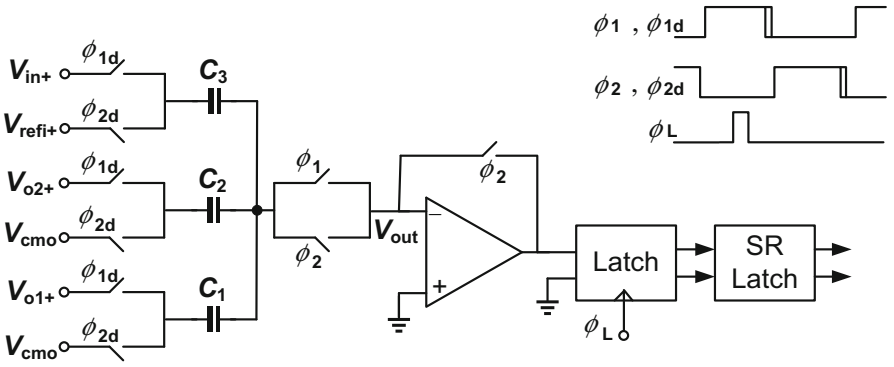

Fig. 17 Switched-capacitor circuit implementation of the passive adder used in the first-stage modulator (shown as single ended for simplicity)

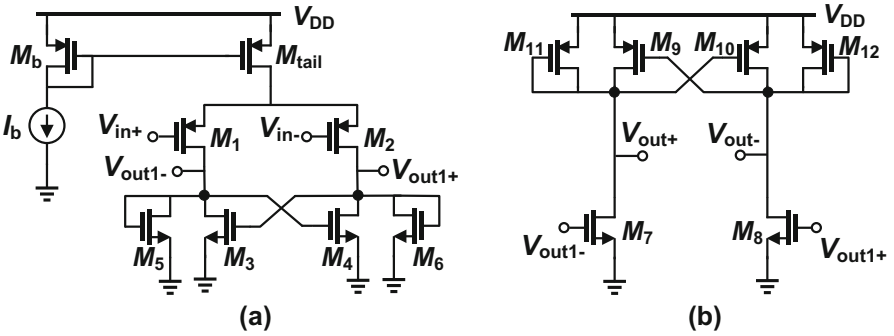

Fig. 18 Preamplifier circuit: **a** first-stage and **b** second-stage amplifiers

4 Circuit-Level Design

The circuit-level design of the proposed MASH 2-1 ΣΔ modulator is examined in details to explore its implementation issues and evaluate its effectiveness. The design is targeted to achieve 14-bit resolution with 10 MHz input signal bandwidth in a 90-nm CMOS process. The power supply voltage is 1 V.

4.1 Switched-Capacitor Circuit Implementation

The proposed MASH 2-1 ΣΔ modulator shown in Fig. 7 is implemented by the switched-capacitor (SC) circuit depicted in Fig. 16. As is seen, the first integrator is a conventional one. To realize the first-stage 4-bit DAC, 15 unit capacitors are shared with the input sampling capacitors. So, the first integrator feedback factor does not decrease which results in saving the amplifier power consumption. The second integrator, $1/(1\text{-}z^{-1})$, has three inputs starting from the first and third integrator outputs (see Fig. 7). Two of them, beginning from the first and third integrator outputs, have one delay unit, z^{-1}, which is combined with $1/(1\text{-}z^{-1})$ simply to form a delaying

integrator. To implement the inter-stage feedback path with two sample delays (z^{-2}), two similar sets of capacitors, C_{FBe} and C_{FBo}, are used. Each of these capacitors samples the third integrator output at even/odd sample phases, holds it for one and half of a clock period and then transmits it to the second integrator output. Because the integrator output is held constant until the end of the next sampling phase, i.e., half of a clock period later, two full cycle delays from the third integrator output to the second integrator output are realized. To implement the path with coefficient h from the third integrator output to its input, 13 capacitors of 15 second-stage DAC unit capacitors are reused. So, h_{opt} is approximated by 13/15 = 0.86 instead of 0.89 obtained by (15) and also behavioral simulations. System-level simulations show that this approximation does not degrade the modulator SNDR significantly.

4.1.1 First-Stage Adder and Quantizer

As indicated before, the first-stage adder should be realized with a passive circuit due to the modulator timing issue. This kind of adder has lower power consumption compared with its active counterpart. The switched-capacitor realization of this adder and first-stage quantizer including the preamplifier, regenerative latch and SR latch are shown in Fig. 17. In the sampling/adding phase (Φ_1), the summation is done, and in the integrating/resetting phase (Φ_2), the preamplifier is reset to reduce the memory effects [42]. The first-stage passive adder output is as follows:

$$V_{out}(z) = \frac{1}{C_1 + C_2 + C_3 + C_P}\left[C_1 V_{o1} + C_2 V_{o2} + C_3(V_{in} - V_{refi})\right] \tag{18}$$

where C_P is the total parasitic capacitance at the passive adder output (V_{out} in Fig. 17). As is seen from (18), one disadvantage of the passive adder is the signal attenuation. To compensate this issue, the quantizer reference voltages are fed to this adder in resetting phase to be attenuated like the main signal does. The offset of the regenerative latch is attenuated by the preamplifier gain when it is referred to the quantizer input. Also, the input offset storage technique [40] is used to attenuate the preamplifier offset. In this technique, the preamplifier offset is stored in adder capacitors during the resetting phase, and then in the adding phase, this stored offset is canceled with the offset voltage of the preamplifier.

The preamplifier is implemented by a two-stage amplifier shown in Fig. 18 to achieve wide bandwidth besides sufficient DC gain to provide an acceptable attenuation for the latch input-referred offset. The diode-connected and cross-coupled transistor loads of this amplifier eliminate the need for an explicit common-mode feedback circuit. The regenerative latch used in the first-stage modulator is implemented by the circuit presented in [57]. Thanks to using an SR latch, the output value of the regenerative latch is held during the resetting phase.

4.1.2 Second-Stage Adder and Quantizer

The second-stage adder should be implemented by an active circuit to realize the inter-stage gain of 4. The switched-capacitor circuit of this adder is plotted in Fig. 19. For

adding V_{o1} with a coefficient of 8, the capacitor ratio of 4 is chosen, and instead the symmetry of V_{o1} is used as the input of the adder in the other phase. So, the adder has a larger feedback factor compared with when a capacitor ratio of 8 is used. The differential output of this adder is compared with the differential references by using a dynamic comparator presented in [8]. The output value is also held by using an SR latch during the resetting phase.

4.1.3 Switches

Three different kinds of switches are used in the implemented modulator. For input sampling switches and switches that are along the signal path, the switch resistance should be constant enough to provide the required linearity. Bootstrapped switches are utilized to implement them [11]. Simple NMOS switches are used when the signal is nearly constant. The remaining switches are realized with CMOS switches where their resistance linearity is more than the NMOS switches but less than the bootstrapped ones.

4.1.4 Sampling Capacitors

More than the quantization noise, the circuit thermal noise restricts the modulator performance. In this way, a power efficient design can be achieved [47]. The values of the first and second integrator sampling capacitors depend on the acceptable thermal noise to achieve the required accuracy. Thermal noise of the second integrator following stages has a negligible quota in the modulator input-referred noise since their circuit noise is shaped with a minimum order of 2. Hence, we just consider the first and second integrator effects in the modulator input-referred circuit noise. Knowing the maximum achievable SQNR of 98 dB for a input signal power of -3.7 dB (-0.7 dBFS for $V_{Ref} = 1$ V) which is obtained by system-level simulations, the maximum allowable quantization noise power is computed about -101.7 dB. Therefore, to achieve an accuracy of 14 bit, corresponds to an SNDR of 86 dB, the maximum allowable thermal noise should be below -90 dB. By assigning 90 and 10 % of the total input-referred thermal noise to the first and second integrator noise quotas, respectively, the minimum sampling capacitors of $C_{S1} \geq 3$ pF and $C_{S2} \geq 1.9$ pF are needed. The first and second integrator sampling capacitors are chosen 3.3 pF and 2 pF to keep a safety margin. The first sampling capacitor is realized by using 15 DAC unit capacitors of 220 fF.

4.2 Operational Transconductance Amplifiers

Some of the circuit design requirements for the integrator operational transconductance amplifiers (OTAs) were obtained by system-level simulations presented in Sect. 3.4. For the first and second integrator amplifiers, a minimum DC gain of 65 dB and maximum normalized differential output swing of 0.1 V is needed. This amount of swing can be simply achieved by usual types of OTAs. But, to provide the required high DC gain in 90-nm CMOS technology, a two-stage OTA with gain-boosting [6] can be used.

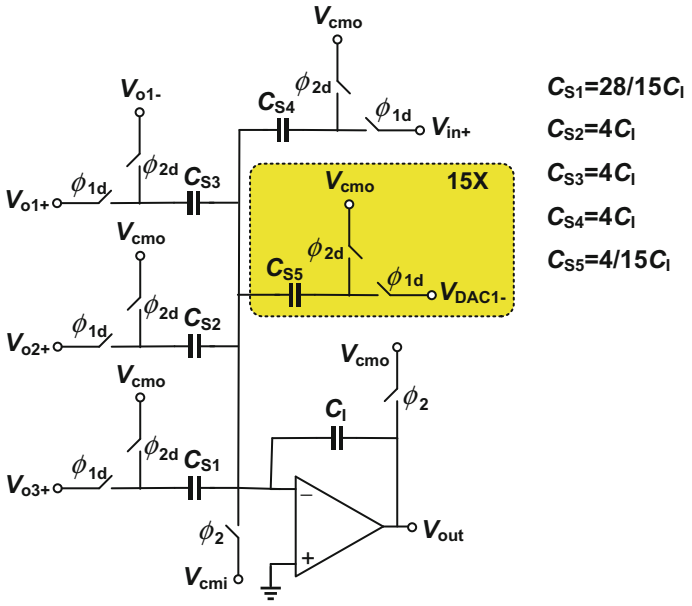

Fig. 19 Switched-capacitor circuit implementation of the active adder used in the second-stage modulator (shown as single ended for simplicity)

Figure 20 shows the implemented OTA structure for the first and second integrators, while transistor sizes and bias currents are different for these two amplifiers owing to their different capacitive load and required settling accuracy. In this structure, the main OTA is a two-stage one with the hybrid-cascode compensation [55,56]. By using this kind of compensation, an OTA with wide bandwidth is achieved. The first stage of the OTA shown in Fig. 20 is a folded-cascode amplifier, and two auxiliary fully differential amplifiers, A_1 and A_2, are used to increase the DC gain of the first stage. The gain enhancement is achieved by increasing the output resistance by a factor equal to the DC gain of the internal amplifiers [6]. The gain-boosting OTAs are shown in Fig. 21 where diode-connected and cross-coupled transistors are used as active loads to eliminate the need for explicit common-mode feedback circuits.

System-level simulation results show that nearly 40 dB DC gain is sufficient for the third integrator OTA. So, to implement this amplifier, the structure presented in [55,56] is used which is actually the main OTA shown in Fig. 20 without the gain boosting.

5 Circuit-Level Simulation Results

The proposed MASH 2-1 $\Sigma\Delta$ modulator has been simulated in a 90-nm CMOS technology using Spectre-RF. A -0.7 dBFS, 2.5 MHz sinusoidal input signal is applied. The output power spectrum is shown in Fig. 22. The achieved SNDR with 8192 points FFT and a Hanning window [44] is 91.1 dB which is decreased to 85.2 dB by including the thermal noise of the circuit. The simulated SNDR against the input signal amplitude is illustrated in Fig. 23 achieving 87 dB dynamic range. Table 1 summarizes the

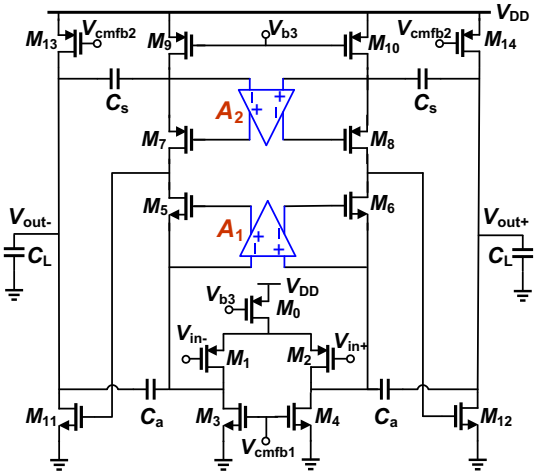

Fig. 20 Operational amplifier used in the first and second integrators

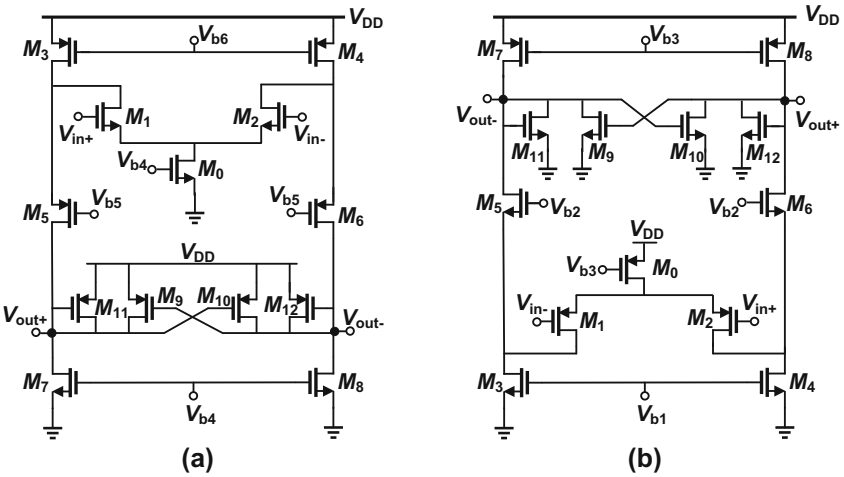

Fig. 21 Gain-boosting amplifiers: **a** nMOS input (A_2) and **b** pMOS input (A_1)

performance of the implemented modulator for three different process corner cases and temperature variations. To verify the overall performance of the proposed modulator and compare it with the other reported designs, the following figure of merit (FoM) is utilized [51]:

$$\text{FoM} = \frac{\text{Power}}{2 \times \text{BW} \times 2^{\text{ENOB}}} \tag{19}$$

where ENOB is the effective number of bits and BW is the input signal bandwidth. Lower power consumption, wider input signal bandwidth, and higher modulator resolution result in smaller value of FoM which shows the better overall performance of the modulator.

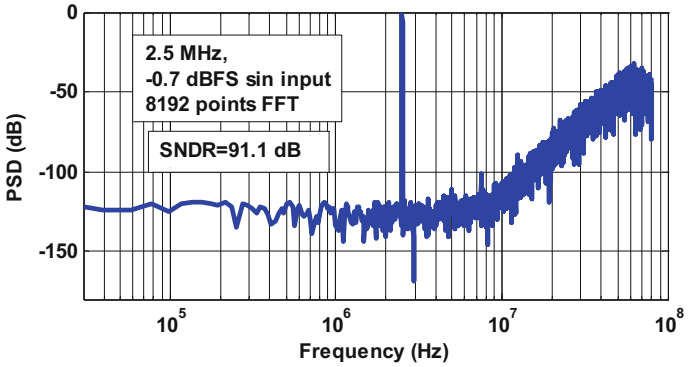

Fig. 22 Simulated output spectrum of the proposed MASH 2-1 ΣΔ modulator excluding the circuit noise (TT @ 27 °C)

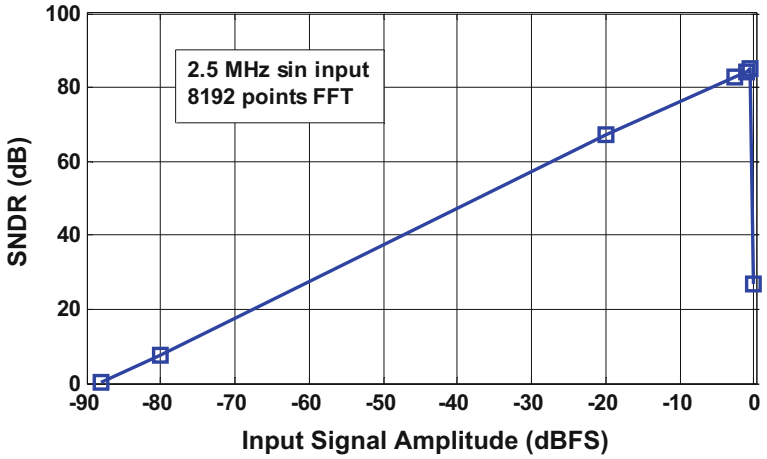

Fig. 23 Simulated SNDR versus the input signal amplitude by including the circuit noise (TT @ 27 °C)

Table 1 Performance summary of the simulated MASH 2-1 ΣΔ modulator

Parameter	TT @ 27 °C	FF@−40 °C	SS @ 85 °C
SNDR	85.2 dB	85.3 dB	80.8 dB
SFDR	101.1 dB	99.7 dB	91 dB
ENOB	13.9 bit	13.9 bit	13.1 bit
Power dissipation	31.6 mW	32.1 mW	29.8 mW
Sampling rate	160 MHz		
Oversampling ratio	8		
Signal bandwidth	10 MHz		
Supply voltage	1 V		
Technology	90-nm CMOS		

Table 2 Performance comparison of the proposed MASH 2-1 ΣΔ modulator with several state-of-the-art modulators

Parameter	Process (nm)	VDD (V)	Modulator architecture	f_s (MHz)	BW (MHz)	SNDR (dB)	Power (mW)	FoM (fJ/conversion)
JSSC'13 [36]	130	1.2	Second-order noise-shaped integrating two-step	160	10	67.4	12.6	330
TIM'13 [18]	65	1.2	Fourth-order 4-bit single-loop	180	6	72.3	18.5	460
JSSC'12 [52]	65	1.2	MASH 1-1-1-1	40	2.5	70.4	3.73	276
TCASI'12 [58]	130	1.2	MASH 2-2	130	5	75.7	16	320
IJCTA'12[a] [47]	90	1	MASH 3-2	160	10	79.4	35.4	230
AICSP'12[a] [26]	90	1	CT/DT double-sampled SMASH 2-2	100	12.5	73.8	17	170
JSSC'11 [28]	180	1.5	Third-order single-loop	50	1.05	78.2	2.9	210
JSSC'11 [38]	180	1.2	Delta-sigma noise-shaped two-step	25	1.56	75	6.35	443
JSSC'10 [4]	90	1.2	Multi-rate MASH 2-1	80	1.92	65.5	6.83	1155
MWSCAS'10[a] [17]	180	1.8	CT Third-order single-loop	320	10	79.31	35.5	235
JSSC'10 [32]	110	1.1	CT Fifth-order single-loop	300	10	62.5	5.32	240
JSSC'10 [25]	180	1.8	CT Fifth-order single loop using time-domain quantization	400	25	67.7	48	484
IEICE Trans'09[a] [53]	180	1.8	Second-order time-interleaved	142.8	1.1	80.5	19.5	1023
TCASI'09[a] [3]	90	1.2	Second-order path coupled	60	2	56	1.56	750
JSSC'09 [13]	90	1.2	Fourth-order single-loop	100	4	66.85	11.76	820
VLSI'09 [39]	180	1.8	Delta-sigma/pipeline	60	2	56	36	748
JSSC'09 [27]	180	1.2	SMASH 2-2	20	0.625	74.6	3.2	583
MWSCAS'09 [1]	90	1.2	MASH 2-2	500	31.25	70	140	866
ICECS'09[a] [10]	180	1.8	Split cross-coupled	160	5	80	11	130

Table 2 continued

Parameter	Process (nm)	VDD (V)	Modulator architecture	f_s (MHz)	BW (MHz)	SNDR (dB)	Power (mW)	FoM (fJ/conversion)
TCASII'08[a] [9]	65	1	MASH 3-1	128	1	93	11.6	153
ISSCC'08 [21]	180	1.5	Noise-coupled time-interleaved	100	4.2	79	28	458
ISSCC'08 [30]	90	1.2	MASH 2-2	420	20	70	27.9	270
AICSP'08[a] [7]	90	1	CT Fifth-order single-loop	800	25	70	16.4	70
TCASI'07[a] [43]	180	1.8	CT Third-order single-loop	640	10	66	7.5	230
This work[a]	90	1	MASH 2-1	160	10	85.2	31.6	103

[a] Simulation results

It is worth mentioning that since the DWA block is not implemented in circuit level, its power consumption is not considered in reported results. However, as stated in [31], for a 4-bit quantizer implemented in a 90-nm CMOS technology, the DWA block consumes a power of less than 2 mW.

Table 2 shows the comparison of the proposed modulator with several state-of-the-art modulators. As is seen, the proposed modulator has a good performance among the other discrete-time structures and even is comparable with continuous-time modulators. It should be mentioned that the results of the proposed modulator are based on the circuit-level simulations, while most of the other reported modulators are reporting the measured results and this is not a fair comparison. Nonetheless, the achieved outstanding FoM of the simulated MASH 2-1 modulator verifies the efficiency of the proposed MASH $\Sigma\Delta$ modulators, and hence, it is also expected a better FoM to be achieved from the measurement results.

6 Conclusions

In this paper, a novel structure of MASH $\Sigma\Delta$ modulators is presented to reduce the in-band quantization noise significantly. This reduction is achieved by enhancing the modulator noise-shaping ability by one order and also optimizing one pair of NTF zeros. All these advantages are achieved only by using two extra analog feedback paths without increasing the number of active blocks. An improved version of this modulator is presented to simplify the modulator realization. In this structure, by removing the inter-stage feedback paths from the first-stage quantizer input, the first-stage adder can be easily realized with a passive circuit to save the power consumption significantly. As an example, a MASH 2-1 modulator with the improved proposed structure has been examined in some different aspects including the timing issue and extraction of the first-stage quantization noise. This modulator is simulated in system and circuit levels using MATLAB/Simulink and Spectre-RF in a 90-nm CMOS technology, respectively. The simulation results show that the implemented MASH 2-1 modulator achieves 87 dB dynamic range and 85.2 dB maximum SNDR over 10 MHz signal bandwidth while consuming 31.6 mW power from a single 1 V supply.

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