A First-Order Derivative-Based QRS-Detection Circuit in Time Domain for ECG Sensors

Atiyeh Karimlou and Mohammad Yavari, *Senior Member, IEEE*

***Abstract*—A novel low-power first-order derivative-based QRS-detection circuit is presented in this brief. The low-power performance is achieved by employing a time-based differentiator circuit instead of the voltage differentiator and also using two D-Flip-Flop (D-FF) blocks for threshold comparing instead of voltage comparators in conventional derivative-based circuits. The proposed circuit is designed and simulated in 180 nm TSMC CMOS process occupying 0.026 mm^2 silicon die area. The simulation results yield a detection error rate of 1.49%, with sensitivity and positive prediction rates of 99.26% and 99.25%, respectively. The power consumption is about 39.8 nW from a 0.8 V supply voltage.**

***Index Terms*—Cardiovascular disease, wearable and wireless electrocardiogram (ECG) sensors, QRS-detection, R-peak.**

I. Introduction

ONE OF the most common detectable waveforms from the sensing electrodes placed on the skin is the electrocardiogram (ECG), which represents the periodic pattern of heart activity [1]. Fig. 1 shows a sample of the acquired ECG signal from the sensing electrodes. The QRS complex is the most important signal feature, which the heart abnormalities can be determined by recognizing QRS complexes and computing the time interval between successive R peaks.

Several approaches for identifying QRS complexes from ECG signals have been developed with the existing compromises often between simplicity, efficiency, and power dissipation. Complicated approaches, like those of wavelet transforms and neural networks, are accurate, but they use a lot of power and demand a lot of memory [2], [3]. As a result, they are often unsuitable for wearable and implantable ECG sensors. With Pan and Tompkins algorithm, the QRS-detector has high detection accuracy [4]. Nonetheless, since the detection steps consist of differentiation, moving averaging, squaring, and adaptive threshold comparing blocks resulting in more computational complexity. In [5], an integrate and fire sampler is presented, that integrates the input signal across a predetermined time frame and detects the QRS complex of input ECG signal. This approach is vulnerable to electrodes mobility and saturated distortions. Simpler approaches such as those based on the first-order derivative [6], [7] and the second-order derivative [8] have been implemented with extremely low power consumption. Although they yield lower accuracy, over the previous few decades, the majority of real-time QRS-detection circuits are implemented through the derivative technique, with the goal of primarily improving the speed and minimizing the consumed die area and power consumption.

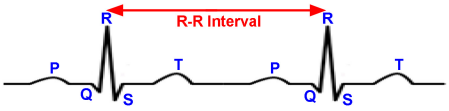

Fig. 1. Sample of the realistic ECG signal.

In this brief, the performance of the first-order derivative-based slope-detection circuit in [7] is considerably improved using a time-based differentiator circuit instead of the voltage differentiator and also two D-FFs for threshold comparing instead of voltage comparators in the slope detector circuit. This circuit does not use any op-amp in the differentiator block and voltage comparators in the slope detector block. So, the power consumption of the proposed circuit is significantly reduced which is about 62.45% compared to [7]. The simulation results of this circuit with 48 different ECG records from the MIT-BIH arrhythmia database [9] verify that this circuit can detect QRS complexes exactly. The detection error rate of the proposed QRS-detection circuit is about 1.49% and achieves the sensitivity and positive prediction rate about 99.26%, and 99.25%, respectively. This circuit is simulated in TSMC 0.18 μm CMOS technology at 500 Hz sampling frequency with about 39.8 nW power consumption.

The rest of this brief is organized as follows. Section II presents the background of the first-order derivative-based QRS-detection approach and defines the concept of the proposed time domain QRS-detection circuit. Section III shows the circuit level design details. Section IV presents the simulation results, and Section V concludes this brief.

II. Proposed QRS-Detection Circuit Structure

The overall structure of a QRS-detection system contains the analog front-end circuit and the back-end QRS-detection circuit. This brief discusses about the back-end QRS-detection circuit and similar to [10], [11], it is assumed that the pre-amplified and filtered analog input signals around 0.3 V are applied to the QRS-detection circuit. One of the simplest slope-detection approaches is the first-order derivative-based circuit, which calculates the derivative of the input signal and compares it with specified threshold values as shown in Fig. 2 [7]. The main advantage of this approach is its fast detection time which makes it as the best candidate for real-time applications. This circuit includes a switched-capacitor differentiator circuit and two voltage comparators to compare the differentiator output with two predefined threshold values

Manuscript received 5 July 2023; accepted 19 July 2023. Date of publication 21 July 2023; date of current version 8 January 2024. This brief was recommended by Associate Editor D. John. *(Corresponding author: Mohammad Yavari.)*

The authors are with the Integrated Circuits Design Laboratory, Department of Electrical Engineering, Amirkabir University of Technology (Tehran Polytechnic), Tehran 15875-4413, Iran (e-mail: myavari@aut.ac.ir).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TCSII.2023.3297901.

Digital Object Identifier 10.1109/TCSII.2023.3297901

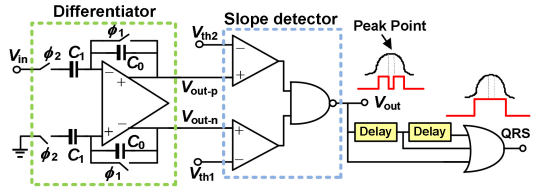

Fig. 2. First-order derivative-based slope-detection circuit [7].

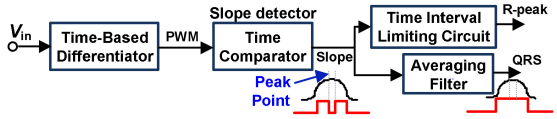

Fig. 3. The block diagram of the proposed first-order derivative-based QRS-detection circuit in time domain.

to detect the high slope components of the input signal. In detecting the high slope regions of the input signal, the peak regions are not detected. So, the last delay blocks and OR gate are used to detect the downward pulses at peak regions of the detected high slope data. This circuit uses a power-hungry op-amp in the differentiator circuit and two voltage comparators to detect the QRS complexes of the input signal, which leads to more power consumption.

To resolve these problems, the first-order derivative-based QRS-detection circuit is implemented in time domain in this brief. The block diagram of the proposed idea is shown in Fig. 3. First, the derivative of the input signal is calculated based on the proposed time-based differentiator circuit. This circuit generates a one-bit pulse width modulated (PWM) output data in which the pulse width of the output data at every clock cycle is proportional to the slope information of the input signal. Then, a time domain comparator is used to detect the high slope regions of the input signal. The time domain comparator block at every clock cycle compares the pulse width of the first step output PWM data with the pulse width of the reference clock signal as a threshold voltage. If the falling edge of the output PWM data be earlier than the rising edge of the reference clock signal or be later than the falling edge of the reference clock signal, these regions will be identified as high slope regions of the input signal. Then, at the last stage, an averaging filter is used to remove the downward pulse at detected high slope regions.

Although this circuit can detect a large number of QRS complexes exactly, some high activity regions in abnormal ECG signals may be incorrectly detected as QRS complexes. For this purpose, an additional time interval limiting circuit has been used to prevent the misidentification of the peaks at a specified time interval from truly detected QRS complexes. In the proposed structure, any power-hungry op-amp is not needed in the differentiator circuit, and hence, it can be designed with low power consumption. Also, this structure uses two D-FFs instead of two voltage comparators in the slope detector stage resulting in more power saving and simple implementation. The circuit level details of the proposed work will be discussed in the following section.

III. Circuit Level Design

The circuit level structure of the presented time-based QRS-detection circuit is shown in Fig. 4. This circuit is composed of a time-based differentiator, a time comparator, an averaging filter, and a time interval limiting block. The structure of the containing blocks is explained in the following sub-sections.

A. Proposed Time-Based Differentiator Circuit

The concept of a differentiator circuit is finding the input signal changes over the constant sampling period. So the first-order derivative of the input signal over the constant sampling frequency can be expressed as $V_{in}[n] - V_{in}[n-1]$.

Then, to have the slope information of the input signal in the time domain, a ramp comparator can be used as the voltage to time converter. By applying the difference signal to the input of the ramp comparator, the pulse width of the output data at every sampling time will be equal to the slope information of the input signal in time domain and it can be expressed as [12]

$$T[n] = \frac{T_r}{V_{r,\max}}(V_{in}[n] - V_{in}[n-1]) \tag{1}$$

where T_r and $V_{r,\max}$ denote the duration and the maximum amplitude of the ramp signal, respectively. In the proposed circuit, $V_{\text{in}}[n-1]$ can be evaluated by integrating the output PWM data using a simple charge-pump integrator circuit. As shown in Fig. 5, the time-based differentiator circuit includes a ramp generator, a comparator, a subtractor, and an integrator. In the ramp generating circuit, the ramp signal is generated by charging and discharging the capacitor C_R with a constant current source, I_R. The charging and discharging phases of the capacitor are controlled by the transistor M_R. The start signal determines the repeating frequency of the generated ramp signal. In this design, the difference signal is compared to the ramp signal. So the required ramp amplitude is small. To realize a low amplitude ramp signal and considering the existing trade-off between the capacitor size and minimum stable current value, the time duration of the ramp signal, T_r, is chosen to be 1/8 of the start signal time duration, T_{CLK}. This scales down the flicker noise power effect of the ramp generator circuit with the coefficient of 1/8. In this design, a passive subtractor circuit is used due to its ultra-low power usage and easier construction. The operation of this subtractor circuit is controlled with two φ_1 and φ_2 non-overlapping clock phases and the output voltage, $V_d[n]$, will be equal to the difference voltage of $V_{in}[n]-V_{int}[n-1]$. As shown in Fig. 5, $V_{int}[n-1]$ is the output of the integrator circuit which is generated from the output PWM data. The integrator is realized by a charge-pump circuit. It integrates the output PWM data by charging and discharging the integrating capacitor, C_{CP}, with equal charging and discharging current sources, I_{sink} and I_{source}, when the start signal is low. Equal currents of I_{sink} and I_{source} are generated using wide-swing cascode current mirrors. The transistors M_{C1} and M_{C2} are used to control the integrating time interval of the charge-pump circuit. The utilized hysteresis comparator in [12] is used for this design with a 10 nA bias current. Monte Carlo simulation results exhibit an average input-referred offset voltage of -1.38 mV with 9.83 mV standard deviation for 1000 samples run resulting in about 29.5 mV input offset voltage.

In this structure, the ramp comparison is done within the feedback loop. For PVT compensation, it is important that any change in ramp slope, I_R/C_R, to be followed by the difference

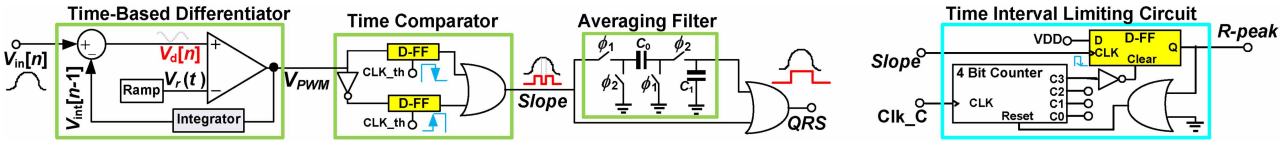

Fig. 4. The total circuit level structure of the proposed time-based QRS-detection circuit.

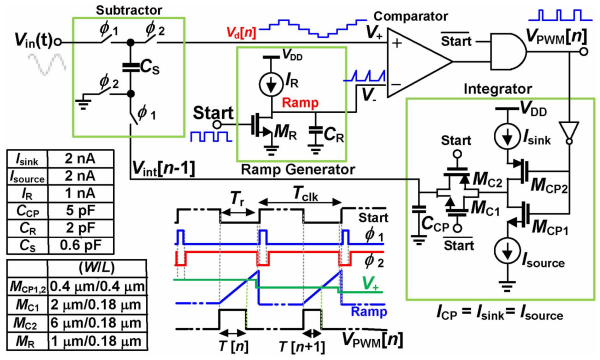

Fig. 5. Total structure of the proposed time-based differentiator circuit.

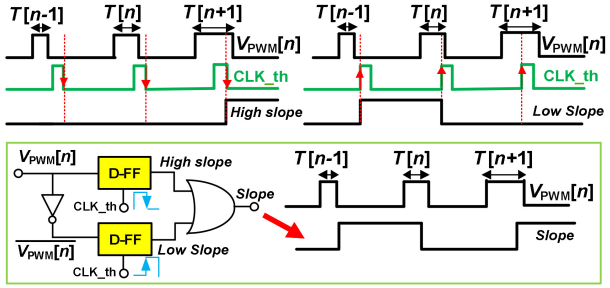

Fig. 6. Time comparator operation.

signal, $V_d[n]$. The difference signal function can be obtained as

$$V_d[n] = V_{in}[n] - 2\frac{C_R \times I_{CP}}{C_{CP} \times I_R} V_d[n-1] + \frac{I_{CP}}{C_{CP}} T_r \qquad (2)$$

In the second term of $V_d[n]$, the ratios of C_R/C_{CP} and I_{CP}/I_R are almost PVT insensitive since although the absolute value of capacitors and current sources highly depend on PVT conditions, the ratio of capacitors and current sources are almost PVT robust. The last term of $V_d[n]$ is constant and adjusts the DC level of the difference signal proportional to any change in the ramp slope. In this term, the ratio of I_{CP}/C_{CP} directly tracks the ratio of I_R/C_R in the ramp function. Hence, any PVT effect on the ramp slope is directly followed by difference signal DC level. So, the PVT effect on the circuit operation is compensated with the negative feedback structure.

B. Proposed Time Comparator Circuit

Since the output of the time-based differentiator circuit is the PWM data, a time comparator is used for threshold comparison. An edge-triggered D-FF can be used as a time comparator in time-based circuits. As demonstrated in Fig. 6, the input PWM waveform is compared with the reference clock signal, CLK_th, as the threshold voltage. To achieve good accuracy, the threshold voltage value is selected to be 0.6 of the input signal maximum slope [13]. With scaling this voltage to time domain at the time duration of the ramp signal, the reference clock signal duration is obtained as 22 us, which is generated at the middle of the ramp signal time duration. The upper D-FF block is sensitive to the falling edge of the clock. At the falling edge of the CLK_th, if the falling edge of the input PWM data was later than the falling edge of the CLK_th signal, then the output of the upper D-FF will be a logic one. This means that the slope of the input signal is greater than the predefined reference value. On the contrary, the bottom D-FF block is sensitive to the rising edge of the clock. At the rising edge of the CLK_th, if the falling edge of the input PWM data was earlier than the rising edge of the CLK_th signal, the output of the bottom D-FF will be a logic one. This means that the slope of the input signal is lower than the predefined reference value. For low activity regions of the input signal, the time comparator output will be zero. Then for detection of the QRS complex regions, a logical OR operation is applied to the output of the upper and bottom D-FF blocks.

C. Averaging Filter

At the last stage of Fig. 4, an averaging filter is used to remove the downward pulses at peak regions of the detected high slope data from the time comparator output. Generally, a low-pass filter with a very low cut-off frequency can be used as an averaging filter. Due to the static power consumption of the analog active low-pass filters, a passive low-pass filter is used for this design. The operation of this circuit is controlled with two non-overlapping control signals of φ_1 and φ_2. By choosing C_0 equal to 20 fF, C_1 equal to 400 fF, and the sampling frequency of 500 Hz, the low cut-off frequency is obtained about 3.79 Hz. The circuit is designed for this low cut-off frequency according to the maximum width of the QRS complexes with some design margin.

D. Time Interval Limiting Circuit

In the QRS-detector circuit, high activity regions in abnormal ECG signals may be incorrectly detected as QRS complexes. To resolve this issue, in some QRS-detector circuits, a time interval limiting circuit is used [14], [15]. The time interval limiting circuit for this design is illustrated in Fig. 4. This circuit includes a 4-bit up-counter, a D-FF circuit, and a logical OR gate. According to time interval information between successive QRS complexes in the MIT-BIH arrhythmia database, to limit the minimum time interval between successive QRS complexes to 250 ms, a 4-bit up-counter which counts with a 31.25 Hz clock signal is used. The reset input of the counter must be activated when an R-peak is detected. So, a logical OR of the R-peak and global gnd is applied to the reset input of the counter. When the counters most significant bit (MSB) becomes high, the D-FF clear input is disabled and at the falling edge of the CLK, the D-FF output becomes one, and hence, the R-peak is detected.

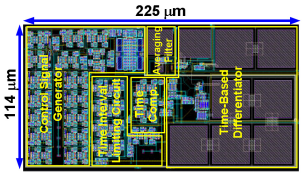

Fig. 7. Layout of the proposed QRS-detection circuit.

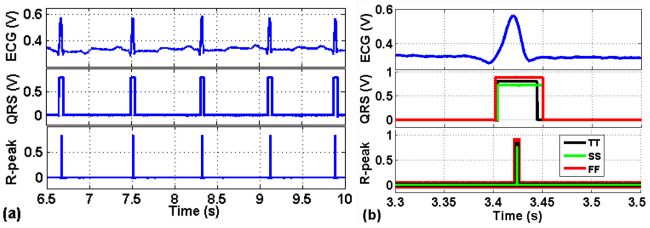

Fig. 8. (a) Post-layout simulation results of the proposed circuit using Tape 100 of the MIT/BIH arrhythmia database by enabling the circuit transient noise and (b) functionality test simulation results in PVT corners (TT at 27°C and 0.8 V, SS at 85°C and 0.72 V, FF at -40°C and 0.88 V).

IV. Post-Layout Simulation Results

To evaluate the performance parameters of the proposed first-order derivative-based QRS-detection circuit in time domain, it is designed with TSMC 180 nm CMOS process and simulated in Cadence Spectre-RF. This circuit works at a low supply voltage of 0.8 V. The circuit is designed to work in sub-threshold region. The operating frequency of the QRS-detection circuit is chosen to be 500 Hz for this design. The involved control signals of the proposed circuit are Start, φ_1, φ_2, CLK_th, and Clk_C which are derived from the system external clock signal using the control signal generator block. The original input clock frequency of 48 kHz is applied to the input of the control signal generator. Then the required control signals are obtained by using the frequency dividers, pulse width adjusting circuits, D-FF blocks, and a non-overlapping clock generator circuit. The layout of the proposed QRS-detection circuit is shown in Fig. 7. This circuit occupies the silicon die area of 0.026 mm^2. The simulated root mean square value of the input-referred noise voltage at the ECG signal bandwidth of 0.5 to 150 Hz is equal to 76.35 μVrms. The flicker noise impact is reduced because of the small ramp duration and using the switched biasing technique [16].

By enabling the circuit transient noise in Cadence Virtuoso, the post-layout simulation result with an input waveform of the realistic ECG signal and the output waveforms of the averaging filter and time interval limiting blocks are shown in Fig. 8(a). This shows the proper operation of each block. The circuit output is one-bit data which is activated when a QRS complex is appeared. By applying Tape 100 of the MIT/BIH arrhythmia database as the input signal, the proposed circuit consumes 39.8 nW total power. The leakage power portion is about 3.74% of total power. The power consumption of the time-based differentiator, time comparator, averaging filter, and time interval limiting blocks are 24.77 nW, 0.173 nW, 0.016 nW, and 0.417 nW, respectively. Other blocks including the logic gates, clock, and bias generating circuits consume about 14.42 nW. The functionality test simulation results in different process corner cases, power supply voltage, and temperature (PVT) variations are shown in Fig. 8(b) indicating its proper performance. The PVT variations do not affect the classification accuracy. Also, the maximum power variation in PVT corner cases is from 39.08 nW to 43.89 nW.

TABLE I
Performance of this Brife with MIT-BIH Database

Tape	SE	PP	DER	ACC	SP	Tape	SE	PP	DER	ACC	SP
100	100	100	0	100	100	201	96.99	99.95	3.06	98.47	99.95
101	99.84	99.47	0.7	99.65	99.46	202	99.77	99.77	0.47	99.77	99.77
102	100	99.95	0.05	99.98	99.95	203	95.91	96.13	7.95	96.02	96.14
103	100	99.9	0.1	99.95	99.9	205	99.85	99.81	0.34	99.83	99.81
104	98.83	97.78	3.41	98.3	97.76	207	96.38	98.13	5.46	97.27	98.16
105	99.26	97.44	3.34	98.33	97.4	208	98.88	99.56	1.56	99.22	99.56
106	99.61	98.87	1.53	99.24	98.87	209	99.8	99.87	0.33	99.83	99.87
107	99.49	99.72	0.8	99.6	99.72	210	99.21	97.51	3.32	98.34	97.47
108	86.78	90.53	22.29	88.85	90.92	212	99.78	99.64	0.58	99.71	99.64
109	99.8	99.57	0.63	99.68	99.57	213	99.94	99.69	0.37	99.82	99.69
111	99.86	99.72	0.42	99.79	99.72	214	99.56	99.73	0.71	99.65	99.73
112	100	99.88	0.12	99.94	99.88	215	99.91	99.76	0.33	99.84	99.76
113	100	100	0	100	100	217	99.82	99.64	0.54	99.73	99.64
114	99.95	99.42	0.64	99.68	99.41	219	100	100	0	100	100
115	100	100	0	100	100	220	100	100	0	100	100
116	99.09	99.79	1.12	99.44	99.79	221	99.71	99.83	0.45	99.77	99.84
117	100	99.55	0.46	99.77	99.54	222	99.88	99	1.13	99.44	98.99
118	99.91	99.56	0.53	99.74	99.56	223	99.92	99.92	0.15	99.92	99.92
119	100	99.9	0.1	99.95	99.9	228	96.35	97.06	6.58	96.71	97.08
121	99.89	99.52	0.59	99.7	99.52	230	100	99.47	0.53	99.73	99.47
122	100	100	0	100	100	231	100	99.87	0.13	99.94	99.87
123	99.74	99.93	0.33	99.84	99.93	232	99.83	99.83	0.34	99.83	99.83
124	100	99.82	0.19	99.91	99.81	233	99.87	99.81	0.32	99.84	99.81
200	98.77	98.62	2.61	98.69	98.62	234	99.89	100	0.11	99.95	100
Total	**SE=99.26**		**PP=99.25**			**DER=1.49**		**ACC=99.26**		**SP=99.25**	

$SE(\%) = TP/(TP+FN)\times 100$. $PP(\%) = TP/(TP+FP)\times 100$.
$DER(\%) = (FN+FP)/\text{Total Beats}\times 100$. Total Beats = $TP+FN$
$ACC(\%) = (TP+TN)/(TP+FP+FN+TN)\times 100$. $SP(\%) = TN/(TN+FP)\times 100$.
TP is the number of truly detected beats.
TN is the number of intervals that truly not contain any detected beats.
FN is the number of true beats that are not detected.
FP is the number of false positive detected beats.

TABLE II
The Performance Estimation on Various Input Databases

Data Base	Number of Records	SE	PP	DER	ACC	SP
MIT-BIH	48	99.26	99.25	1.49	99.26	99.25
PTB-XL	500 (Randomly Selected)*	99.08	97.97	2.98	98.51	97.94
NSR**	18	99.4	98.62	1.99	98.71	98.61
NST***	2 (SNDR = 0 dB)	94.02	75.21	36.97	81.51	69.01
	2 (SNDR = 6 dB)	99.03	97.41	3.58	98.2	97.37

*100 records from each class of PTB-XL database are randomly selected which are sampled at 500 Hz.
**NSR: Normal sinus rhythm database which is sampled at 128 Hz.
***NST: Noise stress test database which is sampled at 360 Hz.

The proposed QRS-detection circuit is modeled and simulated in MATLAB with 76.35 μVrms additive Gaussian noise effect of the circuit input-referred noise, about 29.5 mV input offset voltage of the comparator, and sampling clock jitter effect of 1 ns to evaluate the performance of the system by all 48 recorded ECG signals from the MIT-BIH arrhythmia database. Each of these records contains a 30-minute waveform of different ECG signals. The simulation results are listed in Table I. In this table, various parameters have been calculated to evaluate the performance of the circuit. These parameters include *SE*, *PP*, *DER, ACC,* and *SP* where *SE* denotes the sensitivity and circuit capability for truly detection of the QRS complexes, *PP* denotes the positive prediction rate, *DER* illustrates the detection error rate, *ACC* denotes the detection accuracy, and *SP* illustrates the specificity [17]. As it is observed, the average total sensitivity, positive prediction rate, detection error rate, accuracy, and specificity are 99.26%,

TABLE III
COMPARISON OF THIS BRIEF WITH SEVERAL QRS DETECTION CIRCUITS

Reference	Tech. (nm)	V_{DD} (V)	Type	Power (nW)	Area (mm^2)	Se (%)	PP (%)
MEJO'21 [14]	180	1.8	Energy-Derivative	790	0.011	97.81	99.71
AEU'21 [15]*	130	1.2	Energy-Derivative	31.5	0.097	99.17	99.36
TBCAS'21 [10]	180	1	Delta-Modulators	151	0.248	99.08	99.76
TBCAS'17 [18]@	180	1	Haar-Wavelet	410	0.484	99.6	99.77
TCASII'18 [19]	350	1.5	Morphologic-Filter	1500	--	99.82	99.71
TBCAS'18 [20]**	130	±0.6	Delta-Modulators	720	0.29	99.17*	99.55*
TBCAS'14 [11]$	130	0.3	Level-Crossing	220	0.36	97.76*	98.59*
SJO'22 [21]	180+130	1	Delta-Modulators	1660	0.63	98.67	98.84
JBHI'14 [22]*	130	1.2	Level-Crossing	447	0.016	98.89	99.40
TBCAS'12 [23]	350	1.8	Spline-Wavelet	830	1.11	99.31	99.7
INT'23 [24]*	180	1.8	LPF + Integrator	15.77	0.078	99.13	99.41
This Work*	180	0.8	Time-Derivative	39.8	0.026	99.26	99.25

* Simulation results ** QRS detection and P and T wave detection.
@ Total power consumption and area of interface, controller and QRS detector.
$ Total power consumption and area of ADC and QRS detector.

99.25%, 1.49%, 99.26%, and 99.25%, respectively, which are in the acceptable range for ECG applications.

The circuit operates with proper performance for the input signal with low amplitude and baseline wander. Large input noise levels and large P waves degrade the performance of the circuit. In this design, the overall mean and standard deviation of the delay in detection of the QRS complexes are −10.24 ms and 12.14 ms, respectively, which is a good candidate for real-time detection of R-peaks. To estimate the detection performance of this circuit, the maximum deviation window size is chosen to be 150 ms [17]. Also, the performance of this circuit is estimated with some other databases such as PTB-XL, normal sinus rhythm, and noise stress test databases, which are sampled at different frequencies of 500, 128, and 360 Hz. As reported in Table II, the proposed circuit has proper performance with different databases which are sampled at various frequencies.

In Table III, the performance parameters of this brief in terms of power, area, sensitivity, and positive prediction rate are compared with several related QRS detection circuits. Compared to other reported works in this table, the structures based on wavelet transform [18], [23] and morphologic filters [19] have better sensitivity and positive prediction rate, but they use more power and demand a large area, which are not suitable for wearable and implantable ECG sensors. In comparison with level-crossing type [11], [22], delta-modulators type [10], [20], [21], integrator type [24], and derivative type [14], [15] structures, this brief achieves reasonable accuracy which is suitable for wearable and implantable circuits. The proposed circuit achieves the minimum power consumption among the reported QRS detection circuits listed in Table III except [15], [24]. Nonetheless, the area of the proposed work is considerably smaller than [15], [24]. Also, the area of the proposed circuit is less than other works except [14], [22] since it is implemented in time domain and the slope detector circuit is implemented using a simple time domain comparator. The proposed circuit does not need any complex algorithm or memory for QRS detection.

V. CONCLUSION

In this brief, a new ultra-low-power QRS-detection circuit is presented in time domain. By using the time domain differentiator and time comparator, the power consumption is significantly reduced since high power consuming components such as op-amp and voltage comparators are not required. The proposed QRS-detection circuit does not need any complex algorithm or memory, and hence, the required silicon die area is considerably reduced making it a proper candidate for implantable and wearable real-time ECG recording systems.

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