A Low-Power Delta-Modulation-Based ADC for Wearable Electrocardiogram Sensors

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***Abstract*—In this brief, a new ultra-low power analog-to-digital converter (ADC) based on delta (Δ)-modulation approach is presented for wearable Electrocardiogram (ECG) sensor systems. In the proposed structure, a voltage-to-time converter (VTC) is employed as the residue quantizer in Δ-modulation based ADC circuit. So, the requirement on the high-frequency sampling rate in such ADCs is relaxed and it can be realized with low-power consumption. This structure produces one-bit output data wherein the pulse-width of output data at every clock cycle is proportional to the input signal variation. Therefore, the output data rate is significantly reduced. The proposed ADC is designed in TSMC 0.18 μm CMOS technology and post-layout simulation results exhibit maximum 10.9 effective number of bits (ENOB) with 68.12 nW power from a 0.8 V power supply. This ADC circuit achieves a peak signal-to-noise and distortion ratio (SNDR) about 67.4 dB over ECG signal bandwidth with 4 kHz sampling frequency and occupies about 0.02 mm^2 silicon die area.**

***Index Terms*—Analog-to-digital converters, heart diseases, wearable electrocardiogram, delta-modulation.**

I. Introduction

HEART diseases are one of the major health concerns globally. In such disease, the patient needs continuous and constant monitoring of the heart condition. One of the systems for long-term and consistent tracking of cardiac operation is the wearable electrocardiogram (ECG) sensor [1]–[3].

Fig. 1 depicts the simplified schematic of a wearable ECG sensor [2]. A differential amplifier is utilized for amplifying the input signals. Then, the noise components outside of the signal bandwidth are rejected by a band-pass filter, and transmission line disturbances are suppressed by a notch filter. Finally, the output signal is digitized using an analog-to-digital converter (ADC). These sensors are battery-powered and needs very low power usage due to the strict requirement on the power budget. In such sensors, owing to the consistent tracking of the cardiac operation and the large volume of the generated data, effective power reduction occurs when we have the minimum use of wireless transmitter. So, designing ultra-low power ADC with a lower data rate, whereas satisfying the operational requirements of the wearable ECG sensors, becomes a major design challenge.

In recent years, Δ-modulator based converters have been frequently used for biomedical applications [3]–[7].

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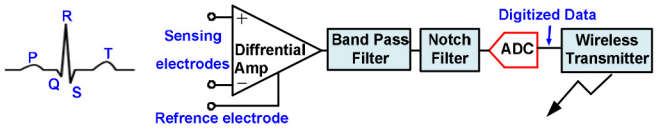


Fig. 1. Simplified schematic of a common wearable ECG sensor.

Δ-modulator is an ADC type that encodes the difference between the present and previous samples of the input signal and has the advantages of simple encoding and data-rate reduction for signal transmission. Several kinds of ADC circuits based on the Δ-modulator structure have been reported in literature. In standard Δ-modulator based circuits, the sampling frequency of the circuit is adjusted depending on the input signal slew rate, and therefore, the circuit needs a large sampling frequency for recovering the input analog signal [3]. Other structures are based on level-crossing (LC) Δ-modulated ADCs [4]. In these ADCs, in order to accurately detect the threshold crossing levels, high-performance blocks and the complete recognition of input signal specifications are needed. Moreover, the signal reconstruction time is affected by slope of the input signal that impacts the ADC's linearity. In [5], a successive approximation register (SAR) ADC acts as the residue quantizer in the Δ-modulator circuit. In such conditions, the SAR ADC also needs to be oversampled resulting in more power dissipation. In [6], [7], standard VCO-based ADC acts as the residue quantizer in Δ-modulator circuit. The main disadvantage of VCO-based ADCs is their nonlinearity contribution.

To resolve the issues of previous works, in this brief, a voltage-to-time converter (VTC) circuit is used as the residue quantizer in the Δ-modulator structure. So, the requirements on high-frequency sampling rate are reduced and the structure can be designed with less power. Also, this structure produces one-bit output data wherein the pulse-width of output data at every clock cycle is proportional to the input signal variation, resulting in a drastically lower output data rate. This ADC exhibits 10.9 effective number of bits (ENOB) with 4 kHz sampling frequency and 68.12 nW power consumption.

This brief is an extension of our previous work described in [8] with improved circuit design, more details on circuit analysis and design, and addition of the post-layout simulation results. This brief is arranged as follows. Section II introduces the construction and small-signal analysis of the presented Δ-modulation based ADC. Section III explains the circuit-level structure. Section IV provides the post-layout simulation results and finally, Section V concludes this brief.

II. Proposed Δ-Modulation Based ADC

In the following sub-sections, for the small-signal model development of this converter, the background on the

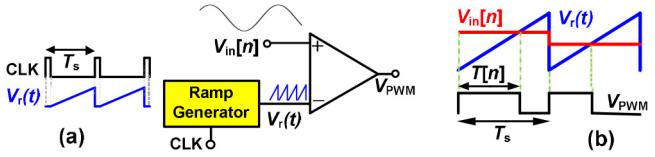


Fig. 2. (a) Block diagram of conventional VTC circuit [9], and (b) ramp comparator operation.

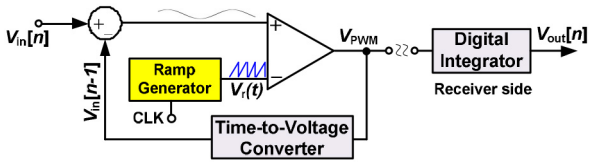


Fig. 3. Suggested Δ-modulation based ADC structure.

conventional VTC circuit is firstly described. Then, the structural details of the proposed ADC are presented.

A. Conventional VTC Circuit

As illustrated in Fig. 2(a), the conventional VTC circuit comprises a voltage comparator and a ramp generator [9]. Whenever the clock (CLK) signal value is zero, the ramp generator produces a linear slope ramp signal. Then, the comparator compares the sampled input signal with the ramp signal and produces a pulse width modulated (PWM) output waveform which its pulse width at every CLK cycle is proportional to the input signal amplitude. For the development of the proposed ADC small-signal model, the VTC transfer function must be defined. With assuming the ramp function as

$$V_r(t) = V_{r,\max} \times \frac{t}{T_s} \tag{1}$$

where $V_{r,\max}$ indicates the maximum amplitude of the ramp signal and T_s denotes the ramp signal's time period. As illustrated in Fig. 2(b), when the amplitude of the time sampled input signal is equal to the ramp amplitude, the pulse width of the output PWM waveform will be $T[n]$. So, we have:

$$V_{in}[n] = V_r(T[n]) = V_{r,\max} \times T[n]/T_s \tag{2}$$

Hence, the transfer function of the VTC circuit is denoted by

$$\frac{T[n]}{V_{in}[n]} = \frac{T_s}{V_{r,\max}} = \frac{1}{f_s \times V_{r,\max}} \tag{3}$$

where $f_s = 1/T_s$ indicates the repetition frequency of the ramp signal. For proper operation, the VTC circuit requires a high-frequency ramp signal and the comparator should have a small delay. Also, the ramp amplitude is adjusted depending on the amplitude of the input signal, and hence, a high linearity ramp signal is needed. These criteria necessitate the creation of a power-hungry structure.

B. Proposed Δ-Modulation Based ADC

In the proposed work, to overcome the VTC circuit design issues, a VTC circuit is employed as the residue quantizer in the Δ-modulation based ADC. Therefore, the VTC circuit's input is the difference of two subsequent samples. Since the difference between subsequent samples is small, the requirements of small comparator delay and high ramp signal repeating frequency are reduced and it can be realized with less power. Fig. 3 illustrates the presented Δ-modulation based ADC block diagram. The output PWM waveform is converted into $V_{\text{in}}[n-1]$ voltage using a time-to-voltage converter in the feedback path of this structure. This voltage ($V_{\text{in}}[n-1]$) is subtracted from the input signal ($V_{\text{in}}[n]$), which is sampled in the subtractor circuit, in order to produce the difference of the two subsequent samples. Then at every CLK cycle, the output PWM waveform is produced by comparing the subtracted signal with the ramp signal. In this structure, the amplitude of the ramp signal is adjusted based on the difference of two consecutive input signal amplitudes. Therefore, the linearity requirement of the ramp signal is highly reduced. Also, this circuit produces one-bit output data which reduces the output data rate, significantly. Finally, in order to have a minimum data transmission rate, a digital integrator is utilized at the receiver side to reconstruct the input signal from the output PWM waveform.

In Δ-modulation-based ADCs, when the input signal has relatively large amplitude changes, the modulation signal cannot exactly track the input signal changes, which results in slope overload. In this structure, the Δ-modulator circuit is combined with the VTC circuit. The quantization levels in the VTC circuit are determined by the digital integrator resolution. So, in this circuit, like differential pulse-code modulation (DPCM) circuit [10], the prediction is combined with multilevel quantizing and the slope tracking condition is relaxed as follows:

$$f_s(q-1)\Delta \geq \left|\frac{dx(t)}{dt}\right|_{\max} \tag{4}$$

where at the constant sampling period, T_s, Δ specifies the maximum step-size magnitude and q denotes the quantization levels in the VTC circuit. For 10-bit resolution, the value of q is very larger than one. So according to Eq. (4), the sampling frequency (f_s) can be selected nearly to Nyquist rate of the input signal bandwidth. On the other hand, according to [11], in PWM converters, at least 8 times oversampling is required to reduce the nonlinearity effects of VTC circuit. Therefore, based on the ECG signal specifications, a sampling frequency of 4 kHz is selected in this design.

Fig. 4(a) depicts the suggested Δ-modulation based ADC's small-signal model where an integrator with a pole at ω_{int} is used in the feedback path as a time-to-voltage converter. For simplicity, in order to reconstruct the input signal from output one-bit PWM data, an integrator is assumed with the same transfer function as the feedback path integrator. Hence, the total small-signal transfer function of the ADC is obtained as:

$$TF = \frac{V_{out}(s)}{V_{in}(s)} = \frac{\frac{1}{f_s \times V_{r,\max}}}{1 + \frac{1}{f_s \times V_{r,\max}} \times \frac{k}{s+\omega_{\text{int}}}} \times \frac{k}{s+\omega_{\text{int}}} \tag{5}$$

By assuming $s << \omega_{\text{int}}$, the transfer function of the ADC after reconstruction will be approximately equal to one. According to behavioral simulation results in MATLAB/Simulink environment, the proposed ADC is tolerant to the gain and phase mismatches between the feedback path and output digital integrators. With ±5% gain mismatch ($k(1+\delta_k)$) and ±1% phase mismatch ($\omega_{\text{int}}(1+\delta_\omega)$) at the output integrator transfer function, the simulated signal-to-noise and distortion ratio (SNDR) value degrades only about ±1 dB.

C. Noise Analysis

Fig. 4(b) depicts the suggested ADC's small-signal model by considering the main thermal noise sources of the circuit. In this model, the noise of the comparator would be specified by the thermal noise of the comparator input transistors,

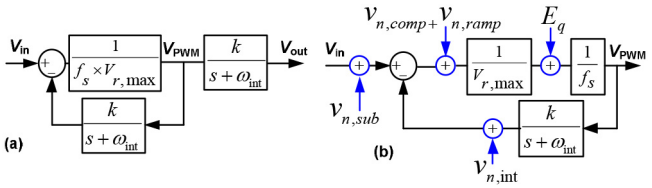


Fig. 4. Small-signal model of the proposed (a) Δ-modulation based ADC and (b) converter by considering the main thermal noise sources.

and the noise of the ramp generator, feedback integrator and subtractor would be determined by the switching noise of the corresponding capacitors. Also, the total time-based quantization noise power is equal to $T_{CLK}^2/12$ [9]. Hence, the total input-referred thermal noise power is given by:

$$V_{n,in,th}^2 = 2 \times \frac{4kT\gamma}{g_m} \cdot \Delta f + \frac{kT}{C_0} + \frac{kT}{C_{CP}} + \frac{2kT}{C_S} + V_{r,\max}^2 \cdot \frac{T_{CLK}^2}{12} \tag{6}$$

where γ is the excess noise factor, k is the Boltzmann's constant, g_m is the transconductance of the comparator input transistors, Δf is the bandwidth of the circuit (which is equal to $f_s/2$), C_0 is the ramp generator output capacitor, C_{CP} is the charge-pump output capacitor, and C_S is the subtracting capacitor. According to Eq. (6), the total input-referred thermal noise root power in signal bandwidth (250 Hz) is obtained as 42.6 μV_{rms}.

The total input-referred flicker noise power is obtained as:

$$V_{n,in,f}^2 \approx \left[\left(\frac{2g_{msi}^2}{W_{si}L_{si}C_{CP}^2} + \frac{3g_{mi}^2}{2W_iL_iC_0^2}\right) \times \frac{K}{8\pi^2 C_{\text{ox}}}\left(\frac{1}{f_L^2} - \frac{1}{f_H^2}\right)\right] + \left(\frac{2K}{W_1L_1C_{\text{ox}}} \ln\frac{f_H}{f_L}\right) \tag{7}$$

where K is a process-dependent constant, C_{ox} is the oxide capacitance density, f_H and f_L represent the maximum and minimum input signal frequencies, respectively. The first and second term denote the noise contribution of the charge-pump and ramp generator circuits, respectively, and their noise contribution is reduced by using large C_{CP} and C_0 capacitors. W, L, and g_m, denote the channel width, channel length, and transconductance of the corresponding transistors. The last term denotes the noise contribution of the comparator circuit where W_1, and L_1 are the channel width and length of the comparator input transistors, respectively. In this design, the flicker noise contribution of these blocks is reduced by using the switched bias technique [12]. The main idea of switched bias technique is to switch the bias transistor between accumulation and strong inversion regions. So, some of the flicker noise states of the circuit are deleted, and hence, the impact of $1/f$ noise is reduced.

III. Circuit-Level Design

Fig. 5 shows the proposed Δ-modulation based ADC structure. This structure is composed of a ramp generator, a subtractor, a comparator, an integrator, and a digital integrator. In the following subsections, the circuit level details of these blocks are explained.

A. Ramp Generator

Fig. 6(a) shows the structure of the ramp generator block. This structure contains a current source composed of M_1–M_4 transistors, C_0 capacitor, and M_0 transistor, which is activated

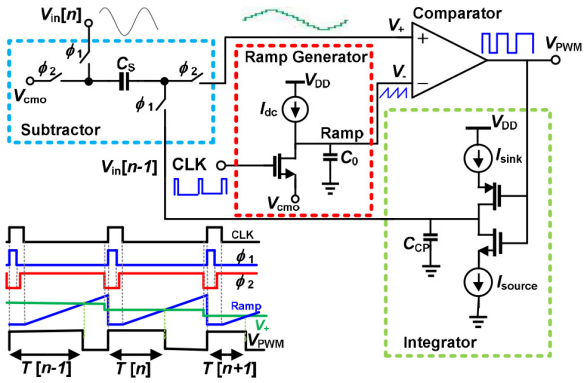


Fig. 5. Structure of the proposed Δ-modulation based ADC.

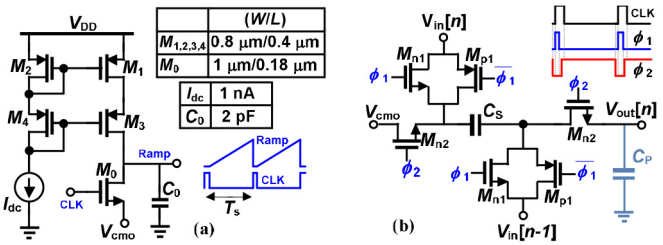


Fig. 6. (a) Ramp generator circuit, and (b) subtractor circuit.

by the CLK signal and used as a switch to control the charge and discharge of the C_0 capacitor. During the charge phase, the CLK signal is low, and therefore, the ramp signal is created by charging the C_0 by a constant current (I_{dc}). In the discharge phase, the CLK signal gets high making the M_0 transistor to turn on and discharge C_0 into V_{cmo}.

B. Subtractor Circuit

A low-power passive subtractor circuit as shown in Fig. 6(b) is chosen for this design. The subtractor circuit operation is controlled with two non-overlapping clock signals of ϕ_1 and ϕ_2. This structure is suited for low power applications and its input and output relationship is given by:

$$\frac{V_{out}[n]}{V_{in}[n] - V_{in}[n-1]} = \frac{-z^{-1}}{1 + \rho - \rho z^{-1}}, \quad \rho = \frac{C_P}{C_S} \tag{8}$$

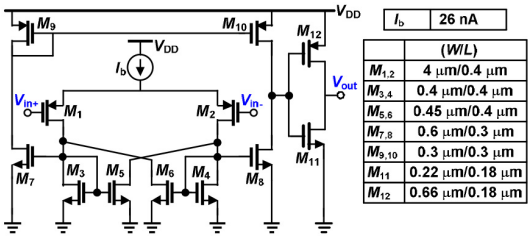
where C_S and C_P are the subtracting and parasitic capacitors of the subtractor output node, respectively. With assuming $C_P << C_S$, this function is simplified as $-z^{-1}$ and this circuit acts as a subtractor with a delay of one sample.

C. Comparator Circuit

In this design, the hysteresis comparator circuit of Fig. 7 is used which reduces the effect of input noise at the proper operation of the circuit. It contains the first stage with positive feedback, a second stage to increase the gain of the comparator and convert the differential input to a single-ended output, and an output stage to provide sharper output edges [13]. According to the simulation results, this comparator achieves about 60 dB gain and has 2.7 mV average input-referred offset voltage from a 0.8 V power supply voltage.

D. Integrator Circuit

A charge-pump integrator is used in the feedback path because of its simple implementation, low power consumption, and simple design. Fig. 8(a) shows the feedback integrator schematic by including a single C_{CP} capacitor and the same



I_b	26 nA

	(W/L)
$M_{1,2}$	4 μm/0.4 μm
$M_{3,4}$	0.4 μm/0.4 μm
$M_{5,6}$	0.45 μm/0.4 μm
$M_{7,8}$	0.6 μm/0.3 μm
$M_{9,10}$	0.3 μm/0.3 μm
M_{11}	0.22 μm/0.18 μm
M_{12}	0.66 μm/0.18 μm

Fig. 7. Comparator circuit [13].

charging and discharging current sources, I_{sink} and I_{source}. A wide-swing cascode current mirror has been used due to its high output impedance. Fig. 8(b) shows the current matching characteristic of the designed charge-pump circuit. The maximum current mismatch between I_{source} and I_{sink} is less than 20 pA when V_{out} ranges from 0.14 V to 0.68 V showing a current matching characteristic greater than 99%.

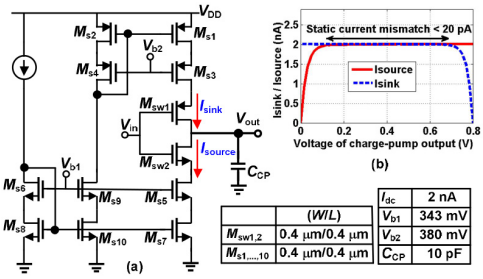
E. Digital Integrator

In time-based ADCs, the resolution of the ADC is determined by the time resolution of the digital integrator [9]. So, for N-bit required resolution, in the linear region of the ramp signal which is equal to $T_s/2$, the time resolution of the integrator (T_C) should be equal to $T_s/2^{N+1}$. Although for ECG signals, 11-bit resolution is adequate, as shown in Fig. 9(a), here a 12-bit up/down counter is used as the digital integrator to achieve the maximum SNDR. In up/down counter, at every counting clock cycle (f_c), it counts up or down by one-bit according to the output V_{PWM} data logic. Then the output of the integrator is down sampled.

IV. Post-Layout Simulation Results

The presented ADC has been simulated utilizing TSMC 0.18 μm CMOS technology in Cadence Spectre RF simulator. Because of the very long simulation time, the digital integrator circuit has been simulated in MATLAB/Simulink environment with 12-bit fixed point resolution. The layout of the simulated ADC is illustrated in Fig. 9(b). The core circuit occupies 0.02 mm^2 total silicon die area. The power supply of the circuit is 0.8 V. The total circuit consumes 68.12 nW power where 54 nW, 5.6 nW, and 1.6 nW are consumed by the comparator, feedback integrator, and ramp generator blocks, respectively. Other blocks including the bias and controlling signal generation circuits consume 6.8 nW power, approximately. Also 0.12 nW dynamic power is consumed by reference voltages and input source, V_{in}. The power consumption and area of the digital integrator is not included since it is realized at the receiver side like [1], [21]. The ramp signal repetition frequency determines the operation frequency of the presented ADC which is 4 kHz and the signal bandwidth is chosen to be 0.5 Hz to 250 Hz. According to the American Heart Association (AHA) standard [14], although the minimum signal bandwidth is recommended to be at least 150 Hz, in many studies to record high-frequency contents, the bandwidth is increased up to 250 Hz. The actual ECG signals acquired from the sensing electrodes have the amplitude between 50 μV to 10 mV [15]. So, the ADC dynamic range should be larger than 46 dB. In this design, to have some design margin, the targeted ENOB is about 10-bit according to the ECG signal specifications and considering a simple analog front-end without any variable gain block.

The simulated input-referred noise root power spectral density of the designed circuit is shown in Fig. 10(a). The noise integration in the signal bandwidth gives a root mean



	(W/L)
$M_{sw1,2}$	0.4 μm/0.4 μm
$M_{s1,...,10}$	0.4 μm/0.4 μm

I_{dc}	2 nA
V_{b1}	343 mV
V_{b2}	380 mV
C_{CP}	10 pF

Fig. 8. (a) Feedback integrator circuit, and (b) simulated static current mismatch.

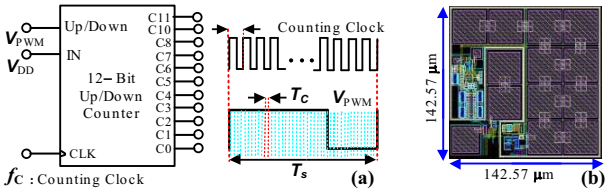


Fig. 9. (a) Digital integrator realization and (b) layout of the proposed ADC.

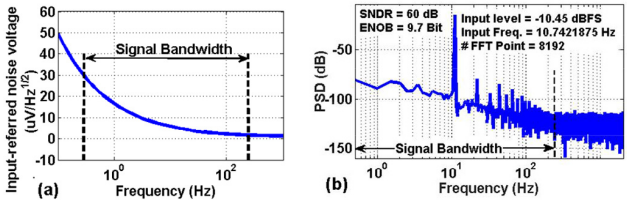


Fig. 10. (a) Input-referred noise root power spectral density and (b) simulated power spectral density (PSD) of the proposed ADC.

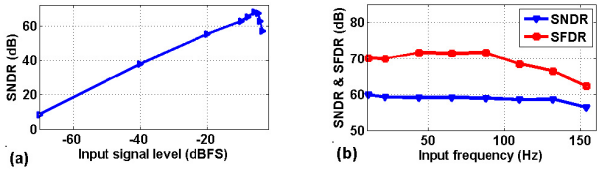


Fig. 11. (a) SNDR versus input signal level, and (b) SNDR and SFDR versus input signal frequency at −10.45 dBFS input level.

square (RMS) noise voltage about 60 μV_{rms}. In all transient simulations, the effect of circuit noise has been considered as well by enabling the transient noise option. The simulation result of the proposed ADC output spectrum for 10.7421875 Hz sinusoidal input signal with 300 mV peak-to-peak voltage is illustrated in Fig. 10(b). This input signal is chosen, since, the input ECG signal is first amplified to around 300 mV and then applied to the input of the ADC. The achieved SNDR at −10.45 dBFS input level is about 60 dB for the proposed Δ-modulation based ADC resulting in 9.7 ENOB. Table I summarizes the simulation results in several process corner cases, power supply voltage and temperature (PVT) changes to validate the correct operation of the suggested structure.

The simulated dynamic range of the proposed ADC is shown in Fig. 11(a). The achieved maximum SNDR is about 67.4 dB at −5 dBFS input signal. The dynamic performance of the ADC is shown in Fig. 11(b) with input signal frequency swept from 10 Hz to 154 Hz in the signal bandwidth. The performance of the suggested Δ-modulation based ADC is evaluated using an actual cardiac record from the MIT-BIH arrhythmia database [16].The constructed signal from this circuit output is shown in Fig. 12. According to the simulation

TABLE I
PVT SIMULATION RESULTS AT −10.45 DBFS INPUT LEVEL AND $f_S = 4$ KHZ

Parameter	TT @ VDD, 27°C	SS @ 0.9 VDD, 85°C	FF @ 1.1 VDD, -40°C
SNDR (dB)	60	59.7	61.95
ENOB (bit)	9.7	9.6	10
Power dissipation (nW)	68.12	60.61	79.2

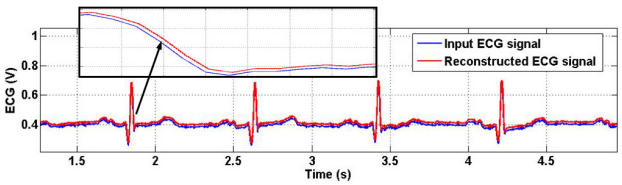


Fig. 12. Reconstructed ECG signal of the ADC output (circuit noise enabled).

TABLE II
PERFORMANCE COMPARISON OF THE PROPOSED ADC

Reference	Tech. (nm)	V_{DD} (V)	ADC Type	$SNDR_{max}$ (dB)	ENOB (bit)	f_s (kHz)	Power (µW)	FoM (fJ/Con.)
TCAS-I'20 [17]	130	0.6	SAR	59.5	10.72	10	0.81-1.88	48-110
TCAS-II'19 [18]	180	0.5	LC	35	5.6	---	0.06-0.22	627[@]
TCAS-I'18 [19]	180	1.5	SAR	68.1	11	40	2.9	33
MEJO'20 [20]	65	1.2	SAR	58.4	9.4	10	0.061	9
JOMS'19 [21][*]	180	0.8	LC	57.5	9	10	0.367[$]	72
AICSP'19 [22][*]	180	1	SAR	57.59[**]	9.3	5	0.42	133.26
TBCAS'19 [23]	180	1	SAR	57.6	10	20	0.5	24.4
JSSC'18 [6]	65	0.5	Time	51.78	8.3	---	1.28	184.5[@]
IA'20 [24][*]	90	0.7	SAR	56.4	9	32	5.8	34
This Work[*]	180	0.8	Time	67. 4	10.9	4	0.06812[$]	8.91

[*] Simulation results. [**] SQNR is reported. [@] Calculated based on Nyquist frequency.
[$] Excluding the digital integrator (up/down counter) power. FoM = Power /(f_s×2^{ENOB})

results, the system does not saturate and maintains proper performance in long time simulation.

Table II outlines the suggested Δ-modulation based ADC specifications and compares post-layout simulation results with several recently published articles in similar applications. To provide a fair comparison, like other references, the achieved maximum SNDR of the proposed ADC is reported in Table II. The proposed ADC structure greatly reduces the power consumption. Also, this circuit produces a one-bit output data stream at 4 kHz average sampling frequency, which results in a significant reduction in output data rate and further power reduction in the transmitter section. In comparison with [18], [21] which are all based on LC ADCs, the proposed ADC has higher SNDR, higher ENOB, and better FoM. Compared to [17], [19], [20], [22]–[24] which are based on SAR ADCs, the proposed ADC has a lower sampling frequency of 4 kHz and produces one-bit output data, resulting in higher power reduction during data transmission from the ADC output. In comparison with [6], which is a time-based ADC, the proposed ADC has the advantage of higher SNDR, higher ENOB, and reduced power dissipation. According to the simulation results, the proposed ADC has better FoM along with reduced output data rate verifying its effectiveness as a promising choice for wearable ECG sensor applications.

V. CONCLUSION

This brief proposes an ADC based on the Δ-modulation structure for wearable ECG sensor devices. The Δ-modulation technique is enabled by using a VTC circuit which alleviates the problems of the conventional VTC circuits. Furthermore, the suggested structure produces one-bit output data at a moderate sampling frequency of 4 kHz leading to a significant reduction in output data rate and greater power saving in the transmitter. This technique also significantly improves the ADC power usage and it is suitable for the quantization of low-activity ECG signals.

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