Microelectronics Journal 46 (2015) 198–206

Contents lists available at ScienceDirect

Microelectronics Journal

journal homepage: www.elsevier.com/locate/mejo

A UWB CMOS low-noise amplifier with noise reduction and linearity improvement techniques

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ARTICLE INFO

Article history:
Received 4 July 2014
Received in revised form
13 November 2014
Accepted 16 December 2014
Available online 9 January 2015

Keywords:
Ultra-wideband CMOS LNA
Linearity
Noise figure
Intermodulation distortion cancellation
Noise cancellation
Common-mode current

ABSTRACT

In this paper, a highly linear CMOS low noise amplifier (LNA) for ultra-wideband applications is presented. The proposed LNA improves both input second- and third-order intercept points (IIP2 and IIP3) by canceling the common-mode part of all intermodulation components from the output current. The proposed LNA structure creates equal common-mode currents with the opposite sign by cascading two differential pairs with a cross-connected output. These currents eliminate each other at the output and improve the linearity. Also, the proposed LNA improves the noise performance by canceling the thermal noise of the input and auxiliary transistors at the output. Detailed analysis is provided to show the effectiveness of the proposed LNA structure. Post-layout circuit level simulation results using a 90 nm RF CMOS process with Spectre-RF reveal 9.5 dB power gain, -3 dB bandwidth (BW_{-3dB}) of 8 GHz from 2.4 GHz to 10.4 GHz, and mean IIP3 and IIP2 of +13.1 dBm and +42.8 dBm, respectively. The simulated S_{11} is less than −11 dB in whole frequency range while the LNA consumes 14.8 mW from a single 1.2 V power supply.

1. Introduction

The demand for high-speed wireless communication systems increases the interest to the ultra-wideband (UWB) standard which emerges as a new technology to transmit high data rate (up to 1 Gb/s) in short distances (< 10 m) with low power [1]. As the first block of a multi-purpose/multi-standard radio-frequency front-end, the realization of broadband low-noise amplifiers (LNAs) are highly required. Broadband LNAs have to provide several requirements such as the broadband input impedance matching, high linearity, and low noise figure (NF) over a multi-GHz bandwidth which make the LNA design very critical and challenging.

The capability of CMOS technology to further reduce the circuit implementation area makes the realization of RF systems on chip more feasible. On the other hand, while the noise performance and bandwidth of CMOS LNAs improve with technology scaling, unfortunately the gain and linearity deteriorates mainly due to the high-field mobility degradation and power supply reduction [2]. Also, due to the presence of large number of in-band interferers and intermodulations (IMs) produced by blockers or transmitter leakage at the LNA input, the stringent linearity requirement over a wide frequency range is a big design challenge for UWB LNAs. Thus, some linearization techniques are necessary to satisfy the linearity requirements of UWB CMOS LNAs.

In broadband applications, both input second-order intercept point (IIP2) and input third-order intercept point (IIP3) are important. A high IIP2 ensures that the LNA stays linear in the presence of large interferences far from the fundamental tone which create a second-order intermodulation (IM2) component in the desired bandwidth. Most of the previously reported linearization techniques have been focused on IIP3 enhancement and there are a few ones improving both IIP2 and IIP3 such as the complementary derivative superposition method [3,4].

The negative feedback linearization for LNAs is not as effective as for base-band circuits, and hence, it is not so popular in high frequency applications [5]. The optimum biasing of the transistor overdrive voltage makes a linearity boost for narrowband input signals [6], but it is sensitive to the process variations. The feedforward is another method which is widely used in the circuit linearization. Derivative superposition [7,8], IM2 injection [9], noise and distortion cancellation [3,4,10], and the post distortion [11] are some categories of the feedforward scheme. The derivative superposition method uses an additional transistor's nonlinearity to cancel that of the main device, and involves MOS transistors working in triode [12] or in weak inversion region [13,14]. The common problem existing in all reported derivative superposition methods is the difficulty to match the transistors working at the different regions. The post distortion scheme uses all transistors in saturation and avoids the input matching degradation [3,15].

Caprio's cross-quad and Quinn's cascomp techniques are used widely in differential circuit linearization [16–18], but have some problems such as the stability and NF degradation. The cascomp

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http://dx.doi.org/10.1016/j.mejo.2014.12.007
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implementation degrades the NF because not only the noise of the auxiliary transistors is added to the output directly, but also these transistors amplify the noise of the input transistors at the output.

In this paper, a new structure is introduced which improves both the linearity and noise performance of CMOS LNAs simultaneously. The linearity is improved by reducing the IM components of the output currents. To do so, two auxiliary pairs as the cascomp structure are utilized to cancel the common-mode currents at the output. Furthermore, in the proposed LNA, the auxiliary paths eliminate the IM3 component of each other resulting in simultaneous improvement of IIP2 and IIP3. Also, the proposed LNA structure improves the noise performance of the cascomp technique by canceling the noise of the input and auxiliary transistors at the output.

The paper is organized as follows. The structure of the proposed LNA is presented in Section 2. Section 3 provides a detailed analysis of the proposed LNA including input matching, gain, linearity, and noise. The circuit level simulation results are presented in Section 4. Finally, Section 5 concludes the paper.

2. Structure of the proposed LNA

Fig. 1 shows the proposed UWB LNA structure where transistors M_5-M_8 are added to the differential structure of conventional cascode common-gate (CG) LNA [11,16,19–21]. M_1 and M_2 are the common-gate input transistors and designed to provide the broadband input impedance matching. M_3 and M_4 are utilized as cascode transistors to improve both the gain and reverse isolation. Transistors M_5 and M_6 are used as an auxiliary pair to cancel the common-mode parts of IM components at the output. These transistors provide a common-mode current equal to the input pair (M_1 and M_2) but with the opposite sign. Using only these transistors (M_5 and M_6) increases the NF because their noise is directly added at the output and also the noise of M_1 and M_2 appeared at the source of M_3 and M_4 is amplified by these transistors. Thus, transistors M_7 and M_8 are utilized to create a noise cancellation path to improve the noise performance. According to the simulation results, the total output noise added by M_7 and M_8 transistors is smaller than the removed noise of $M_{1,2}$ and $M_{5,6}$ by the noise cancellation path. Therefore, the overall NF of the proposed LNA is reduced compared to the conventional LNA. The resistor R_L in parallel with L_D and the output parasitic capacitance forms a passive RLC Load. The inductors L_S are used to resonate with the input parasitic capacitances. An RF MOS process with a separated and surrounded bulk with a guard ring is used to realize the proposed LNA. The resistors, inductors, and capacitors are implemented with the poly resistors, spiral inductors, and metal-isolator-metal (MIM) capacitors, respectively. A proper constant current biasing circuit is used to generate the bias voltages in the proposed LNA which is not shown in Fig. 1 for simplicity.

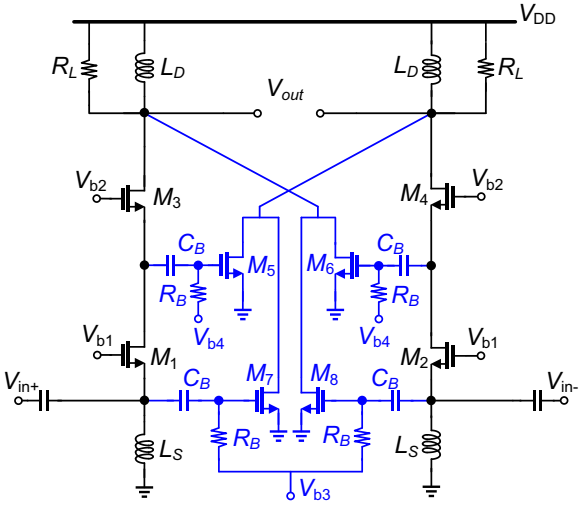

Fig. 1. Proposed UWB CMOS LNA.

Unlike the previous reported LNAs using the cascomp linearization technique, which usually degrades the NF, in the proposed structure the transistors M_7 and M_8 are used besides of the M_5 and M_6 transistors to improve the NF by canceling the noise of the input and auxiliary transistors. Also, these transistors are biased in strong and weak inversion regions, respectively, to create an equal g''_m but with an opposite phase resulting in a small-signal current without any IM3 distortion. Hence, not only the additional transistors (M_5–M_8) attenuate the IM2 and IM3 currents of input transistors significantly, but also eliminate the third-order nonlinear current of each other. It results in a significant enhancement in both IIP2 and IIP3 besides reducing the overall NF of the proposed LNA. Although using auxiliary transistors with different operating regions make their matching more challenging, but this is the expense of significant linearity improvement achieved with the proposed IM cancellation technique.

3. Analysis of the proposed LNA

In this section, the proposed LNA is analyzed in details. The required conditions to improve the linearity and reduce the noise figure are obtained. To consider the body effect in common-gate transistors, the total transconductance of the ith transistor is assumed as $g_{mt,i}=g_{mi}+g_{mbi}$.

3.1. Input matching

The common-gate configuration is chosen to provide the broadband input impedance matching. By assuming $g_m r_{ds} \gg 1$, the input impedance of the proposed LNA is obtained as follows:

$$Z_{in}(s) \approx \left(\frac{1}{g_{mt1}} \| sL_S \| \frac{1}{sC_{P1}}\right) \tag{1}$$

where g_{mt1} is the total transconductance of M_1 in which the body effect is also included, and $C_{P1}=C_{gs1}+C_{gs7}+(1+g_{m7}|Z_{out}|C_{gd7})+C_{sb1}$ is the total parasitic capacitance at the source of M_1.

To have a broadband input matching from 3.1 GHz to 10.6 GHz, the inductor L_S is designed to resonate with parasitic capacitance of C_{P1} at the center frequency of the bandwidth. Hence, the input matching condition is simplified as:

$$1/g_{mt1} = R_S \tag{2}$$

3.2. Gain

When the input matching condition is satisfied, the differential voltage gain of the proposed LNA is derived as:

$$A_v = \frac{1}{2}\left(g_{mt1}+g_{m6}+g_{m8}\right)|Z_{out}| \tag{3}$$

where Z_{out} is the output impedance of the proposed LNA at the output resonance frequency, $\omega_0=1/\sqrt{(C_{P3}L_D)}$, and it can be approximately written as:

$$Z_{out} \approx \left(\frac{1}{r_{ds6}}+\frac{1}{r_{ds8}}+\frac{1}{r_{ds3}+R_{D1}\left(1+g_{mt3}r_{ds3}\right)}+\frac{1}{R_L}\right)^{-1} \tag{4}$$

where $R_{D1}=R_B\|[r_{ds1}+(1+g_{mt1}r_{ds1})R_S]$ and C_{P3} is the output parasitic capacitance including $C_{db5,6}$, $C_{db7,8}$, $C_{db3,4}$ and $C_{gd3,4}$. As it is clear, due to the increased total transconductance, the differential voltage gain of the proposed LNA is increased compared to the conventional LNA at the cost of more power consumption.

3.3. Linearity

In a differential pair, the small-signal drain current of transistors can be decomposed into the common-mode and differential mode components as $i_d = i_{cm} + i_{diff}$. Thus, the intermodulation currents can be written as $i_{IMj} = i_{IMj,cm} + i_{IMj,diff}$, where i_{IMj} is the jth-order intermodulation current of an MOS transistor. The common-mode part, which is produced due to the nonlinearity and mismatch between the input transistors, degrades the circuit performance specially the linearity. Therefore, canceling the common-mode part of output current, which is the main idea of the proposed structure, improves the linearity specially IIP2 because the common-mode is the dominant part in the IM2 current [22]. Since the interaction between IM2 components at the frequency of $f_1 \pm f_2$ and $f_2 \pm f_1$, with fundamental tones (f_1 and f_2), introduces an IM3 component at the frequency of $2f_1 \pm f_2$ and $2f_2 \pm f_1$, respectively, the proposed common-mode canceling structure improves IIP3 by two ways. Firstly, it attenuates the IM3 component of output current. Secondly, it reduces the second-order interaction due to the significant IM2 attenuation.

In the following subsections, the effect of the proposed LNA structure on the linearity is analyzed in details.

3.3.1. IIP2 improvement analysis

According to Fig. 2(a), the output current of each branch (i_{out+} and i_{out-}) is formed by the current of three paths. Two pairs ($M_{1,2}$ and $M_{7,8}$) make a positive common-mode current, i_{cm}, and one pair (M_5 and M_6) creates an i_{cm} equal to them but with an opposite sign. By summing these currents, the common-mode parts are subtracted from each other in the output current, but the differential currents are added together due to the same sign. So, it makes the small-signal gain of the proposed LNA to be increased and IM currents to be reduced compared to the conventional counterpart.

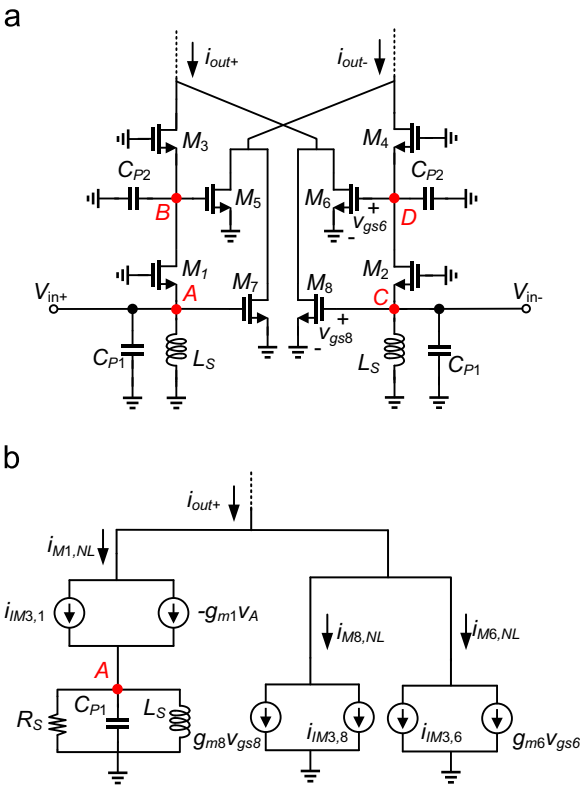

Fig. 2. Equivalent circuits used in linearity analysis: (a) equivalent circuit and (b) single-ended equivalent model of (a) used in IM3 distortion cancellation analysis.

By assuming i_j, i_{out+}, and i_{out-} to be the small-signal part of the drain current of M_j, and the output current of the right and left branches, respectively, in Fig. 2(a), we can write

$$i_1 = i_{diff} + i_{cm} \Rightarrow i_5 = \frac{-i_1}{g_{mt3}} g_{m5} = \left(\frac{g_{m5}}{g_{mt3}}\right)(-i_{diff} - i_{cm}) \tag{5}$$

$$i_2 = -i_{diff} + i_{cm} \Rightarrow i_6 = \frac{-i_2}{g_{mt4}} g_{m6} = \left(\frac{g_{m6}}{g_{mt4}}\right)(i_{diff} - i_{cm}) \tag{6}$$

The current of M_7 and M_8 transistors can be derived similar to i_5 and i_6, respectively. Thus, the output currents are obtained as follows:

$$i_{out+} = i_1 + i_6 + i_8 = i_{diff}\left(1 + \frac{g_{m6}}{g_{mt4}} - \frac{g_{m8}}{g_{mt2}}\right) + i_{cm}\left(1 - \frac{g_{m6}}{g_{mt4}} + \frac{g_{m8}}{g_{mt2}}\right) \tag{7}$$

$$i_{out-} = i_2 + i_5 + i_7 = -i_{diff}\left(1 + \frac{g_{m5}}{g_{mt3}} - \frac{g_{m7}}{g_{mt1}}\right) + i_{cm}\left(1 - \frac{g_{m5}}{g_{mt3}} + \frac{g_{m7}}{g_{mt1}}\right) \tag{8}$$

According to (7) and (8), the common-mode part of the output currents can be canceled if the following condition is satisfied:

$$g_{m5,6} = g_{mt3,4}\left(1 + \frac{g_{m7,8}}{g_{mt1,2}}\right) \tag{9}$$

This condition can be well satisfied by an appropriate choice of the transistors aspect ratio (W/L). If it is assumed that $g_{mt3,4} = g_{mt1,2}$, the common-mode current cancellation condition is simplified to $g_{m5,6} = g_{mt1,2} + g_{m7,8}$. At this condition, the first term of relations (7) and (8) is equal to $2i_{diff}$ and the second term is canceled. Hence, the proposed LNA structure increases the small-signal gain and reduces the IM2 part of the output currents significantly resulting in an increased IIP2.

3.3.2. IIP3 improvement analysis

As mentioned before, the proposed IM canceling structure improves IIP3 by attenuating the IM3 component of output current. Furthermore, the auxiliary transistors ($M_{5,6}$ and $M_{7,8}$) cancel the IM3 components of each other by biasing them in different operating regions. The following analysis confirms that the proposed structure cancels the third-order distortion generated by the input and auxiliary transistors. In this analysis, the current of transistors is divided into linear and nonlinear parts. This analysis calculates the output third-order nonlinear voltage created by i_{IM3} to derive the distortion cancellation condition. The second-order nonlinearity is ignored here due to its intensive attenuation as explained in Section 3.3.1.

Fig. 2(b) shows the equivalent circuit to calculate the nonlinear output voltage. The nonlinear small-signal current of each auxiliary transistor contains its intrinsic third-order intermodulation current and a nonlinear current created according to IM3 current of input transistors denoted by $i_{IM3,j}$ and $g_{mj}v_{gsj}$, respectively. According to Fig. 2(b), the nonlinear voltage of node A, $v_{A,IM3}$, due to $i_{IM3,1}$, when the input impedance is fully matched to the antenna, is obtained as

$$v_{A,IM3} = \frac{i_{IM3,1}}{1 + g_{mt1}R_S} R_S \approx \frac{i_{IM3,1}}{2} R_S \tag{10}$$

According to (10), $i_{IM3,1}$ is equally divided between the input impedance and R_S. Also the nonlinear current of M_6 and M_8 ($i_{M6,NL}$ and $i_{M8,NL}$) transistors are obtained as:

$$v_{gs6} = \frac{-i_{IM3,2}}{2g_{mt4}} = \frac{i_{IM3,1}}{2g_{mt4}} \Rightarrow i_{M6,NL} = \frac{g_{m6}}{2g_{mt4}} i_{IM3,1} + i_{IM3,6} \tag{11}$$

$$v_{gs8} = -v_{A,IM3} = \frac{-i_{IM3,1}}{2g_{mt2}} \Rightarrow i_{M8,NL} = \frac{-g_{m8}}{2g_{mt2}} i_{IM3,1} + i_{IM3,8} \tag{12}$$

Thus, the positive part of the output third-order nonlinear voltage is approximately given by:

$$v_{out+,\mathrm{IM3}} = -\left(\frac{i_{\mathrm{IM3},1}}{2}\left(1+\frac{g_{m6}}{g_{mt4}}-\frac{g_{m8}}{g_{mt2}}\right)+i_{\mathrm{IM3},6}+i_{\mathrm{IM3},8}\right)R_L \tag{13}$$

According to (13), the required condition to cancel the third-order intermodulation distortion of the input transistors (M_1 and M_2) at the output is obtained as:

$$g_{m7,8} = g_{mt1,2}\left(1+\frac{g_{m5,6}}{g_{mt3,4}}\right) \tag{14}$$

As it is seen from the relations (9) and (14), the IM2 and IM3 cancellation conditions are different. Thus, the proposed technique can cancel only one of IM2 or IM3 components at one time or reduce both of them by a proper design to improve both IIP2 and IIP3 in comparison with the traditional LNA. Also, $v_{out-,\mathrm{IM3}}$ can be calculated similarly. So, regardless to the mismatch between the corresponding transistors, $i_{\mathrm{IM3},1}$ and $i_{\mathrm{IM3},2}$ are canceled out from the output voltages ($V_{out+,\mathrm{IM3}}$ and $V_{out-,\mathrm{IM3}}$). As a result, the nonlinear output voltage is given by the following relation when the condition expressed in (14) is satisfied

$$v_{out,\mathrm{IM3}} = v_{out+,\mathrm{IM3}} - v_{out-,\mathrm{IM3}} = -2R_L\left(i_{\mathrm{IM3},6}+i_{\mathrm{IM3},8}\right) \tag{15}$$

where $i_{IM3,j}=(g''_{m,j}v_{gs,j}^3)/6$. According to (15), the third-order nonlinearity of the proposed LNA is dominated by IM3 currents of $M_{5,6}$ and $M_{7,8}$ transistors. In the proposed LNA structure, the related auxiliary transistors ($M_{5,6}$ and $M_{7,8}$) are biased in the strong and weak inversion regions, respectively, and designed properly to have an equal g''_m but with the opposite sign. As a result, the remained IM3 components of the output current eliminate each other, and hence, a significant IIP3 improvement is achieved.

3.4. Noise figure

Fig. 3 illustrates the noise contribution of the input transistors at the output. According to this figure, the channel noise of M_1 has opposite polarities at its drain and source terminals. Therefore, by an appropriate choice size of M_5 and M_7 transistors, this noise can be canceled at the output node. The noise canceling condition is derived by analyzing the circuit when the input is fully matched to the antenna. Under this condition, the noise current of M_1 is divided between R_S and the input impedance by a factor of $1/(1+g_{mt1}R_S)$. So, the output noise voltage due to the thermal noise of M_1 is given by:

$$\frac{V_{n,out,diff}}{I_{n,M_1}} = \frac{V_{n,out+}-V_{n,out-}}{I_{n,M_1}} = \frac{1}{1+g_{mt1}R_S}\left(1+\frac{g_{m5}}{g_{mt3}}-\frac{g_{m7}}{g_{mt1}}\right)R_L \tag{16}$$

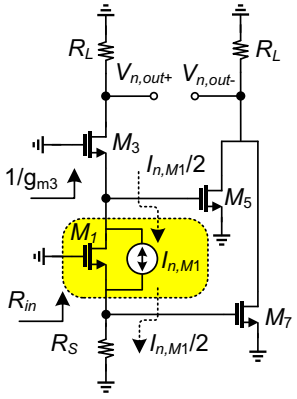

Fig. 3. Contribution of $I_{n,M1}$ at the output.

where $V_{n,out,diff}$ represents the fully-differential output noise voltage, and $I_{n,M1}$ is the thermal channel noise current of M_1. According to (16), the cancellation condition of the thermal noise of $M_{1,2}$ transistors is carried out similar to the IM3 distortion cancellation condition which is given in (14). According to the relation (14), by considering $g_{mt1,2}=g_{mt3,4}$, the noise and IM3 cancellation condition is simplified as $g_{m7,8}=g_{mt1,2}+g_{m5,6}$, which can be well satisfied by a proper design of the corresponding transistors aspect ratio. At this condition, the output noise of the proposed LNA is dominated by the noise of R_L, $M_{5,6}$ and $M_{7,8}$ transistors. The noise contribution of cascode transistors, $M_{3,4}$, is neglected because their thermal noise passes through itself since $1/g_{mt3,4}\ll R_{D1}$. Using the half-circuit of the proposed LNA shown in Fig. 4, when the simplified noise cancellation condition is satisfied, the circuit's noise factors due to the thermal noise of M_5 and M_7 transistors and load resistance, R_L, are obtained as follows:

$$F_{M_5} = \frac{\gamma}{\alpha}\frac{4kTg_{m5}}{1/4(4kT/R_S)\left(1+(g_{m5}/g_{mt3})+(g_{m7}/g_{mt1})\right)^2} = \frac{\gamma}{\alpha}\frac{g_{m5}g_{mt1}}{g_{m7}^2} \tag{17}$$

$$F_{M_7} = \frac{\gamma}{\alpha}\frac{4kTg_{m7}}{1/4(4kT/R_S)\left(1+(g_{m5}/g_{mt3})+(g_{m7}/g_{mt1})\right)^2} = \frac{\gamma}{\alpha}\frac{g_{mt1}}{g_{m7}} \tag{18}$$

$$F_{R_L} = \frac{4kT/R_L}{1/4(4kT/R_S)\left(1+(g_{m5}/g_{mt3})+(g_{m7}/g_{mt1})\right)^2} = \frac{g_{mt1}}{R_Lg_{m7}^2} \tag{19}$$

where $\alpha=g_m/g_{d0}$ and γ is the excess thermal noise coefficient in MOS transistors. Hence, the total noise factor of the proposed LNA is approximately given by:

$$F_{proposed} = 2\left(1+\frac{g_{mt1}}{g_{m7}^2}\left(\frac{\gamma}{\alpha}(g_{m5}+g_{m7})+\frac{1}{R_L}\right)\right) \tag{20}$$

According to the (20) and assuming that $g_{mt,1,2}=g_{m5,6}$, the overall NF of the proposed LNA is also simplified resulting in:

$$F_{proposed} = 2\left(1+\frac{3}{4}\frac{\gamma}{\alpha}+\frac{R_S}{4R_L}\right) \tag{21}$$

On the other hand, the simplified noise factor of the conventional differential cascode CG LNA is given by [23]:

$$F_{conv} = 2\left(1+\frac{\gamma}{\alpha}+\frac{4R_S}{R_L}\right) \tag{22}$$

An analytical comparison with the same value of device parameters shows that the proposed LNA structure reduces the noise factor about 22% compared to the conventional LNA. In this comparison, the value of components of $R_S=50\,\Omega$, $R_L=10\,\mathrm{K}\Omega$, $\gamma=2$ and $\alpha=1$ are considered.

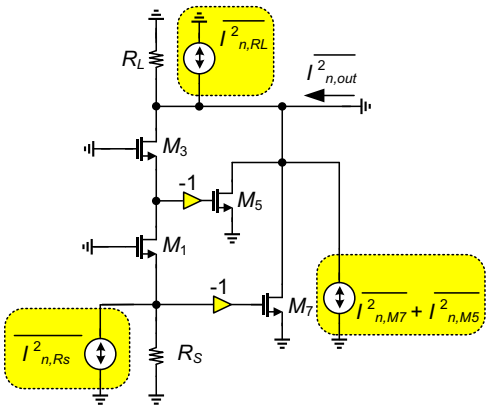

Fig. 4. Equivalent half circuit of the proposed LNA for NF calculation.

4. Simulation results

To evaluate the performance of the proposed LNA and validate the aforementioned analytical results, several simulation results are provided using a 90 nm RF-CMOS process with Spectre-RF. A differential cascode CG LNA is also designed and simulated to provide a fair comparison. The main purpose of the proposed LNA design was to improve the NF and IIP3. So, the IM2 cancellation condition is not satisfied. The device values of the simulated LNAs and the bias current of transistors are summarized in Table 1. As is seen, the input transistors of the proposed LNA have smaller bias current than the conventional one, because of using auxiliary transistors to have the similar gain. But the total output current of the proposed LNA is greater than the conventional LNA owing to auxiliary transistors which should have large bias currents to satisfy the NF and linearity improvement conditions. According to the relations (9) and (14), the transistors $M_{5,6}$ or $M_{7,8}$ consume large bias currents for IIP2 or NF and IIP3 improvements, respectively. In the design of the proposed LNA, it is preferred to have a lower NF and higher linearity at the cost of about only 1.5 mW higher power consumption compared to the conventional LNA.

Table 1
Device parameters of the proposed and conventinal LNAs.

Parameter	Proposed LNA		Conventional LNA	
	W/L	I_D (mA)	W/L	I_D (mA)
$M_{1,2}$	16 × 4.5 μm/0.2 μm	1.7	16 × 6.1 μm/0.36 μm	5.5
$M_{3,4}$	16 × 4 μm/0.2 μm	1.7	16 × 5.9 μm/0.36 μm	5.5
$M_{5,6}$	6 × 4 μm/0.1 μm	1.6	–	
$M_{7,8}$	24 × 5 μm/0.1 μm	2.9	–	
L_D	2.5 nH		12.25 nH	
L_S	5 nH		2.5 nH	
R_L	10 kΩ		10 kΩ	
R_B	10 kΩ		10 kΩ	
C_B	1 pF		1 pF	

To confirm the schematic performances of the proposed LNA and its capability for implementation, the complete layout of the proposed LNA is carried out which is illustrated in Fig. 5 and occupies 632 μm × 692 μm silicon die area. The post layout simulation results are also provided besides the schematic simulations.

To examine the stability of the proposed LNA, the pre and post layout simulated K_f and Δ over a wide frequency range is shown in Fig. 6. It shows that the Stern stability conditions ($K_f > 1$ and $\Delta = S_{11}S_{22} - S_{12}S_{21} < 1$ [21]) are provided over the whole bandwidth. Thus, although the stability of the proposed LNA can be degraded due to the Miller effect of $C_{gd7,8}$, but according to Fig. 6, the proposed LNA is unconditionally stable over the targeted bandwidth.

Fig. 7 shows the scattering parameters (S_{11} and S_{21}) of the simulated amplifiers before and after the post layout simulations. The $S_{11} < -11$ dB over 2–11 GHz bandwidth expresses that the input impedance is well matched to the antenna. The simulated power gain (S_{21}) is also shown in Fig. 7. Fig. 7(a) shows that S_{21} of the proposed LNA is about 2 dB greater than that of conventional one. Therefore, the proposed structure improves the gain as theoretically expected. Although the S_{21} and -3 dB BW of the proposed LNA reduced in the post layout simulation and it is about 9.5 dB and 8 GHz, respectively, the post layout simulation results show that the voltage gain of the core amplifier is about 12.2 which is about 3 dB higher than S_{21}. So, the proposed LNA is suitable for UWB applications.

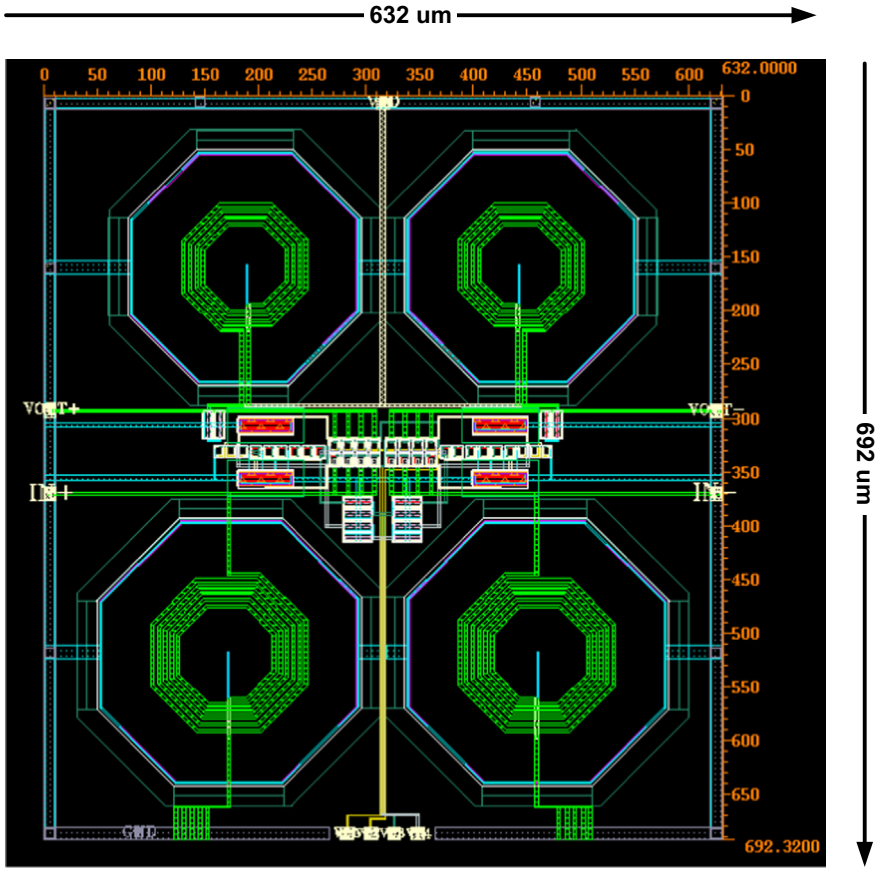

Fig. 5. Layout of the proposed LNA.

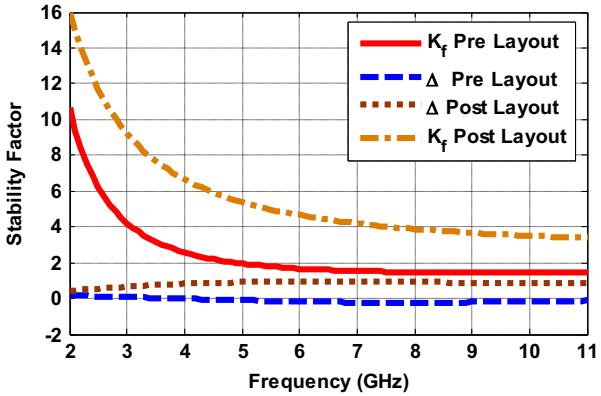

Fig. 6. Stern stability factors (K_f and Δ) of the proposed LNA.

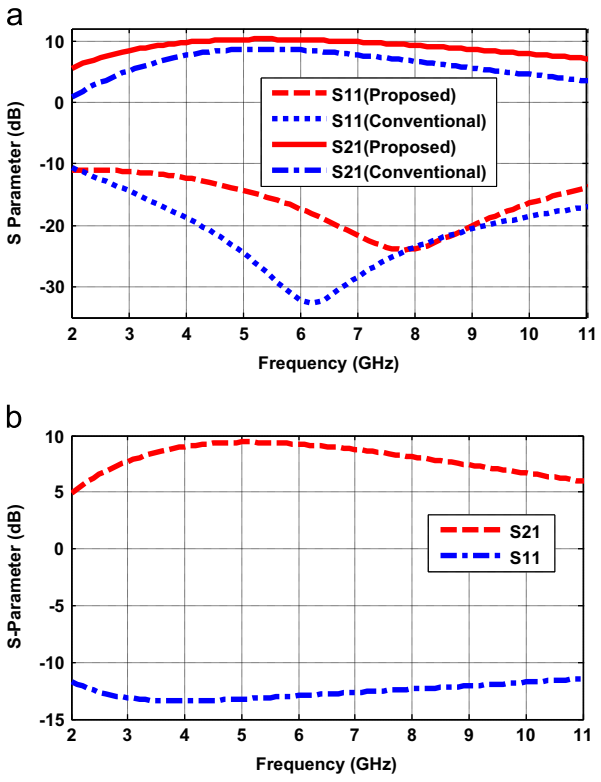

Fig. 7. S-parameters of the simulated LNAs: (a) conventional and proposed LNAs pre layout simulation and (b) proposed LNA post layout simulation.

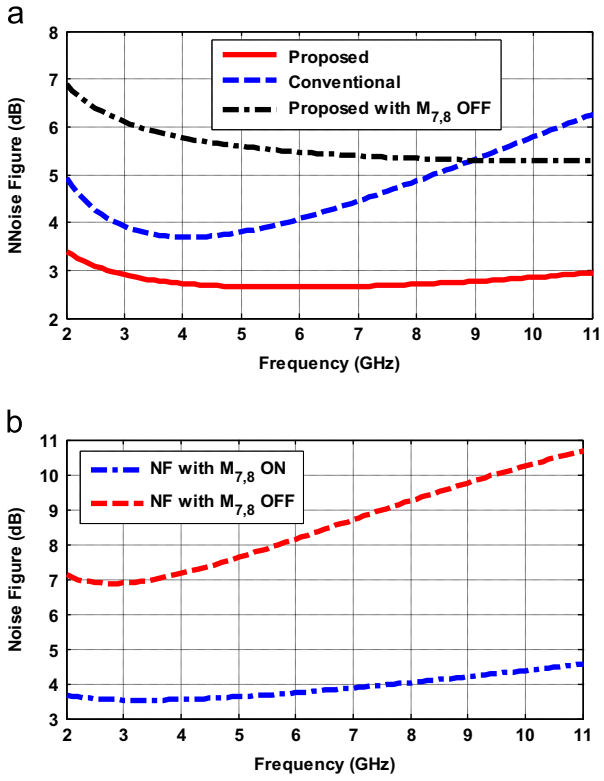

Fig. 8. NF of simulated LNAs: (a) conventional and proposed LNAs pre layout simulation and (b) proposed LNA post layout simulation.

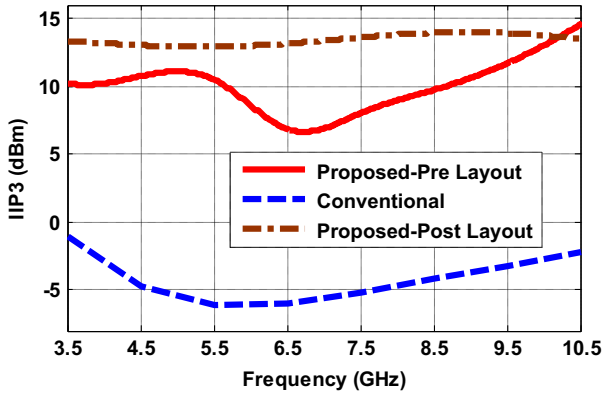

Fig. 9. IIP3 with 20 MHz two-tone spacing versus input frequency.

The pre and post layout simulated NF of the designed LNAs is shown in Fig. 8. According to Fig. 8(a), which shows the NF of schematic simulated LNAs, the proposed LNA improves the NF about 1.3 dB at the worst case. As it is seen in Fig. 8(b), the proposed LNA achieves a minimum NF about 3.5 dB over the −3 dB bandwidth after the post layout simulation. Also the efficiency of proposed structure in noise canceling is verified by turning M_7 and M_8 transistors on and off. The dash and dash-dotted lines in Fig. 8(b) shows that the NF when the noise canceling transistors are off and on, respectively. As it is clear, the NF is improved as large as 3 dB at the worst case in both pre and post layout simulations by using the noise cancellation technique. The simulation results show that the contribution of $I_{n,M1}$ and $I_{n,M2}$ in the total NF changes from 16.9% to 0.88% when M_7 and M_8 are turned on. The noise contribution of the auxiliary pair ($M_{5,6}$) and R_L are also reduced from 11.24% and 5.4% to 3.96% and 0.46%, respectively, by satisfying the noise cancellation condition. Also, the noise contribution of transistors $M_{7,8}$ in the total noise figure is about 13.6%. Thus, as mentioned before, the total noise added by M_7 and M_8 transistors is much smaller than the removed noise of $M_{1,2}$ and $M_{5,6}$ transistors from the output.

To examine the efficiency of the proposed technique on IIP3 improvement, a two-tone test at 5.5 GHz, which is the frequency of maximum gain, with 20 MHz frequency spacing is used in both simulated LNAs. According to the schematic simulation results, the average IIP3 of the proposed and conventional LNAs is about +10.4 dBm and −5.5 dBm, respectively over 8 GHz bandwidth. Also, the post layout simulation results show that the average IIP3 of the proposed LNA is about +13.1 dBm which is increased due to the gain reduction. The frequency dependency of IIP3 in pre and post layout simulations is tested by sweeping the input two tones frequency over 3–11 GHz and the results are shown in Fig. 9. Fig. 10 shows the IIP3 of the simulated LNAs at the worst case frequency (5.5 GHz) versus the two-tone frequency spacing. The dash dotted line in both Figs. 9 and 10 is the IIP3 of the proposed

LNA after the post layout simulation. According to these figures, the post layout simulation results indicate that the IIP3 of the proposed LNA is robust against the input and two-tone spacing frequency.

To test the effect of the proposed LNA structure on the second-order nonlinearity, a two-tone test at frequencies of 4.5 GHz and 4.52 GHz, which creates an IM2 term at 9.02 GHz, is performed to calculate the IIP2. To do this, an intentional 2% mismatch is considered in resistors and inductors and for transistors a random mismatch is given by the Gaussian distribution with a standard deviation ($\Delta W/W$) equal to $0.187/\sqrt{(W*L*M)}$, where W, L and M, are the width, length and number of multipliers in each transistor, respectively. A Monte-Carlo simulation is performed to show the effectiveness of the proposed IM2 cancellation technique. As shown in Fig. 11, the IIP2 of the proposed LNA is higher than 55.5 dBm while the maximum IIP2 of the conventional LNA is 33.1 dBm, which corresponds to about 22.4 dB improvement at the worst case in schematic simulation. Also, Fig. 12 shows that the minimum IIP2 of the proposed LNA is 41.3 dBm after the post layout simulation which is a great achievement for UWB applications.

The results of pre and post layout simulations for different process corner cases and temperature variations spanning from −40 °C to 85 °C are summarized in Table 2. This table shows that the performances of the proposed LNA have small variations in corner cases and consequently, the proposed LNA is robust against PVT variations.

The achieved performance of the simulated LNAs is summarized in Table 3 and the comparison with several recently reported UWB CMOS LNAs is performed using the following figure of merit (FoM) [11]:

$$FoM = \frac{S_{21}[abs] \times IIP3[mW] \times BW[GHz]}{(F-1) \times P_{dc}[mW]} \quad (23)$$

where S_{21} represents the maximum absolute power gain ($|S_{21}|$), F is the minimum noise factor over the frequency range, BW represents the −3 dB bandwidth, IIP3 denotes the average input-referred intercept point, and P_{dc} is the power consumption. As is seen, by using the proposed LNA structure an outstanding FoM is achieved compared to the previously reported UWB LNAs listed in Table 3. However, this is not a fair comparison since the results presented here are based on schematic and post layout simulations while most of the references listed in Table 3 are reporting the measured results. Nonetheless, the post-layout simulation results of the proposed LNA in different process corner cases and temperature variations and its outstanding FoM verify the efficiency of the proposed structure in the design of UWB CMOS LNAs as well.

5. Conclusions

In this paper, a UWB CMOS LNA with linearity and noise improvement techniques is presented. Two differential pairs with a cross-connected output are cascaded in the proposed structure. By canceling the common-mode part of all IM currents, both IIP3 and IIP2 of the proposed LNA are improved. According to the simulation results, average IIP3 and IIP2 are about +13.1 dB and +42.8 dB, respectively, at the worst case. Also, the proposed structure creates a noise cancellation path to reduce the overall NF.

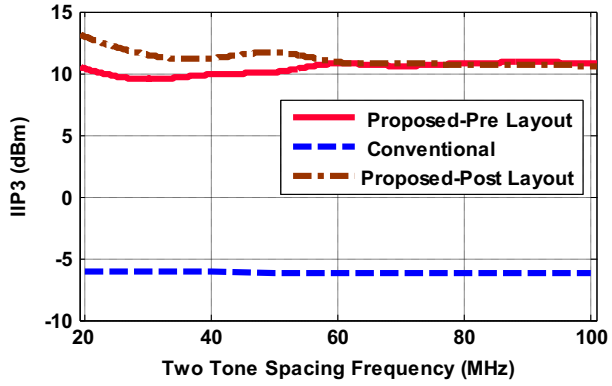

Fig. 10. IIP3 of simulated LNAs at 5.5 GHz versus two-tone frequency spacing.

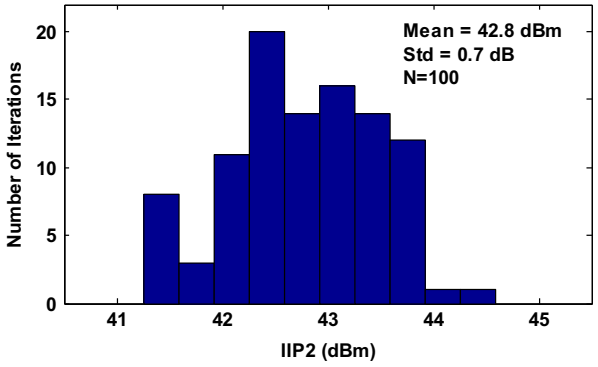

Fig. 12. Monte-Carlo post layout simulation results of IIP2 at 4.5 GHz with 20 MHz two-tone spacing.

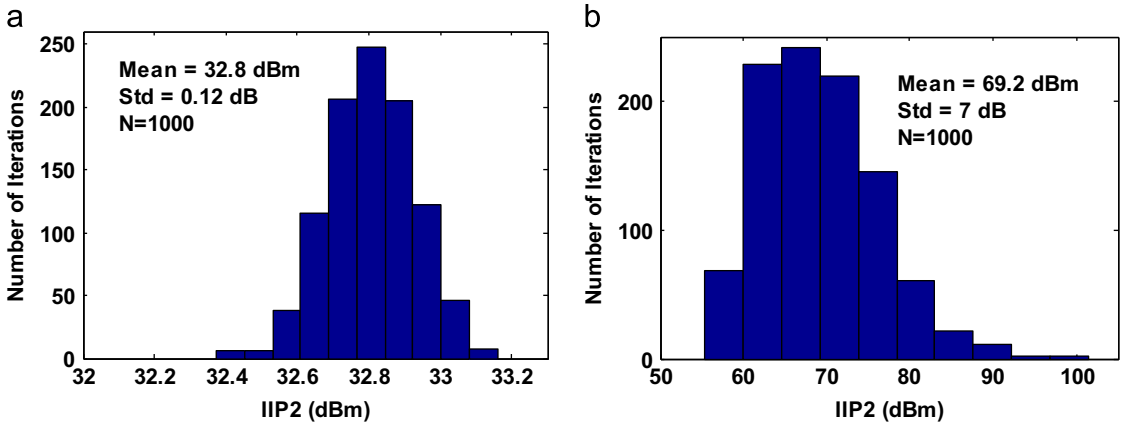

Fig. 11. Monte-Carlo pre layout simulation results of IIP2 at 4.5 GHz with 20 MHz two-tone spacing: (a) conventional LNA and (b) proposed LNA.

Table 2
Simulated performance summary of the proposed LNA in different process corner cases.

Process Corner Case	TT @ 27 °C		FF @ -40 °C		SS @ 85 °C	
	Post layout	Pre layout	Post layout	Pre layout	Post layout	Pre layout
−3 dB BW (GHz)	2.4–10.4	2.5–10.9	2.3–10.5	2.5–10.8	2.5–10	1.2–11.8
S_{11} (dB)	< −11.2	< −11	< −10.6	< −10.8	< −9.4	< −10
S_{21} (dB)	9.5	10.3	11.4	11.7	7.8	9
NF (dB)	3.5	2.6	3	1.9	4.3	3.4
IIP3 (dBm)	+13.1	+10.4	+12.5	+8.4	+13.3	+11.3
IIP2 (dBm)	+42.8	+69.2	+49.4	+67.3	+50.6	+71.3
Power (mW)	14.8	15.6	17.1	15.6	12.1	15.4

Table 3
Performance comparison of the proposed LNA with several recently reported state-of-the-art UWB CMOS LNAs.

References	CMOS Process (nm)	−3 dB BW (GHz)	S_{11} (dB)	S_{21} (dB)	NF (dB)	IIP3 (dBm)	IIP2 (dBm)	Supply (V)	Power (mW)	FoM
JSSC'07 [23]	180	1.2–11.9	< −11	9.7	4.5	−6.2	+9.7	1.8	20	0.7
JSSC'04 (STD) [24]	180	2.3–9.2	< −9.9	9.3	4	−6.7	+3	1.8	9	0.9
JSSC'04 (TW) [24]	180	2.4–9.5	< −9.4	10.4	4.2	−8.8	−4.5	1.8	9	0.7
JSSC'06 [25]	180	1.3–12.3	< −10	8.2	4.6	+9.1	–	–	4.5	69.7
IEICE Elex'08 [26] [a]	130	2.6–10.7	< −11	13.5	2.7	+5	–	1.2	13.5	49.3
CTA'09 [27]	130	2.7–8.8	< −10	12	4	+1.2	–	1.2	1.4	58.5
ISCAS'09 [28] [a]	130	4.7–11.7	< −11.9	12.4	2.9	−3	–	1.2	13.5	4.8
IEICE Elex'10 [29] [a]	180	2–6.5	< −10	11	2.7	+4.4	–	1.8	7.6	21
ISCAS'11 [30] [a]	130	2–7.6	< −10	13.8	1.9	−15.2	–	1.1	2.2	3.4
T'MTT'11 [31]	90	2.6–10.2	< −9	12.5	3	−2.4	–	1.2	7.2	10.9
Elec. Lett.'11 [32]	130	3.1–10.6	< −10	14.5	4.5	−4.8	–	1.0	7	5.5
Elec. Lett.'12 [33]	180	3.2–9.7	< −10	9.3	4.8	−7	–	1.2	4.7	1.2
Mejo.'12 [34] [a]	90	1–16.1	< −10	10.7	3.1	−3.2	–	1.2	3.2	25.3
Mejo'13 [35] [a]	180	3.1–10.6	< −10	12.6	2.9	−4.6	–	1.8	15.2	2.3
JCSC'13 [36] [a]	180	3.1–10.6	< −5.5	12.8	2.5	−8.2	–	1.2	12.1	2.3
Elec. Lett.'13 [37]	130	0.1–5	< −10	18.3	1.8	−9.5	–	1.5	14	5.2
T'MTT'13 [38]	130	2.2–12.2	< −10	13	1.9	+1	+46	1.8	7.4	61.8
JSSC'13 [39]	65	0.1–10	< −11.7	24	2.6	−13.5	+5	1.2	8.6	15.8
MWC. Lett.'14 [40]	180	1–12.5	< −10	15.2	2.2	−0.2	–	1.8	18	30.6
Mejo'14 [41]	180	2.9–12.7	< −8.5	17.8	4.8	−11.5	–	1.2	9.67	2.1
TCAS I'14 [42]	90	3.5–9.25	< −8	15	2.4	−12	–	0.8	9.6	1.6
Conventional LNA [a]	90	3.2–8.9	< −15	8.7	3.9	−5.5	+32.8	1.2	13.2	0.6
Proposed LNA[a]	90	2.4–10.4	< −11.2	9.5	3.5	+13.1	+42.8	1.2	14.8	79.4

[a] Simulation results.

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