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A 10-BIT 0.5 V 100 kS/s SAR ADC WITH A NEW RAIL-TO-RAIL COMPARATOR FOR ENERGY LIMITED APPLICATIONS*

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In this paper, a 10-bit 0.5 V 100 kS/s successive approximation register (SAR) analog-to-digital converter (ADC) with a new fully dynamic rail-to-rail comparator is presented. The proposed comparator enhances the input signal range to the rail-to-rail mode, and hence, improves the signal-to-noise ratio (SNR) of the ADC in low supply voltages. The effect of the latch offset voltage is reduced by providing a higher voltage gain in the regenerative latch. To reduce the ADC power consumption further, the binary-weighted capacitive array with an attenuation capacitor (BWA) is employed as the digital-to-analog converter (DAC) in this design. The ADC is designed and simulated in a 90 nm CMOS process with a single 0.5 V power supply. Spectre simulation results show that the average power consumption of the proposed ADC is about 400 nW and the peak signal-to-noise plus distortion ratio (SNDR) is 56 dB. By considering 10% increase in total ADC power consumption due to the parasitics and a loss of 0.22 LSB in ENOB due to the DAC capacitors mismatch, the achieved figure of merit (FoM) is 11.4 fJ/conversion-step.

Keywords: Successive approximation register (SAR); SAR analog-to-digital converters; rail-to-rail CMOS comparators; nanometer CMOS technologies.

1. Introduction

In order to increase the operating life of the devices used in energy limited applications such as the implantable medical devices, portable instruments, and energy harvesting systems, the power dissipation of the utilized mixed-signal systems has to be optimized.[1–8] The analog-to-digital converter (ADC) is one of the essential

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components in signal processing systems inherently consuming a large amount of the total power. Therefore, low-power ADCs are of high popularity for such applications.

On the other hand, since the transistors channel length continue to scale down in sub-micron CMOS processes, the leakage current increases and the intrinsic gain of the transistors is insufficient. As a result, the efficiency due to the technology scaling is degraded.[5,6] Moreover, the threshold and supply voltages do not scale at the same pace in advanced CMOS technologies and this poses several challenges in analog sub 1-V circuit design. In comparison with other ADC architectures, successive approximation register (SAR) ADCs employ minimal analog building blocks. This results in lower power consumption. Furthermore, the negative effects of using the sub-micron CMOS technologies on the overall ADC performance are limited.

From the above, it can be concluded that SAR ADCs are the most suitable choice for low power applications such as the battery operated and implantable devices. Several solutions have been proposed to operate the analog circuits using a low supply voltage such as the voltage boosting,[5,6] using low threshold voltage devices[3] and design in the sub-threshold region.[7] However, the voltage boosting technique increases the risk of gate oxide breakdown in nanometer CMOS technologies. Using low threshold voltage devices increases the process complexity and requires additional masks resulting in higher fabrication costs. The circuit design in sub-threshold regime is limited to lower frequency applications.

This paper presents a 10-bit 0.5 V 100 kS/s SAR ADC by employing a new fully dynamic rail-to-rail comparator to achieve the full-scale input swing with nanowatt power consumption. The rest of the paper is organized as follows. Section 2 presents the proposed rail-to-rail CMOS comparator. Design considerations of the realized ADC are explained in Sec. 3. Section 4 presents the ADC simulation results. Finally, Sec. 5 concludes the paper.

2. Proposed Rail-to-Rail Comparator

Although, the low supply voltage reduces the power dissipation of the SAR ADC, it inherently limits the maximum input signal swing and this results in low peak signal-to noise ratio (SNR). By considering only the thermal noise of the front-end sample and hold (S/H) circuit and the capacitor array, the value of the peak SNR for the binary-weighted capacitive array with an attenuation capacitor (BWA) is given by[8]:

$$\mathrm{SNR}_{\max} = \left(8kT \times \left[4 + 2^{(1-0.5N)} - 2^{-1.5N}\right] \times \left[2 - 2^{(1-N)}\right]\right)^{-1} C_u V_{\mathrm{in}}^2 , \qquad (1)$$

where V_{in} is the peak-to-peak of the sinusoidal input voltage. C_u and k denotes the DAC unit capacitor and the Boltzmann constant, respectively. T is the temperature in Kelvin and N defines the ADC resolution with $N \geq 2$. To overcome the poor peak SNR issue, a larger C_u and/or a rail-to-rail input voltage swing is needed. Since both the silicon die area and the DAC switching power dissipation increase with a large C_u, employing a rail-to-rail comparator is a good approach in low voltage supply designs.

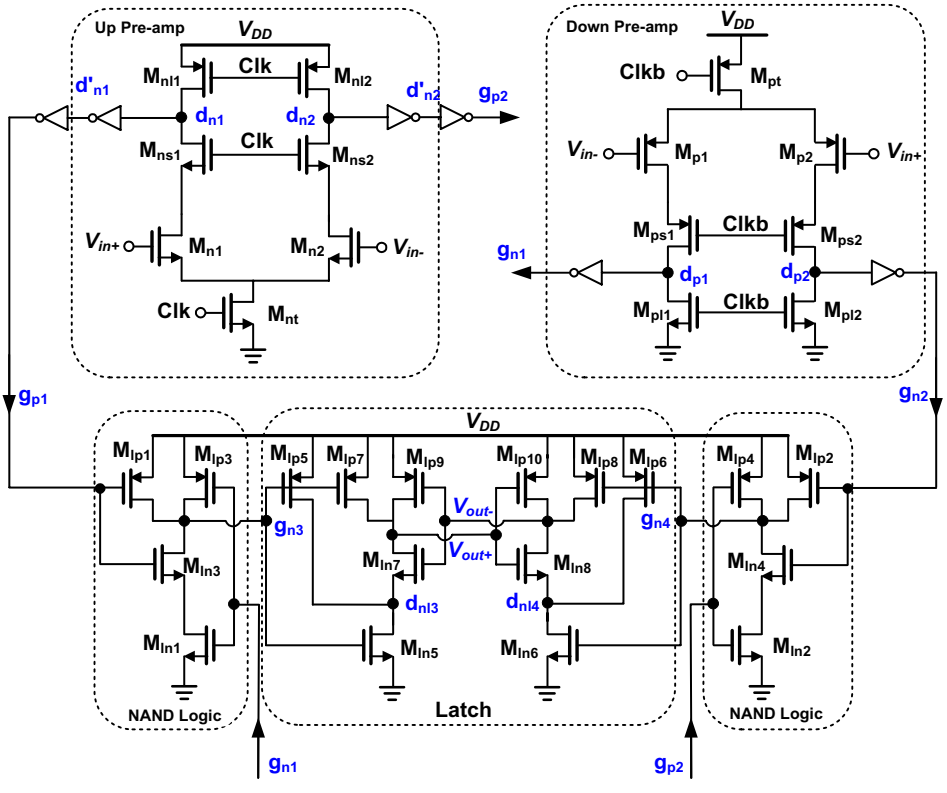

Fig. 1. Proposed rail-to-rail CMOS comparator.

Figure 1 shows the proposed fully dynamic rail-to-rail CMOS comparator comprising of two pre-amplifiers and a latch stage. The basic structure of the proposed comparator originates from the comparators introduced in Refs. 10 and 14. In order to extend the input common-mode range to the rail-to-rail, the pMOS and nMOS differential pairs ($M_{p1,2}$, $M_{n1,2}$) are connected in parallel to serve as the pre-amplifiers. Also transistors $M_{ln1,2,3,4}$ and $M_{lp1,2,3,4}$ act as two NAND logics to reduce the offset voltage of the latch partially.

The operation of the proposed comparator is similar to that is reported in Ref. 10. During the reset phase (when clk is low), both $M_{nl1,2}$ and $M_{pl1,2}$ transistors are turned on, and hence, the parasitic capacitances at nodes d_{n1} and d_{n2} are charged to V_{DD} whereas the parasitic capacitances at nodes d_{p1} and d_{p2} are discharged to the ground. Therefore, the nodes $g_{n1,2}$ and $g_{p1,2}$ are charged to V_{DD} due to the inverters. Due to the NAND logics, the output signals of the inverters are combined together making the nodes g_{n3} and g_{n4} to discharge to the ground. Thereafter, transistors $M_{lp7,8}$ are turned on making $V_{\text{out}+}$ and $V_{\text{out}-}$ nodes to be charged to V_{DD}. When clk goes high, the evaluation phase is started, and hence, the parasitic capacitances at nodes d_{n1}

and d_{n2} are discharged in different rates depending on the magnitude of the input voltage. On the other hand, the parasitic capacitances at nodes d_{p1} and d_{p2} are charged at different rates. Furthermore, an input dependent differential voltage is formed between the output nodes of each pre-amplifier ($d_{n1,2}$ and $d_{p1,2}$) making the inverters to turn on at different times, and as a result, the input voltage difference, ΔV_{in}, is converted to the time and/or phase differences. The inverters act as amplifiers in order to regenerate the signal at nodes $d_{n1,2}$ and $d_{p1,2}$. Also, they reduce the input-referred offset voltage of the output latch stage. The amplified signals with different time intervals are applied to the output latch stage and due to the positive feedback; the cross-coupled inverters force one of the output nodes to the ground and the other one to V_{DD}.

The proposed comparator was simulated in a 90 nm standard CMOS process. Spectre-RF simulations show that this comparator can resolve the input signal differences as low as 5 μV. The result of an overdrive recovery test for a 20 MHz clock frequency and 5 μV input signal difference is shown in Fig. 2.

In addition to the advantages of the comparator introduced in Ref. 10, the proposed comparator has a rail-to-rail input voltage swing and lower kick-back noise due to the stacked $M_{ns1,2}$ and $M_{ps1,2}$ transistors. However, the maximum speed of this comparator is equal to 1 GHz which is lower than the comparator of Ref. 10. This is due to the lower supply voltage and increased parasitic capacitances of the circuit.

Assuming the voltage of 1 least significant bit (LSB) to be 60 μV, the worst case delay of the simulated comparator is less than 0.64 ns. In order to measure the input-referred offset voltage, a random mismatch with the Gaussian distribution is applied to the threshold voltage V_{TH} and current factor β ($\mu C_{\text{ox}} W/L$) of each transistor pair.

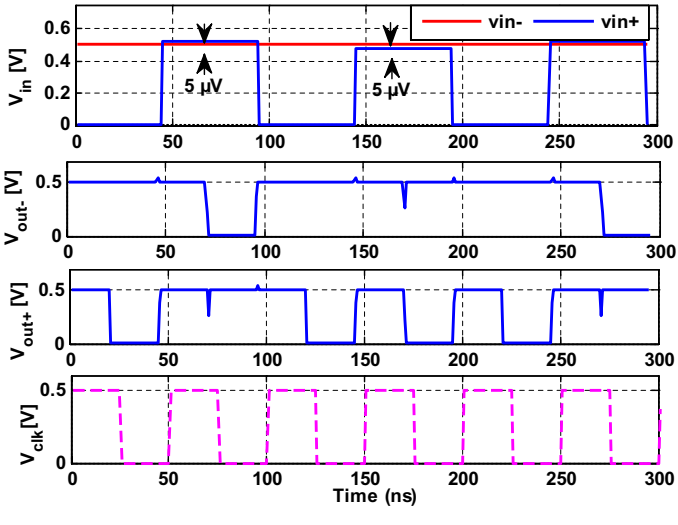

Fig. 2. Overdrive recovery test for a 5 μV input signal difference.

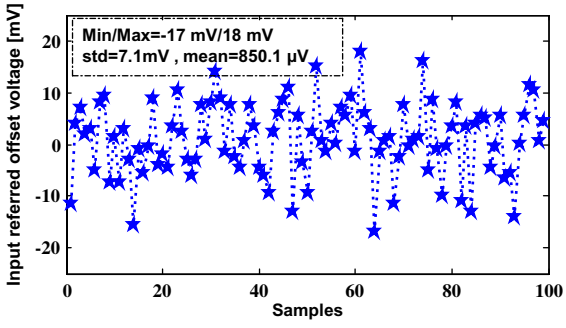

Fig. 3. Simulation result of the equivalent input-referred offset voltage (TT @ 27°C).

The random mismatch is modeled as follows[11]:

$$\sigma_{V_{\mathrm{TH}}} = \frac{A_{V_{\mathrm{TH}}}}{\sqrt{WL}}, \quad \sigma_{\beta} = \frac{A_{\beta}}{\sqrt{WL}}\,. \tag{2}$$

Since the parameters $A_{V_{\mathrm{TH}}}$ and A_{β} are process dependent, in this simulation, their values are assumed to be $3\,\mathrm{mV}\times\mu\mathrm{m}$ and $1\%\,\mu\mathrm{m}$, respectively. Therefore, with these assumptions, a slowly varying ramp signal was applied to the comparator input and a Monte-Carlo transient simulation with 100 iterations was performed. The equivalent input-referred offset voltage and the related histogram are illustrated in Figs. 3 and 4, respectively.

As shown in Fig. 3, the standard deviation ($\sigma_{V\mathrm{off}}$) of the comparator offset voltage is about 7.1 mV while the mean offset voltage is about 851 μV. The offset voltage of the comparator may affect the accuracy. It degrades the SNR by reducing the input signal range. Therefore, considering 3σ and mean offset of 851 μV, the total offset voltage of the simulated comparator is about 22 mV, which degrades the SNR by

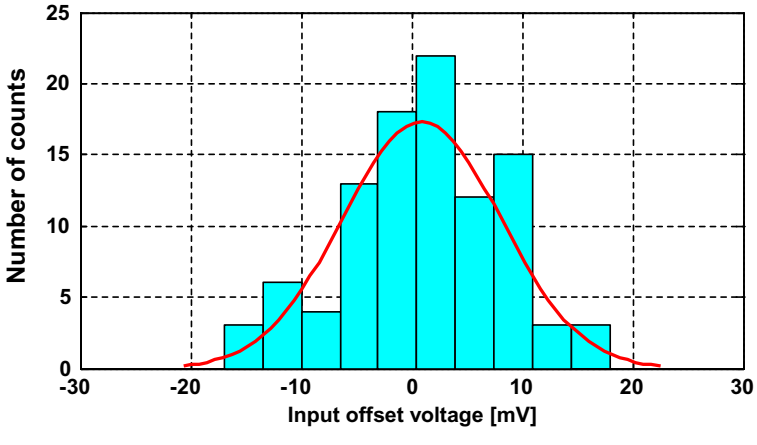

Fig. 4. Histogram of the equivalent input-referred offset voltage (TT @ 27°C).

0.39 dB. As a result, this SNR degradation leads to a loss of 0.065-LSB. The total offset voltage is comprised of the offset voltage of differential input pairs, inverters, NAND logics, and the latch stage. The offset voltage of the latch stage ($V_{\text{off,latch}}$) when referred to the comparator input is given by:

$$V_{\text{os,referred}} = \frac{V_{\text{off,latch}}}{G_n + G_p}\,, \tag{3}$$

where $V_{\text{os,referred}}$ is the equivalent input-referred offset voltage of the latch. G_n is the total voltage gain between $d_{nl3,4}$ nodes and the gate of nMOS differential pairs, and G_p is the total voltage gain between $d_{nl3,4}$ nodes and the gate of pMOS differential pairs. Since G_n and G_p are large enough, the effect of $V_{\text{os,referred}}$ on the overall input offset voltage is negligible. The offset voltage of the other components are divided by the related voltage gains and referred to the comparator input.

The dynamic voltage gain between each stage at the beginning of the evaluation phase for 1 LSB input signal difference is shown in Fig. 5. Figure 5 briefly indicates that primary stages have significant effect in the total input-referred offset voltage, such that the input differential pairs ($M_{p1,2}$, $M_{n1,2}$) have the highest contribution to the input offset voltage. The dominant factor in offset voltage of differential input pairs is their threshold voltage mismatch which can be reduced by increasing the transistor sizes.[10] However, the input parasitic capacitance is increased which may

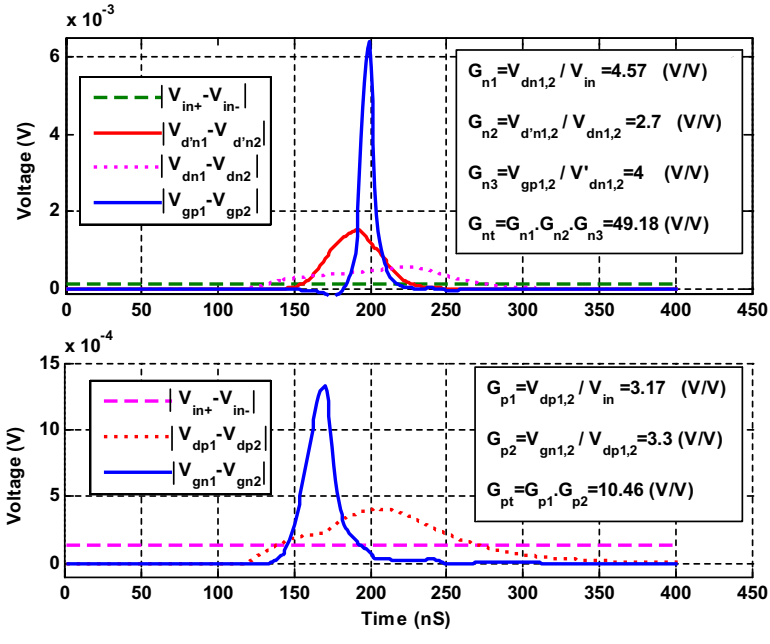

Fig. 5. Absolute values of the voltage differences between each stage at the beginning of the evaluation phase.

Table 1. Simulation results of the proposed rail-to-rail comparator.

Parameters	TT @ 27°C	FF @ − 40°C	SS @ 85°C
Power supply voltage (V)	0.5	0.5	0.5
Clock frequency (MHz)	20	20	20
Power dissipation (nW)	730	793	670
Worst case delay (ns)	0.63	0.41	1.07
Resolution (μV)	5	5	5
Kick-back noise (mV)	3–8	2–8	3–6
Input-referred offset voltage σ_{Voff} (mV)	7.1	5.3	7.7
Process		90 nm CMOS	

affect the accuracy of the DAC. Table 1 summarizes the detailed simulation results of the proposed comparator in different process corner cases and temperature variations.

3. Design of SAR ADC

Since the fully-differential circuit structure consumes more power, the single-ended architecture is chosen in this design. However, the fully-differential architecture provides better common-mode rejection and less distortion.[1] The schematic diagram of the simulated SAR ADC is shown in Fig. 6. The main components of the SAR ADC are the digital-to-analog converter (DAC), S/H circuit, comparator, and the SAR. In this section, the design of ADC building blocks is described.

3.1. *Capacitor array and S/H circuit*

As shown in Fig. 6, in order to reduce the DAC switching power dissipation, the BWA[16] has been employed in the simulated SAR ADC. In addition to low power consumption, the BWA architecture reduces the size of the total capacitance,

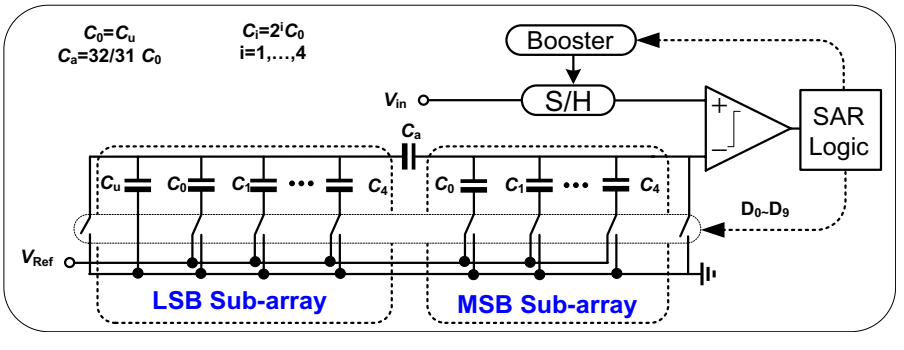

Fig. 6. Schematic diagram of the simulated SAR ADC.

although it is sensitive to the mismatch and parasitic capacitances.[16] The DAC capacitors should have sufficient matching to meet the desired ADC accuracy. The effect of the capacitance mismatch on the ADC accuracy for the BWA structure has been investigated in Refs. 17 and 18. Due to the attenuator capacitor, the capacitance mismatch effect of the LSB capacitors is reduced by 1/32 in this design. Therefore, the matching requirement of the MSB capacitors will be dominant. The unit capacitor value is determined by considering the capacitors matching, kT/C noise, and technology design rules. In this design, the matching requirement is dominant. The minimum value of the unit capacitor to meet the matching requirement is determined by the maximum standard deviation of differential nonlinearity (DNL) error. The maximum standard deviation of DNL and integral nonlinearity (INL) errors for the BWA architecture with an attenuation capacitor can be approximated as[17]:

$$\sigma_{\mathrm{DNL,max}} \approx \sqrt{2^{3\frac{N}{2}}}\left(\frac{\sigma_u}{C_u}\right)\mathrm{LSB}\,, \tag{4}$$

$$\sigma_{\mathrm{INL,max}} \approx \sqrt{2^{3\frac{N}{2}} \times \frac{V_{\mathrm{in}}}{V_{\mathrm{Ref}}}}\left(\frac{\sigma_u}{C_u}\right)\mathrm{LSB}\,, \tag{5}$$

where N is the desired resolution of the ADC, C_u and σ_u are the nominal value and the standard deviation of the unit capacitor, respectively. In this design, the metal-insulator-metal (MIM) capacitors are used to implement the capacitor array. In order to guarantee that the matching requirement is satisfied and no missing code to be occur in the ADC digital output, the $3\sigma_{\mathrm{DNL,max}}$ must be less than 0.5 LSB. In the used technology to have 10-bit matching, the maximum value of σ_u/C_u should be 0.09%. Note that in relation (5), V_{in} is equal to V_{REF}, due to the rail-to-rail input signal range. Also, the standard deviation of the capacitor mismatch, $\sigma(\Delta C/C)$, is $\sqrt{2}$ times of σ_u/C_u.[2] Consequently, the value of $\sigma(\Delta C/C)$ is obtained as 0.13% corresponding to a 110 fF capacitance. Therefore, to have a better matching, the value of C_u is chosen as 120 fF.

Since the input signal sampling is not performed by the capacitive DAC, simple inverters are used to connect the bottom plates of the DAC capacitors to the power rails. The S/H circuit of the ADC is comprised of a sampling switch and a holding capacitor. To achieve a wide bandwidth in the S/H circuit, the sampling switch must have a small on-resistance. Due to the lower supply voltage (0.5 V) in this design, these switches may have very poor on-resistance which degrades the S/H circuit settling and linearity performance. The clock feed-through and charge injection are the other factors distorting the sampled input signal. So, the sampling switch was implemented using a CMOS transmission gate and to mitigate the poor on-resistance problem, the gate of the nMOS transistor is driven by a voltage boosting circuit[19] which is shown in Fig. 7.

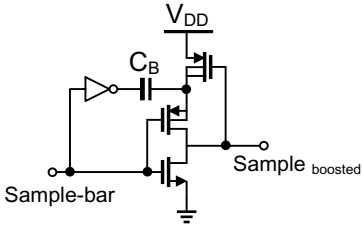

Fig. 7. Voltage boosting circuit.[19]

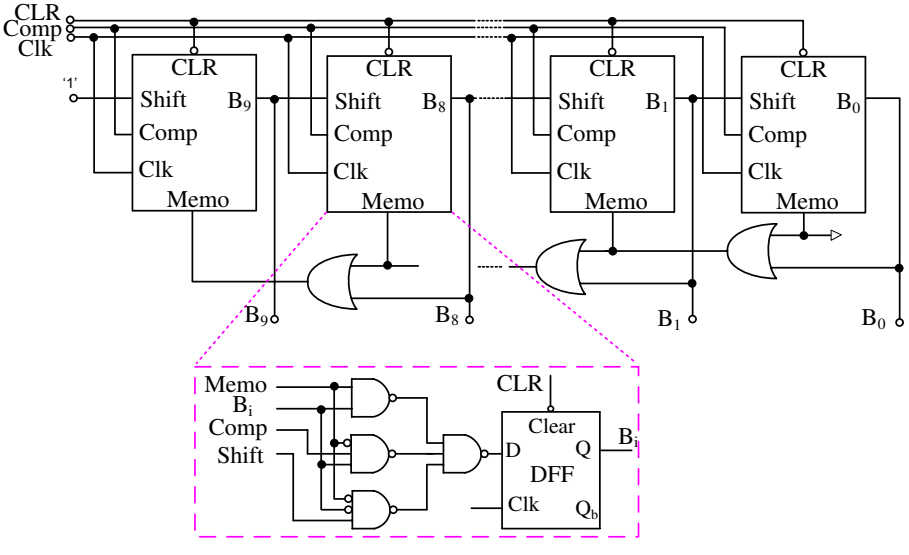

Fig. 8. SAR control logic.[20]

3.2. *SAR control logic*

The controlling signals of the comparator, S/H circuit, and the DAC switches are generated in the SAR control logic based on the successive approximation algorithm. The non-redundant structure[20] is used to generate the necessary controlling signals. The schematic diagram of the 10-bit SAR control logic is illustrated in Fig. 8 which is comprised of 10 multiple input shift registers. Each shift register comprises of a decoder-multiplexer and a D flip-flop where all were implemented with NAND gates.

4. Simulation Results

A 10-bit 0.5 V 100 kS/s SAR ADC based on the proposed comparator is designed and simulated in a 90 nm CMOS process. Spectre-RF simulations show that the average power consumption of the proposed ADC is about 400 nW from a 0.5 V single power

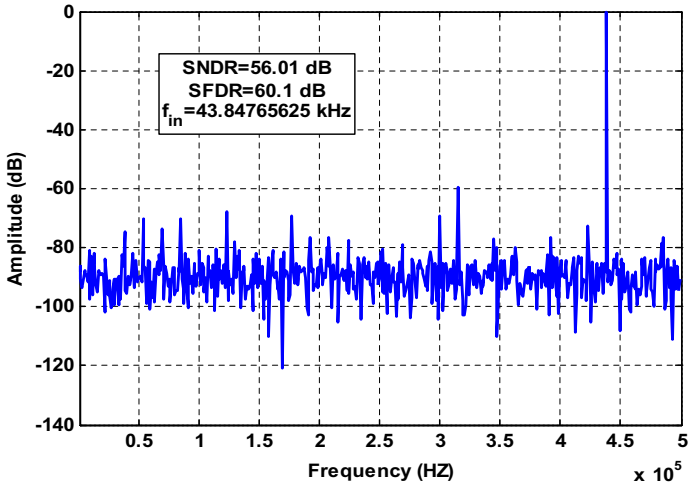

Fig. 9. Output spectrum of the simulated SAR ADC excluding the circuit noise.

supply and the peak SNDR is 56 dB without considering the effect of RC parasitics and the DAC capacitors mismatch. To calculate the SNDR, 1024 data points were used in the fast Fourier transform (FFT) analysis. The output spectrum of the simulated ADC for a rail-to-rail 43.84765625 kHz sine-wave input and 100 kS/s sampling rate is shown in Fig. 9. The simulated SNDR versus the input signal frequency is shown in Fig. 10. As is seen, the SNDR is almost constant in the Nyquist bandwidth and a good effective resolution bandwidth (ERBW) is achieved. In these simulations, the circuit noise was not considered. But, the kT/C noise of the DAC capacitive array and the S/H circuit was calculated according to Ref. 8, and the overall kT/C noise at the input of the ADC yields a mean-square value of about

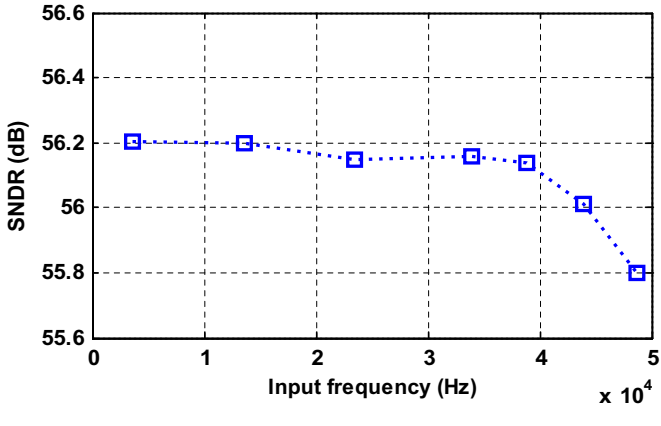

Fig. 10. The simulated ADC SNDR versus the input signal frequency.

Table 2. Performance summary of the simulated SAR ADC excluding the RC parasitics and DAC capacitors mismatch.

Parameter	TT @ 27°C	FF @ −40°C	SS @ 85°C
Resolution		10 bit	
Sampling rate		100 kHz	
Supply voltage		0.5 V	
Input voltage range		rail-to-rail	
Process		90 nm CMOS	
SNDR@ $f_{in} = 43.84765625$ kHz	56.01 dB	55.19 dB	55.58 dB
SFDR	60.1 dB	58.81 dB	59.62 dB
ADC power dissipation			
Comparator	116 nW	159 nW	102 nW
DAC	178 nW	257 nW	121.2 nW
Digital	106 nW	142 nW	98 nW
Total power consumption	400 nW	558 nW	321.2 nW
FoM	8.9 fJ/c-s	13.6 fJ/c-s	7.5 fJ/c-s

$6.5\times10^{-9}\text{V}^2$. Therefore, it has a negligible effect on the overall SNDR. The details of the simulated ADC performance in different process corner cases and temperature variations is summarized in Table 2.

The following figure-of-merit (FoM) is used to compare the simulated ADC performance with the state-of-the-art SAR ADCs:

$$\text{FoM} = \frac{\text{Power}}{\min\{f_s, 2 \times f_{in}\} \times 2^{\text{ENOB}}} . \tag{6}$$

In order to have a realistic FoM, the effect of RC parasitics on the ADC performance should be considered. Although the estimation of the RC parasitics of ADC building blocks is difficult without having a layout design, but from the reported relations in Refs. 17 and 18, another relation is derived to estimate the effect of the parasitic capacitances of the DAC on the power consumption. Explicit details and calculations are provided in Appendix A.

Table 3 provides a comparison of this work with the current state-of-the-art low power SAR ADCs. Note that, the reported FoM in Table 3 is obtained by assuming 10% increase in the total ADC power consumption due to the RC parasitics. Also, in spite of the unit capacitor is chosen large enough, to consider the DAC capacitors mismatch effect on the ADC SNDR, it was modeled in Simulink and a Monte-Carlo simulation with 200 iterations was performed and the result is shown in Fig. 11. According to the calculations in Sec. 3.1, in this simulation, the standard deviation of each capacitor is assumed as 0.13%. As shown in Fig. 11, the worst case SNDR is 60.13 dB whereas the ideal counterpart is 61.47 dB. In other words, the DAC capacitors mismatch leads to an increase of $32.3\times10^{-9}\text{V}^2$ in the power of the quantization noise (about 36%). So by considering 36% increase in the quantization noise power, the achieved SNDR from the circuit-level simulations is 54.67 dB.

Table 3. Performance comparison of the simulated ADC with several recently reported low-power SAR ADCs.

References	Process	Resolution	Sampling rate	Supply	Input range	Power consumption	SNDR	FoM
JSSC'07[1]	0.18 μm	8 bit	200 kS/s	0.9 V	Rail-to-rail	2.47 μW	47.4 dB	65 fJ/c-s
JSSC'12[2]	0.13 μm	10 bit	1 kS/s	0.4 V, 1V	1 Vp-p	53 nW	57 dB	94.5 fJ/c-s
JSSC'11[4]	0.18 μm	10 bit	100 kS/s	0.6 V	Rail-to-rail	1.3 μW	57.7 dB	21 fJ/c-s
ISSCC'11[13]	65 nm	10 bit	20 kS/s	0.55 V	—	206 nW	55 dB	22.4 fJ/c-s
BioCAS'11[5,a]	0.5 μm	10 bit	100 kS/s	1.2 V	0.7 V	12 μW	58.9 dB	166.3 fJ/c-s
ISCAS'09[9,a]	0.13 μm	10 bit	100 kS/s	1 V	1 Vp-p	1 μW	57 dB	17 fJ/c-s
ISCAS'11[12,a]	90 nm	10 bit	1 MS/s	1 V	1 Vp-p	7 μW	57.14 dB	11.9 fJ/c-s
ESSCIRC'11[15]	0.25 μm	8 bit	31.25 kS/s	0.5 V	Rail-to-rail	87.41 nW	45.14 dB	20 fJ/c-s
CTA'12[18]	0.35 μm	10 bit	2 kS/s	1 V	Rail-to-rail	130 nW	58.4 dB	96 fJ/c-s
ISCAS'12[21,a,b]	0.18 μm	8 bit	16 kS/s	1.2 V	—	450 nW	49.9 dB	132 fJ/c-s
JCSC'11[22,a,b]	0.18 μm	8 bit	1.23 MS/s	1.2 V	25.6 μA	73.19 μW	46.23 dB	357 fJ/c-s
NEWCAS'12[23,a]	0.18 μm	9 bit	25 kS/s	1 V	—	160 nW	53 dB	17 fJ/c-s
MWSCAS'12[24,a]	0.18 μm	11 bit	200 kS/s	1.2 V	—	6.7 μW	67.6 dB	18.8 fJ/c-s
This work[a]	90 nm	10 bit	100 kS/s	0.5 V	Rail-to-rail	440 nW	54.67 dB	11.36 fJ/c-s

[a]Simulation results.
[b]Current mode.

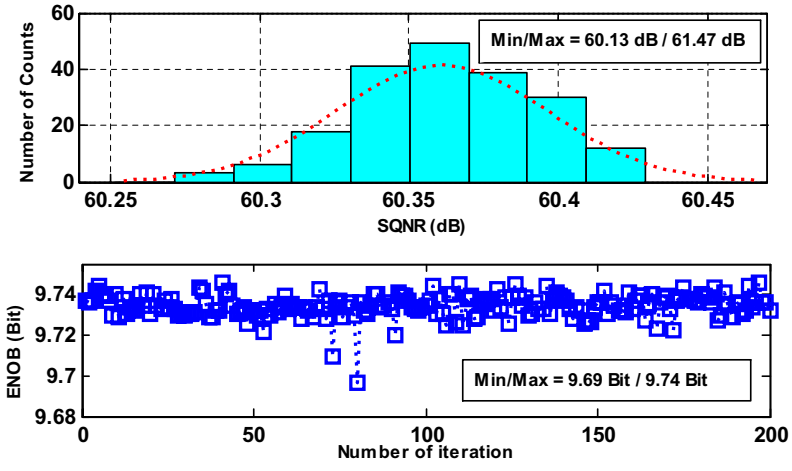

Fig. 11. Behavioral Monte-Carlo simulation of (a) SNDR and (b) ENOB by considering the DAC capacitors mismatch.

As is seen from Table 3, by using the proposed rail-to-rail comparator, a better FoM is achieved with 0.5 V power supply in 90 nm CMOS. It should be noted that although the reported results for the presented SAR ADC are based on Cadence simulation results while most of the other ADCs are implemented on chip, but its outstanding FoM verifies its performance as a good candidate for low power SAR ADCs.

5. Conclusion

In this paper, a 10-bit low power SAR ADC targeted for energy limited applications was designed and simulated. In order to extend the common-mode input signal range and achieve a better SNR in 0.5 V power supply, a new rail-to-rail CMOS comparator was proposed. To reduce the power dissipation of the capacitive DAC, the BWA[16] was employed in this design. The designed SAR ADC achieves a FoM of 11.4 fJ/conversion-step.

Acknowledgment

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Appendix A

Since the DAC capacitor array occupies the most area of the ADC, the effect of its parasitics is investigated here. The power consumed from the reference voltage due to the DAC parasitic capacitances has been estimated in Ref. 17. As shown in Fig. A.1, we modeled the total parasitic capacitance at the MSB sub-array with $C_{\mathrm{PM,total}}$; which consists of the entire top-plate parasitic capacitances of the MSB sub-array capacitors, the input parasitic capacitor of the comparator, the top-plate parasitic

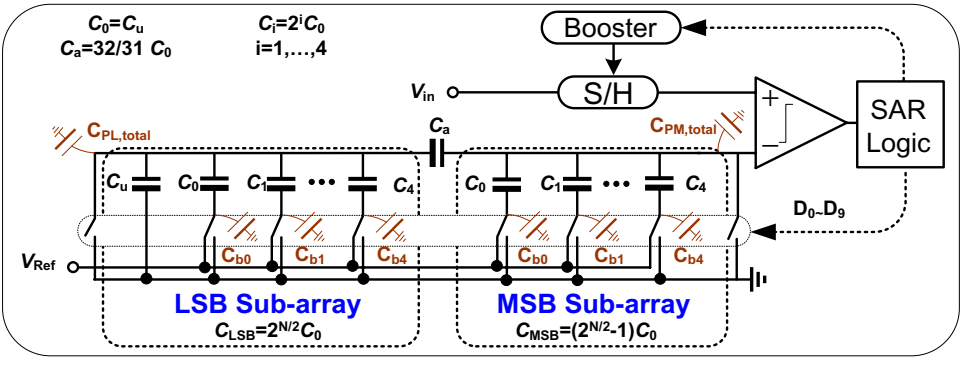


Fig. A.1. Parasitic capacitances in the DAC capacitor array.

capacitance of the attenuation capacitor, and the parasitic capacitors due to the routing metals. Similarly, the total parasitic capacitance at the LSB sub-array is modeled by $C_{\mathrm{PL,total}}$ consisting of the entire top-plate parasitic capacitances of the LSB sub-array capacitors, the bottom-plate parasitic capacitance of the attenuation capacitor, and the parasitic capacitors due to the routing metals. Also, the bottom-plate parasitic capacitance of the main capacitors, the switches, and routing parasitic capacitances are modeled by C_{bi}.

A. *Effect of top-plate parasitic capacitances on the power consumption*

As mentioned in Ref. 17, it can be shown that the power dissipation due to the top-plate parasitic capacitance is negligible. Note that the relation (26) in Ref. 17 is calculated for the conventional binary-weighted structure which should be derived for the BWA structure here. To estimate the power consumed by top-plate parasitic capacitances, we assume that the $C_{\mathrm{PM,total}}$ is equal to $C_{\mathrm{PL,toal}}$, and hence, both of them have the same power dissipation. Therefore, only the effect of $C_{\mathrm{PM,total}}$ on the power dissipation is calculated. Since the LSB sub-array capacitors is much bigger than $C_{\mathrm{PL,total}}$, the equivalent capacitance of the series combination of C_a and the total LSB sub-array capacitors is approximately equal to the unit capacitor.

Thus, the power consumption of $C_{\mathrm{PM,total}}$ can be approximated by the following relation which is similar to the relation (26) given in Ref. 17:

$$\begin{aligned} P_{\text{parasitic-top}} &\approx \frac{2^{\frac{N}{2}} f_{\mathrm{clk}} C_0}{N+1} \left(\frac{C_{\mathrm{PM,total}}}{2^{\frac{N}{2}} C_0}\right) \\ &\quad \times \left\{ \left(\frac{1}{6} + \frac{1}{3}\left(\frac{1}{2}\right)^N\right) V_{\mathrm{ref}}^2 + \frac{1}{6} V_{\mathrm{in}}^2 + \left(\frac{1}{2}\right)^{\frac{N}{2}} V_{\mathrm{in}} V_{\mathrm{ref}} \right\}, \\ &\approx \frac{f_{\mathrm{clk}} C_{\mathrm{PM,total}}}{N+1} \times \frac{1}{6}(V_{\mathrm{ref}}^2 + V_{\mathrm{in}}^2) \end{aligned} \tag{A.1}$$

where $V_{\text{in}} = \sum_{i=1}^{N}(\frac{D_i V_{\text{ref}}}{2^i})$ is the equivalent analog voltage of the corresponding digital word. By assuming D_i =1, the relation (A.1) is simplified as:

$$P_{\text{parasitic-top}} \approx \frac{f_{\text{clk}} C_{\text{PM,total}}}{N+1} \times \frac{1}{3} V_{\text{ref}}^2 . \tag{A.2}$$

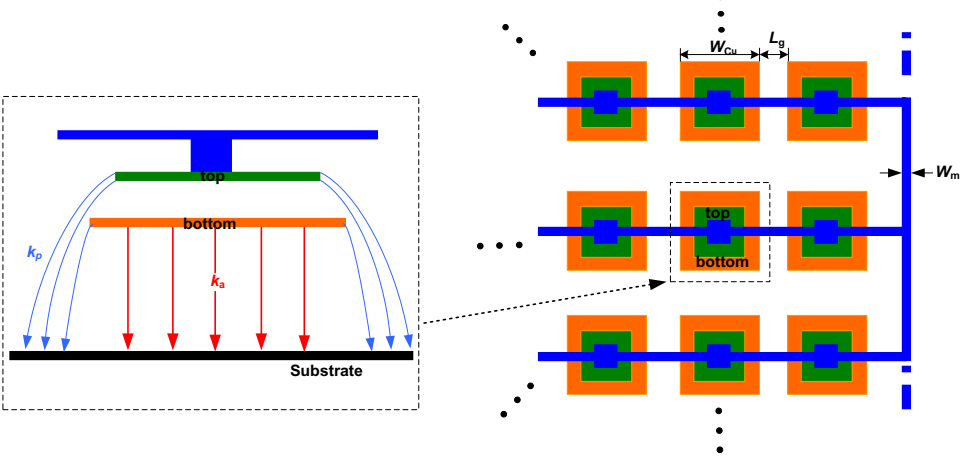
In the layout, the upper metal layers of the process are used for the capacitors. So, the value of the top-plate parasitic capacitors is small and only the power consumption of the bottom-plate parasitic capacitances will be dominant. Anyway, as mentioned in Ref. 18 the value of the $C_{\text{PM,total}}$ can be approximated as:

$$C_{\text{PM,total}} \approx 2^{\frac{N}{2}} C_{\text{pu,top}} + C_{\text{p,rout}} + C_{\text{p,comp}} , \tag{A.3}$$

where $C_{\text{pu,top}}$ is the top-plate parasitic capacitance of the unit capacitor to the substrate. $C_{\text{p,comp}}$ is the input parasitic capacitance of the comparator and $C_{\text{p,rout}}$ is due to the routing metals. Usually $C_{\text{pu,top}}$ is dominated by fringing effects and can be calculated as $C_{\text{pu,top}} \approx 4 \times k_p \times \sqrt{A_{C_u}}$, where k_p represents the specific capacitance per unit length of the MIM capacitor and A_{C_u} denotes the area of the unit capacitor. Finally, by assuming a common-centroid arrangement for unitary capacitors, a lower limit for $C_{\text{p,rout}}$ can be given by:

$$C_{\text{p,rout}} \approx 2^{\frac{N}{2}} [2k_p \cdot (L_g + W_m) + k_a \cdot L_g \cdot W_m] . \tag{A.4}$$

As shown in Fig. A.2, W_m is the width of the interconnecting metal strip, L_g is the space between adjacent unit capacitors, and k_a is the specific capacitance per unit area of the MIM capacitor. These parameters are technology dependent, and their values can be obtained from the design rules of the utilized process. The value of these parameters is listed in Table A.1 for the utilized 90 nm CMOS process. Note



(a) (b)

Fig. A.2. (a) MIM capacitor structure and (b) floor plan of the unit capacitors.[18]

Table A.1. Value of the technology dependent parameters.

					Parasitic capacitance	
Parameter	k_C (fF/μm^2)	A_{C_u} (μm^2)	L_g (μm)	W_m (μm)	k_a (aF/μm^2)	k_p (aF/μm^2)
Value	2.5	7×7	2	0.5	15	45

that for the typical MIM capacitors, the value of the unit capacitor is given by $C_u = k_C \times A_{C_u}$, where k_C is the capacitor density.

B. *Effect of bottom-plate parasitic capacitances on the power consumption*

The power dissipation due to the bottom-plate parasitic capacitors has been calculated in Ref. 17 and can be written as follows:

$$P_{\text{Parasitc-bottom}} \approx \frac{f_{\text{clk}} V_{\text{ref}}^2}{N+1}(C_{b0} + C_{b1} + \cdots + C_{bN}), \tag{A.5}$$

where C_{bi} (i.e., $i = 0, \ldots, N$) is the total bottom-plate parasitic capacitance. The bottom-plate parasitic capacitance of the unit capacitor can be approximated by $C_{\text{pu,bottom}} \approx 4 \times k_p \times \sqrt{A_{C_u}} + k_a \times A_{C_u}$.[18] From the above, the estimated values of the parasitic capacitors are listed in Table A. 2.

Finally, the overall power consumption due to the parasitic capacitances of the DAC capacitor array can be approximated by:

$$\begin{aligned} P_{\text{Parasitc}} &= P_{\text{Parasitc-bottom}} + 2 \times P_{\text{Parasitc-top}} \Rightarrow \\ &\approx 2 \times \frac{f_{\text{clk}} V_{\text{ref}}^2}{N+1}\left(\frac{C_{\text{PM,total}}}{3} + C_{b0} + C_{b1} + C_{b2} + C_{b3} + C_{b4}\right). \end{aligned} \tag{A.6}$$

By applying the estimated value of each parasitic capacitance in relation (A.6), $P_{\text{Parasitic}}$ is obtained about 10 nW which is 2.5% of total ADC power consumption. Note that the power consumption due to the bottom-plate parasitic capacitors is about 9 nW. The power dissipation due to the effect of the parasitic resistors was not considered in $P_{\text{Parasitic}}$. The reason is that, due to the lower sampling rate, its effect can be reduced dramatically by using thick metal layers in layout design. Also, in estimating the power consumption due to the parasitics, only the effect of the DAC parasitic capacitances was considered. It should be noted that the proposed work

Table A.2. Estimated value of parasitic capacitors.

	Top-plate parasitic capacitors				Bottom-plate parasitic capacitors (i.e., $C_{bi} = C_{\text{p,bot}} + C_{\text{p,rout}} + C_{\text{p,switch}}$)				
Capacitor	$C_{\text{P,top}}$	$C_{\text{P,rout}}$	$C_{\text{P,comp}}$	$C_{\text{PM,total}}$	C_{b0}	C_{b1}	C_{b2}	C_{b3}	C_{b4}
Estimated value	40 fF	7.3 fF	8.7 fF	55 fF	3.93 fF	5 fF	13 fF	34.3 fF	92.4 fF

improves the performance considerably, and even with 10% increase in total power consumption, the effect of RC parasitics on the overall ADC performance is negligible.

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