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A noise-shaping SAR ADC for energy limited applications in 90 nm CMOS technology

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Abstract In this paper, an ultra-low-power successive approximation register analog-to-digital converter (ADC) for energy limited applications is presented. The ADC resolution is enhanced by using a noise-shaping technique which does not need any integrator and only uses a finite impulse response (FIR) filter. To provide a first-order noise-shaping, the quantization error is firstly extracted by using the digital-to-analog converter (DAC) dummy capacitor and it is then employed in the error feedback scheme. The proposed structure employs a low-gain and low-swing operational transconductance amplifier (OTA) to realize the FIR filter which operates only at the sampling phase. To minimize the power consumption of the ADC analog part, the OTA is powered off during the conversion phase. The proposed ADC is designed and simulated in a 90 nm CMOS technology using Spectre with a 0.5 V single power supply. The simulated ADC uses a fully-differential 8-bit charge redistribution DAC with an oversampling ratio of 8 and achieves 10.7-bit accuracy. The simulated average power consumption is 4.53 μW and the achieved maximum SNDR and SFDR are 66.1 and 73.1 dB, respectively, resulting in a figure of merit of 27.6 fJ/conversion-step.

Keywords Successive approximation register · Analog-to-digital converters · Noise-shaping · Rail-to-rail comparator

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1 Introduction

Recently, charge redistribution successive approximation register (SAR) analog-to-digital converters (ADCs) are widely used in moderate resolution and moderate speed applications such as portable instruments, battery operated devices, and biomedical signal processing systems [1–8], mainly due to their low power consumption and simple structure. Nonetheless, for effective resolutions beyond 10 bits, obtaining a very low figure of merit (FoM) is quite challenging due to the limited accuracy of the SAR ADC building blocks [2, 6–9]. In other words, since the total number of capacitors in the charge redistribution digital-to-analog converter (DAC) increases exponentially with increasing the number of bits, the accuracy of the DAC may be deteriorated due to the poor matching and parasitic effects in the physical implementation. Besides, the DAC switching power consumption is also exponentially increased. On the other hand, in higher resolutions, the value of the LSB voltage decreases compared to the input-referred noise of the comparator. So, in order to avoid the latching errors, an additional pre-amplifier is necessary to drive the comparator resulting in more power consumption.

Several solutions have been proposed to enhance the resolution of the SAR ADCs by reducing the comparator offset and improving the DAC accuracy. A time-domain comparator instead of the conventional voltage-domain comparator is used in [6, 8] where the need for the pre-amplifier is eliminated. The hybrid DAC structure is employed to improve the DAC matching [10], and hence, the ADC linearity. Using both the time-domain comparator and the hybrid DAC may be a proper candidate to increase the ADC resolution. However, in the nano-meter CMOS technologies due to the poor matching and static power consumption of the resistive ladder, used in the hybrid

DAC, the FoM of the ADC may be degraded. Digital calibration techniques are employed to alleviate the static and dynamic errors [11]. Although the calibration techniques improve the ADC linearity, they will increase the ADC power dissipation and complexity due to the calibration circuit.

Recently, the oversampling and noise-shaping characteristics of the sigma-delta modulators were employed in the SAR ADCs to achieve higher resolutions [9, 12]. In [12] by using additional capacitors, a passive method was used to extract the quantization error. In this way, the quantization error is attenuated due to the charge sharing and the modulator performance is degraded. In addition, an active adder using an operational transconductance amplifier (OTA) with several input branches is necessary resulting in a low feedback factor, and consequently, it requires a high gain-bandwidth product (GWB) OTA [9]. In [9], a cascade of FIR and infinite impulse response (IIR) filters are utilized to provide an equivalent third-order noise-shaping where two orders is resulted from the FIR filter and one order from the IIR filter which is realized by an integrator. But, in this scheme, to avoid the instability resulting from the FIR filter coefficients, a duration for the OTA gain instead of a minimum value is needed necessitating a careful circuit design. Moreover, there is some clock complexity and also passive sampling in this work resulting in more sensitivity to the circuit non-idealities.

In this paper, a fully-differential noise-shaping SAR ADC is proposed which uses the unit capacitor of the DAC array to extract the quantization error. This structure eliminates the need for additional capacitors in [12] and uses a low-gain low-swing single-stage OTA to provide a first-order noise-shaping which operates only at the sampling phase. The OTA is turned off during the conversion phase to save the power. In addition, the proposed structure has a rail-to-rail input range providing a wide dynamic range.

The paper is organized as follows. In Sect. 2, the structure of the proposed SAR ADC is presented. The circuit design considerations are described in Sect. 3. The simulations results of the proposed ADC and the comparison with several state-of-the-art SAR ADCs are provided in Sect. 4. Finally, Sect. 5 concludes the paper.

2 Proposed SAR ADC structure

The block diagram of the proposed noise-shaping SAR ADC is shown in Fig. 1. In this structure, the error feedback scheme is employed to provide a first-order noise-shaping [13] and the quantizer is realized by a SAR ADC instead of a conventional flash-based quantizer which is used in the conventional sigma-delta modulators. In the

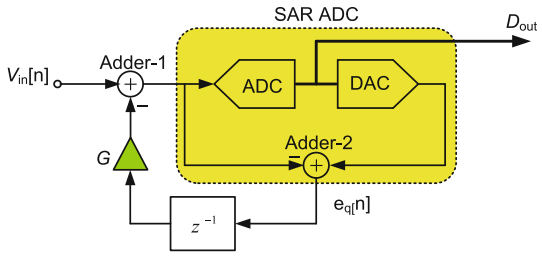

Fig. 1 Block diagram of the proposed noise-shaping SAR ADC

sampling phase, the difference between the input voltage and the quantization error of the previous sample is applied to the ADC input to achieve a first-order noise-shaping. In the following, how to extract the quantization noise in the SAR ADC is explained.

Figure 2 shows the conventional m-bit fully-differential charge redistribution SAR ADC. The main components are the capacitor array, a comparator, and a SAR logic. In this structure, the capacitor array serves as both the charge redistribution DAC and the input signal sample & hold (S/H) circuit. Since the ADC structure is fully differential, the operation of both sides is complementary. At the sampling phase, the top-plate of all capacitors is connected to the input common-mode voltage, V_{cmi}, (usually equal to 0.5 V_{DD} in most designs) and simultaneously the bottom-plate of the capacitors in the positive and negative sides are connected to $V_{\mathrm{in+}}$ and $V_{\mathrm{in-}}$, respectively. After the sampling phase, all capacitors are disconnected from the input voltage and also the input common-mode voltage. Thereafter, the conversion phase is started and the SAR changes the bottom-plate voltage of capacitors to approximate the sampled voltage. At the end of the conversion phase, the DAC voltages of positive and negative sides are, respectively, as follows:

$$V_{DAC+}[n] = -V_{in+}[n] + V_{cmi} + D_{m-1}[n]\frac{V_{\mathrm{Ref}}}{2} + \cdots + D_0[n]\frac{V_{\mathrm{Ref}}}{2^m} \quad (1)$$

$$V_{DAC-}[n] = -V_{in-}[n] + V_{cmi} + \overline{D_{m-1}}[n]\frac{V_{\mathrm{Ref}}}{2} + \cdots + \overline{D_0}[n]\frac{V_{\mathrm{Ref}}}{2^m} \quad (2)$$

As is seen from the relations (1) and (2), at the end of the conversion phase, the DAC voltages are the quantization error plus the input common-mode voltage. This residue voltage is available in the analog form. So, it can be exploited as the quantization error, $e_q[n]$, and transferred via feedback (Fig. 1). In [12], in order to store and transfer the residue voltage, a few additional capacitors (called residue capacitors) have been added in the DAC array capacitors and they are interleaved between the DAC array and the feedback path. By this way, to implement a

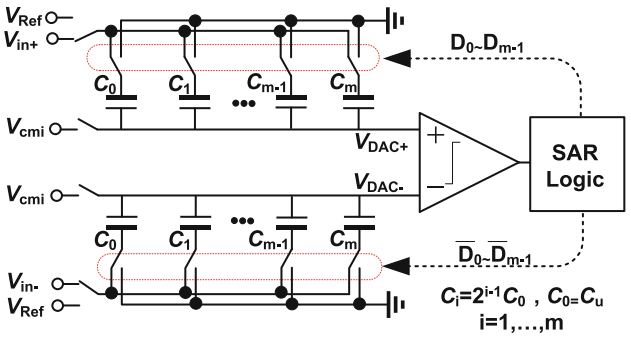

Fig. 2 Conventional *m*-bit SAR ADC

third-order sigma-delta modulator, a total of 19 residue capacitors (equivalent to 1.9 pF) were added into the DAC array. The loading effect (charge sharing) of these capacitors is not investigated in [12], and in addition, the required OTA is forced to drive a large capacitive loading resulting in more power consumption.

In the proposed structure, to avoid using the passive sampling, the unit capacitor of the charge redistribution DAC is used to transfer the quantization error. It is interleaved with another unit capacitor to provide the unit delay of the feedback path. Figure 3 shows an example of the proposed structure for a 3 bit SAR ADC. $C_{r1,2}$ are the residue capacitors and are interleaved to extract and transfer the quantization error. As shown in Fig. 3(a), during the sampling phase, the quantization error of the previous sample ($e_q[n-1] = e_{q+}[n-1] - e_{q-}[n-1]$) which is differentially stored in the C_{r2} residue capacitors, is applied to the top-plate of all capacitors through the unity-gain buffer. Simultaneously, the bottom-plate of all capacitors is connected to the input voltage. So, the stored voltage in all capacitors is the difference between the input voltage and the quantization error of the pervious sample. Then, at the conversion phase, the successive approximation procedure generates all digital codes. As shown in Fig. 3(b), at the end of the present conversion phase, the quantization error, $e_q[n]$, is stored in the C_{r1} residue capacitors (i.e. $e_{q+}[n-1]$ is stored in the positive side C_{r2} capacitor, and $e_{q-}[n-1]$ is stored in the negative side C_{r2} capacitor and consequently $e_q[n-1]$ is stored differentially on C_{r2} set). So at this time, the V_{DAC} voltage (i.e. $V_{DAC+} - V_{DAC-}$) is given by:

$$V_{DAC}[n] = e_q[n-1] - V_{in}[n] + \sum_{i=0}^{m-1} D_i[n] \frac{V_{Ref}}{2^{m-i}} \tag{3}$$

where $V_{in} = V_{in+} - V_{in-}$, and the summation expresses output bits of the SAR logic in the analog form.

On the other hand, the value of the quantization error is obtained from the relations (1) and (2) as:

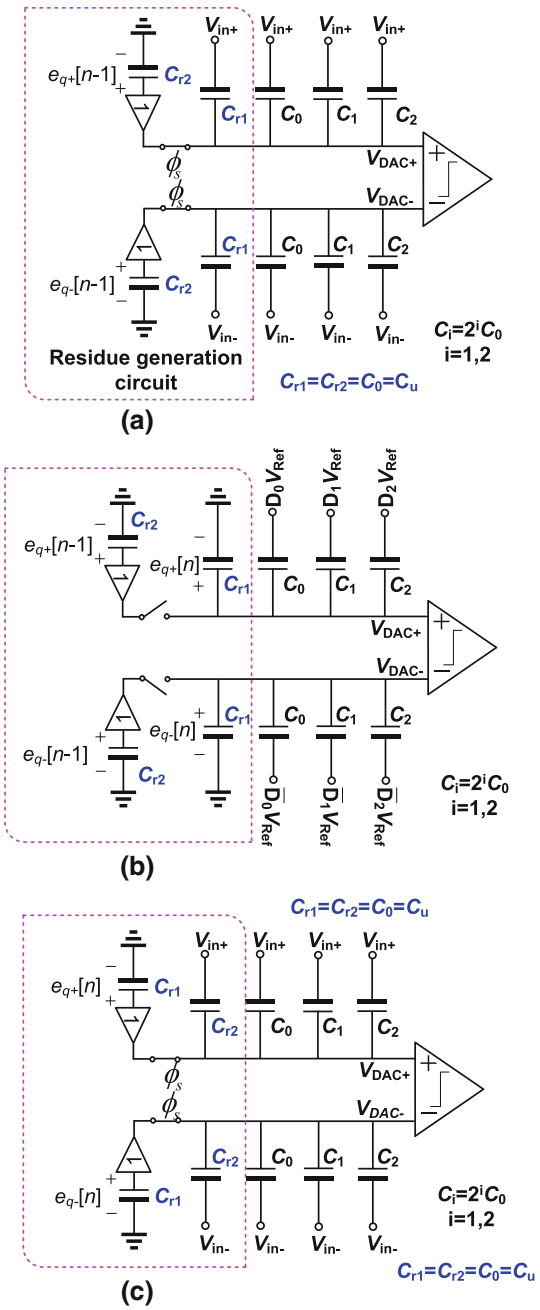

Fig. 3 Operation of the proposed ADC with 3-bit SAR quantizer at: **a** sampling phase, **b** conversion phase, and **c** the next sampling phase

$$V_{DAC}[n] = e_q[n] \tag{4}$$

By applying the relation (4) into (3), the following relation is obtained:

$$e_q[n] - e_q[n-1] = -V_{in}[n] + \sum_{i=0}^{m-1} D_i[n] \frac{V_{Ref}}{2^{m-i}} \tag{5}$$

where the term $e_q[n] - e_q[n-1]$ represents a first-order noise-shaping. In other words, the equivalent analog output

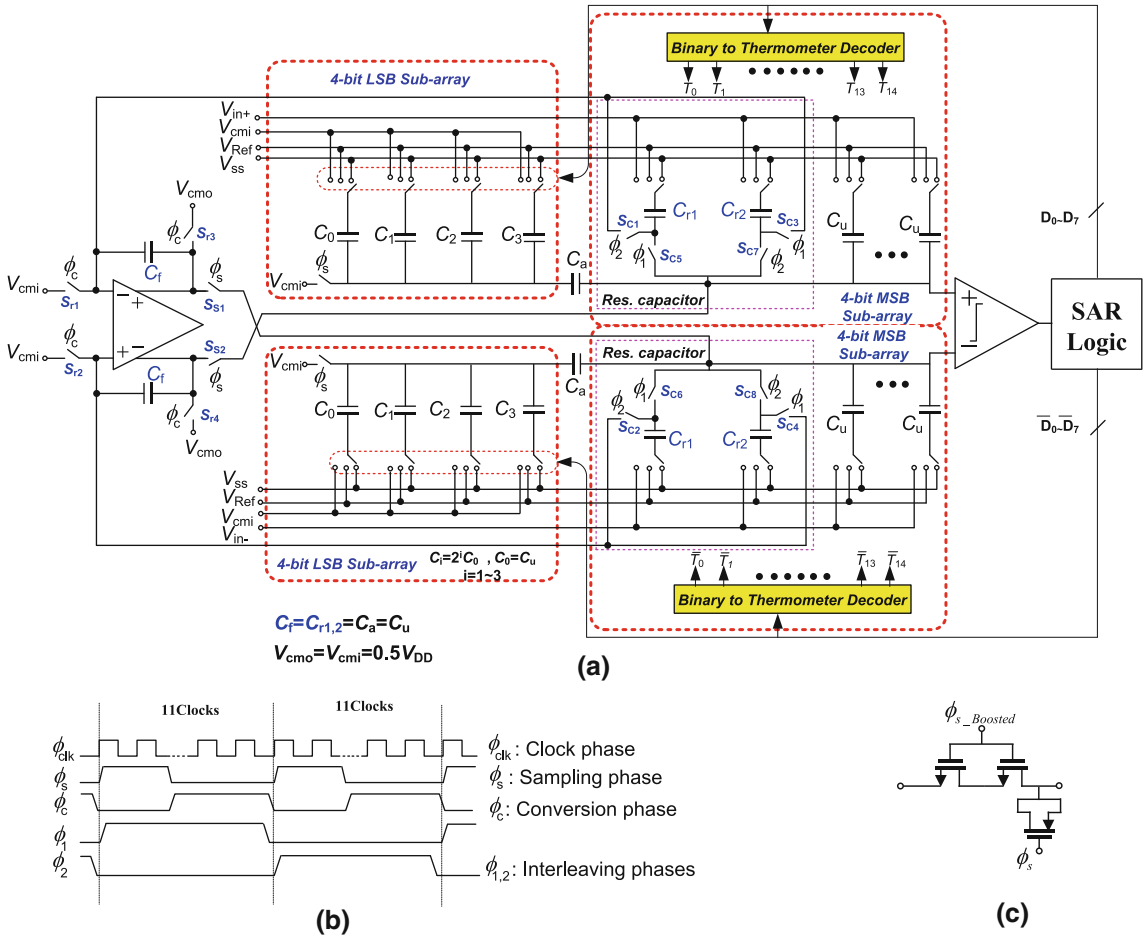

Fig. 4 **a** Proposed noise-shaping ADC with 8-bit SAR quantizer, **b** timing diagram, and **c** the realization of $S_{S1,2}$, S_{C1-8} and S_{r1-4} switches

of the ADC, V_{out}, at the end of the conversion phase is given by:

$$V_{out}[n] = V_{in}[n] + e_q[n] - e_q[n-1] \tag{6}$$

As is seen, the input signal directly appears at the output while the quantization error is first-order shaped. Therefore, according to Fig. 3, the quantization error is extracted by using $C_{r1,2}$ residue capacitors and then it is applied to the quantizer's input by its injection into the charge redistribution DAC array. This circuit implementation is in the fully compliance with the system realization of a first-order error feedback sigma-delta modulator shown in Fig. 1.

At the next sampling phase, as shown in Fig. 3(c), the role of C_{r1} and C_{r2} residue capacitors is interchanged and C_{r1} is connected to the unity-gain buffer whereas C_{r2} acts as the DAC dummy capacitor. Since the residue capacitors are reset by the input voltage, there is no memory effect. This procedure is repeated for each sample of the input signal.

3 Circuit level design considerations of proposed SAR ADC

This section describes the circuit level implementation details and considerations of the proposed SAR ADC. A design example of the proposed SAR ADC with 11-bit resolution and 100 kS/s Nyquist rate has been implemented in the circuit level to verify its usefulness. This design has been performed in a 90 nm CMOS technology with 0.5 V power supply to save the power consumption. In the following, the circuit details are explained.

The proposed ADC can provide the maximum signal-to-quantization noise ratio (SQNR) of 72.9 dB by using an oversampling ratio (OSR) of 8 and an 8-bit SAR quantizer. Figure 4 shows the complete schematic of the proposed noise-shaping SAR ADC. To reduce the number of DAC capacitors, the split architecture with an attenuation capacitor is used as the charge redistribution DAC array [14]. To realize the 8-bit DAC array, in this design, a 4-bit

thermometer coded DAC in the MSB sub-array and a 4-bit binary weighted DAC in the LSB sub-array are utilized (more explained later). Φ_1 and Φ_2 are two non-overlapping clock phases and used to provide the unit delay by interleaving C_{r1} and C_{r2} capacitors. The operation of the ADC is as follows.

At the sampling phase and when Φ_1 is high, the bottom-plate of MSB sub-array capacitors except the C_{r2} residue capacitors is connected to the input voltage whereas their top-plate is connected to the buffer output. At the same time, the both-plate of LSB sub-array capacitors is connected to the common-mode voltage. During phase Φ_1, the C_{r1} residue capacitors are connected to the DAC and act as the unit capacitors in the MSB sub-array ($C_{r1,2} = C_u$) whereas the C_{r2} residue capacitors are connected to the buffer inputs and transfer the previously sampled quantization error. Their role is changed during Φ_2 phase. In this design, the 5th bit capacitors of the MSB sub-array are also employed as the residue capacitors. Note that these capacitors contain the quantization error as long as their bottom-plate voltage remains unchanged. Therefore, an additional D-latch is used to maintain this bottom-plate voltage during next interleaving phase (i.e. during Φ_1 for C_{r2} and during Φ_2 for C_{r1}). With beginning the conversion phase (Φ_c), the OTA is disconnected from the DAC capacitors and the stored charge in the feedback capacitor, ($C_f = C_u$) is discharged to prevent the charge accumulation. The SAR changes the bottom-plate voltage of capacitors to approximate the sampled voltage. After generating the output bits, the quantization error of the present sample is stored in C_{r1}. So, by beginning the next sampling phase, the role of residue capacitors is interchanged. When Φ_2 goes high, the C_{r2} residue capacitors are connected to the DAC capacitors while the C_{r1} capacitors transfer the previous quantization error. The bottom-plate of the MSB sub-array capacitors excluding C_{r1} is connected to the input voltage while their top-plate is connected to the previous quantization error through the unity-gain buffer. Therefore, the difference between the input voltage and the pervious quantization error is stored in the DAC capacitors, and hence, according to the relation (6), this provides a first-order noise-shaping. Similar to the previous sample, the SAR control logic generates the output codes at the conversion phase. This procedure is repeated for each sample of the input signal.

Due to the noise-shaping property, the offset voltage of the comparator is shaped [9, 13]. But, the matching requirement of the DAC capacitor array, the linearity of the switches and also the OTA performance, are the main factors which may affect the ADC performance. These issues are explained in the following.

3.1 DAC capacitor array

As mentioned before, in the proposed noise-shaping SAR ADC shown in Fig. 4, the DAC capacitor array is implemented by the split capacitive array (SCA) with an attenuator capacitor [14]. The SCA structure reduces the total DAC capacitance and switching power. Nonetheless, it is sensitive to the parasitic capacitances on both sides of the attenuator capacitor, C_a. Besides, it is necessary to provide sufficient matching in the DAC capacitors to meet the desired ADC accuracy. The effect of capacitance mismatch upon the ADC accuracy for SCA structure has been investigated in [15, 16]. Due to the attenuator capacitor, the capacitance mismatch effect of the LSB sub-array is reduced by 1/16 in this design. Thus, the matching of the MSB sub-array will be important. Here, to relax the matching requirement of the MSB sub-array, it is implemented by using the unary weighted array whereas the LSB sub-array is implemented by the conventional binary weighted array. Also, to provide good matching between the MSB and the LSB sub-arrays, the attenuator capacitor was chosen equal to C_u and the dummy capacitor of the LSB sub-array is eliminated [6, 16]. Note, that by using the unary weighted structure in the MSB sub-array, the switching power of the capacitor array is also reduced, because regardless of the conventional binary weighted array, the number of capacitors which is needed to be charged in each conversion phase is different and it depends on the value of the input sample. Briefly, the unit capacitor value is determined by considering the required capacitor matching, thermal noise, and technology design rules.

The minimum value of the unit capacitor to meet the matching requirement is determined by the maximum standard deviation of ADC differential nonlinearity (DNL) error. By employing unary weighted array in the MSB sub-array, the following relation must be satisfied for a single-ended SCA structure [15]:

$$\frac{\sigma_u}{C_u} < \frac{1}{3 \times 2^{N-M+1}} \tag{7}$$

where N is the targeted ADC resolution, M is the number of MSB bits and σ_u is the unit capacitor standard deviation. For $N = 11$ and $M = 4$, the maximum value of σ_u/C_u of 0.13 % is achieved. The standard deviation of the capacitor mismatch, $\sigma(\Delta C/C)$, is $\sqrt{2}$ times of σ_u/C_u [3]. Consequently, the value of $\sigma(\Delta C/C)$ is obtained as 0.18 % corresponding to a 90 fF capacitance in the utilized 90 nm CMOS process.

On the other hand, by considering the thermal noise, another minimum value for the DAC unit capacitor is determined. To do so, the overall kT/C noise at the ADC

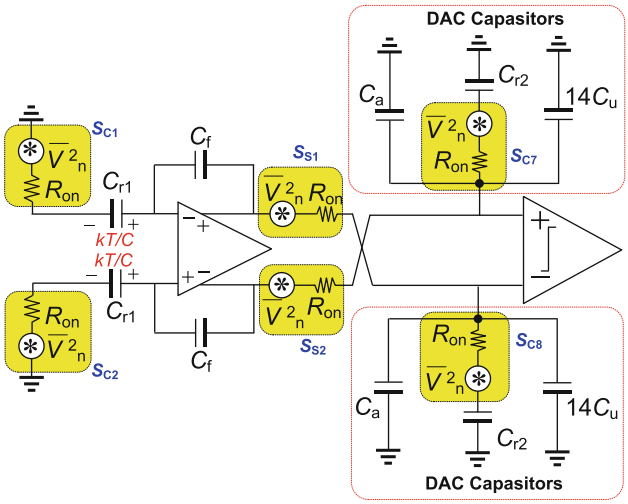

Fig. 5 Equivalent circuit for FIR filter noise analysis when $\Phi_2 = \Phi_s = 1$

input must be calculated. This noise includes the kT/C noise of the capacitor array and the thermal noise of the FIR filter (S_{C1-8} and $S_{S1,2}$ switches in Fig. 4). Similar to [17], the kT/C noise of the SCA capacitive array in the fully differential mode can be approximated as:

$$\overline{V}^2_{n,DAC} = 2 \times \frac{kT}{C_u}\left(2^{(1-\frac{N}{2})} - 2^{(-\frac{3N}{2})}\right) \approx \frac{1}{2^{\frac{N}{2}-1}}\frac{kT}{C_u} \tag{8}$$

where C_u is the DAC unit capacitor, k is the Boltzmann constant, T is the absolute temperature, and N denotes the ADC resolution with $N \geq 2$. The thermal noise of S_{C1-8} and $S_{S1,2}$ switches is calculated based on the equivalent circuit shown in Fig. 5. This circuit is drawn in the sampling phase and when Φ_2 is high. Hence, by using the superposition theorem and assuming no correlation between the noise sources, the following relation is obtained:

$$\begin{aligned}\overline{V}^2_{n,FIR} &= 2 \times \left\{\frac{kT}{C_u} + \frac{kT}{16 \times 33C_u} + \frac{kT}{16.5 \times 15.5C_u} + \frac{kT}{C_u}\right\} \\ &\approx 4\frac{kT}{C_u}\end{aligned} \tag{9}$$

The coefficient 2 in relation (9) accounts for the noise of the fully differential mode. The first term in this relation is the thermal noise of S_{C3} (S_{C4}) switches which is stored in C_{r1} during Φ_1 phase and transferred similar to the quantization error in the Φ_2 phase. Also, the second and third terms indicate the thermal noise contribution of S_{s1} (S_{s2}) and S_{C7} (S_{C8}) switches in the FIR filter, respectively. Finally, the last term in this relation is the thermal noise of S_{C1} (S_{C2}) switches which has the considerable effect in the overall kT/C noise. As is seen from the relations (8) and (9), it is clear that the effect of FIR filter thermal noise is dominant. So, the overall kT/C noise of the ADC is approximated by relation (9). Due to the oversampling, only a fraction of this noise falls into the band of interest. As a result, the minimum value of C_u is obtained about 105 fF by thermal noise consideration.

Finally, the minimum value of the metal–insulator–metal (MIM) capacitance in the used process is about 49 fF. Consequently, in this design, the unit capacitance is not limited by the technology design rules. Therefore, the DAC unit capacitance is selected 105 fF to meet the thermal noise requirement.

As shown in Fig. 4, at the sampling phase, the quantization error is only applied to the top-plate of the MSB sub-array capacitors and the top-plate of LSB sub-array capacitors is connected to the common-mode voltage. Therefore, the quantization error is not stored at the bottom-plate parasitic capacitance of LSB sub-array and also the settling of the OTA is relaxed due to the load capacitor reduction. On the other hand, during the MSB bits generation, the bottom-plate of LSB sub-array capacitors is connected to the common-mode voltage. Since they are switched from V_{cmi} to V_{Ref} and/or to ground during the LSB bits generation, the switching power of the LSB sub-array is also reduced. In addition, the voltage level of $V_{Ref}/2$ (V_{cmi}) is generated without any capacitor switching in the LSB sub-array. So, the resolution of LSB sub-array can be reduced from 4-bit to 3-bit. However, the 4-bit resolution is allocated to the LSB sub-array where the extra 1-bit acts as the redundancy and can compensate the incorrect DAC settling errors happening due to the bottom-plate parasitic capacitance of the attenuator capacitor.

3.2 OTA structure

Since the unity-gain buffer is used to transfer the quantization error through the feedback path, it is necessary that its closed-loop dc gain (G) to be near 1 to achieve good accuracy. However, the OTA finite open-loop dc gain (A_{dc}) decreases the closed-loop gain as $G = 1 - 1/A_{dc}$. This causes the ADC noise transfer function (NTF) zero to move from z = 1 to inside of the unit circle in the z-plane

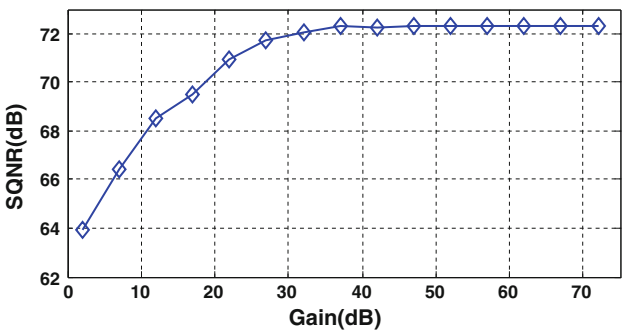

Fig. 6 Simulated ADC SQNR versus the OTA open-loop dc gain

whereas the location of the ADC NTF pole is not changed. As a result, for low values of A_{dc}, the inband quantization noise is increased. According to the behavioral simulation results shown in Fig. 6, an SQNR more than 69 dB is achieved when the OTA dc gain is as low as 17 dB.

Since the unity-gain buffer processes only the quantization noise and it is a few mV when the ADC resolution is high enough (2 mV in this design example), so a low-swing OTA is needed to realize the buffer. From the theoretical calculations, the minimum transconductance value of input transistors to meet the required gain bandwidth product (GBW) is obtained about 20 μA/V. In this calculation, the load capacitance, C_{load}, is the summation of the MSB sub-array capacitors in the DAC capacitor array plus the parasitic capacitances which is altogether about 1.68 pF. As shown in Fig. 4, two clock cycles of the SAR operation were allocated to the sampling phase which provides approximately 230 ns settling time for OTA.

In order to achieve the desired dc gain, the single-stage folded-cascade OTA shown in Fig. 7(a) is used as the unity-gain buffer. The transistors $M_{2,3}$ and $M_{6,7}$ act as the up-level shifters to enhance the OTA input common-mode voltage from 0.25 to about 0.35 V. This is needed to guarantee that the tail transistor, M_1, to be biased in the saturation region in all process corner cases at this low supply voltage which is 0.5 V, although they reduce the gain and unity-gain bandwidth of the OTA slightly. The OTA bias and common-mode feedback (CMFB) circuits are shown in Fig. 7(b, c), respectively. Since the OTA operates only at the sampling phase, it is powered off at the conversion phase by bias switching technique to save the power consumption. This makes the average power consumption of the simulated OTA to be decreased from 11.7 to 3.1 μW. AC simulation results shown in Fig. 8 indicate that the simulated OTA achieves 21.7 dB dc gain and 7.23 MHz unity-gain bandwidth with 66° phase margin. Table 1 summarizes the detailed simulation results of the OTA. Note that in proposed ADC structure, the residue capacitors $C_{r1,2}$ and the feedback capacitor C_f have the same value. So, the feedback factor of the OTA in the closed-loop configuration is 0.5.

3.3 Implementation of the switches

As shown in Fig. 4, the top-plate of the LSB sub-array and MSB sub-array capacitors is only connected to the common-mode voltage and to the OTA output, respectively, whereas their bottom-plate is connected to the input voltage and/or to the power rails (V_{Ref} and ground) and common-mode voltage by three type switches. In order to accommodate full swing input, all bottom-plate sampling switches are implemented using CMOS transmission gates. Since the supply voltage of this design is 0.5 V, it may degrade the capacitor array settling and linearity performance due to poor and signal dependent on-resistance of the switches. Therefore, the gate of nMOS transistors is driven by a booster circuit [18]. Also, the bottom-plate of the LSB sub-array capacitors is connected to the

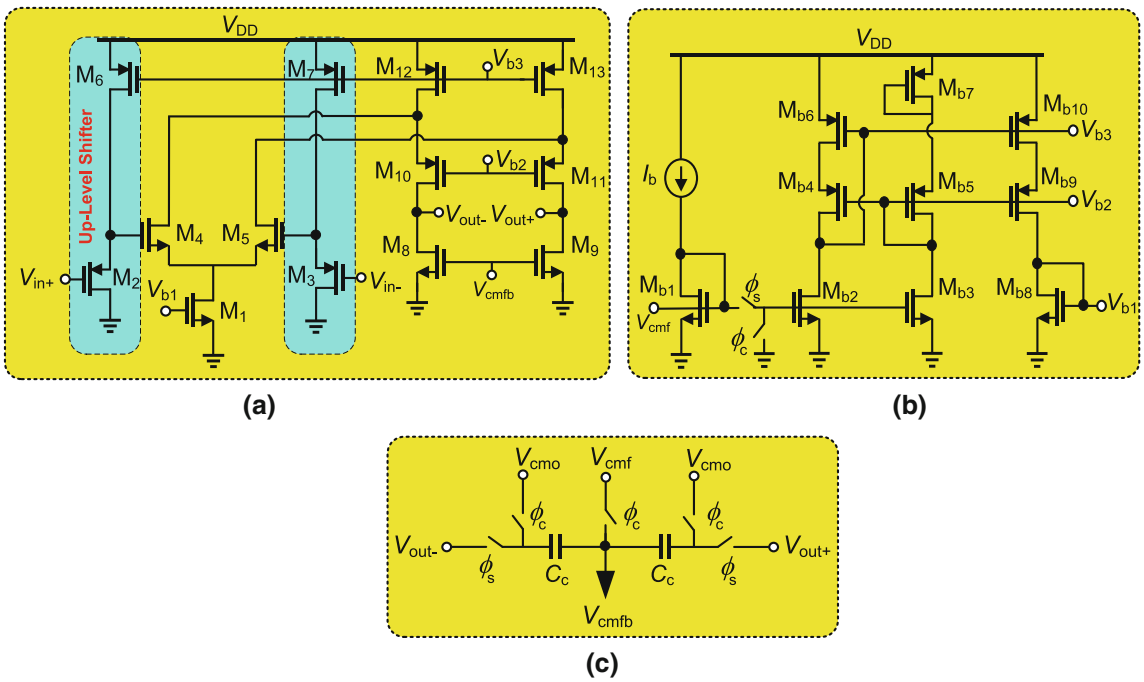

Fig. 7 **a** OTA, **b** bias, and **c** common-mode feedback circuits

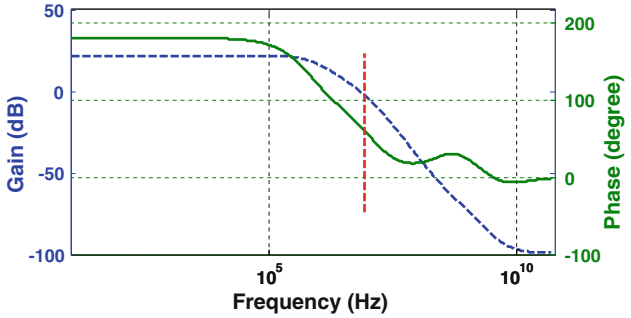

Fig. 8 Simulated frequency response of the OTA

Table 1 Performance summary of the simulated OTA

Parameter	TT @ 27 °C	FF @ −40 °C	SS @ 85 °C
DC gain	21.76 dB	22.23 dB	21.9 dB
GBW	7.23 MHz	8.95 MHz	5.88 MHz
Phase margin	66°	60°	69°
0.5 LSB settling time	191 ns	183 ns	197 ns
Avg. power consumption (without switching)	11.7 μW	11.85 μW	12 μW
Avg. power consumption (with switching)	3.1 μW	3.1 μW	3.3 μW
Load capacitance	1.68 pF		
Feedback factor	0.5		
Supply voltage	0.5 V		
Technology	90 nm CMOS		

common-mode voltage by similar switches. The boosted clock will be about 1 V at most. Hence, there is no gate oxide breakdown concern here. To connect the bottom-plate of these capacitors to power rails during the successive approximation procedure, minimum size nMOS and pMOS transistors were used due to the low frequency operation of the simulated ADC. In addition to the capacitor array switches, other switches are added to the structure which provide feedback loop to exploit and transfer the quantization error. These switches are marked by S_{r1-4}, S_{C1-8} and S_{S1-2} in Fig. 4(a). The switches S_{r1-4} and S_{C1-4} are not critical since one side of them is connected to the common-mode voltage and the virtual ground, respectively. By contrast, the switches S_{S1-2} and S_{C5-8} may be critical since they have a floating behavior and their charge injection may introduce some harmonic distortion and affect the ADC accuracy. Fortunately, the introduced distortion is dependent on the quantization error instead of input signal. Therefore, the distortions amplitude will be small compared to the input signal.

To investigate the introduced error due to the charge injection of S_{C5-8} switches, consider the case where the switches $S_{C5,6}$ or the switches $S_{C7,8}$ are going to be turned off. Due to the non-overlapping phase, the $S_{C5,6}$ ($S_{C7,8}$) switches will turn off before activating the $S_{C1,2}$ ($S_{C3,4}$) switches. Since the C_{r1} (C_{r2}) capacitor has high impedance in comparison to the $15C_u$ capacitor, the contribution of the injected charge in the stored quantization error on C_{r1} (C_{r2}) will be small (about 1/16). The charge injected into the charge redistribution capacitors is not important because they are reset during the next sampling phase.

Note that the switches $S_{S1,2}$, S_{C1-8} and S_{r1-4} are used to switch the voltage around the common-mode voltage. As shown in Fig. 4(c), a two-transistor stack is used instead of single nMOS transistor, to reduce the leakage current [19]. Also, to mitigate the poor on-resistance, the gates of both transistors are driven by the boosted voltage. Finally, an additional pMOS transistor is used as a dummy for $S_{S1,2}$ and S_{C1-8} switches to reduce the charge injection and clock feed-through effects.

3.4 Comparator

A rail-to-rail comparator is employed in this design to achieve the maximum dynamic range in 0.5 V power supply. Figure 9 shows the structure of this comparator. The basic structure of the comparator originates from the comparators introduced in [20, 21]. In order to extend the common-mode input range to the rail-to-rail, a few modifications have been applied here. The comparator comprises of two up and down preamplifiers and the latch stage. In fact, the p- and n- type differential pairs ($M_{p1,2}$, $M_{n1,2}$) are connected in parallel with each other to act as the rail-to-rail pre-amplifiers. Also, the transistors located on both sides of the latch stage act as NAND logics and combine the output voltage of the inverters.

The operation of this comparator is similar to [21]. At the reset phase when Clk is low, the parasitic capacitances of nodes d_{n1} and d_{n2} are charged to V_{DD} whereas the parasitic capacitances of nodes d_{p1} and d_{p2} are discharged to the ground. Moreover, the voltage at nodes $g_{n1,2}$ and $g_{p1,2}$ is charged to V_{DD} due to the inverters. This leads the voltage of the g_{n3} and g_{n4} nodes to discharge to the ground. Thereafter, the resetting transistors, $M_{lp7,8}$, are turned on and causes the V_{out+} and V_{out-} nodes to be charged to V_{DD}. During the evaluation phase when the Clk is high, the stored voltage on the parasitic capacitances of the d_{n1} and d_{n2} nodes are discharged from V_{DD} to the ground whereas the parasitic capacitances at nodes d_{p1} and d_{p2} are charged to V_{DD} at different time rates which depends on the magnitude of each input voltage. Therefore, the inverters of each pre-amplifier are turned on at different times making the input voltage difference converted to the time and or phase differences. This voltage amplified by the inverters

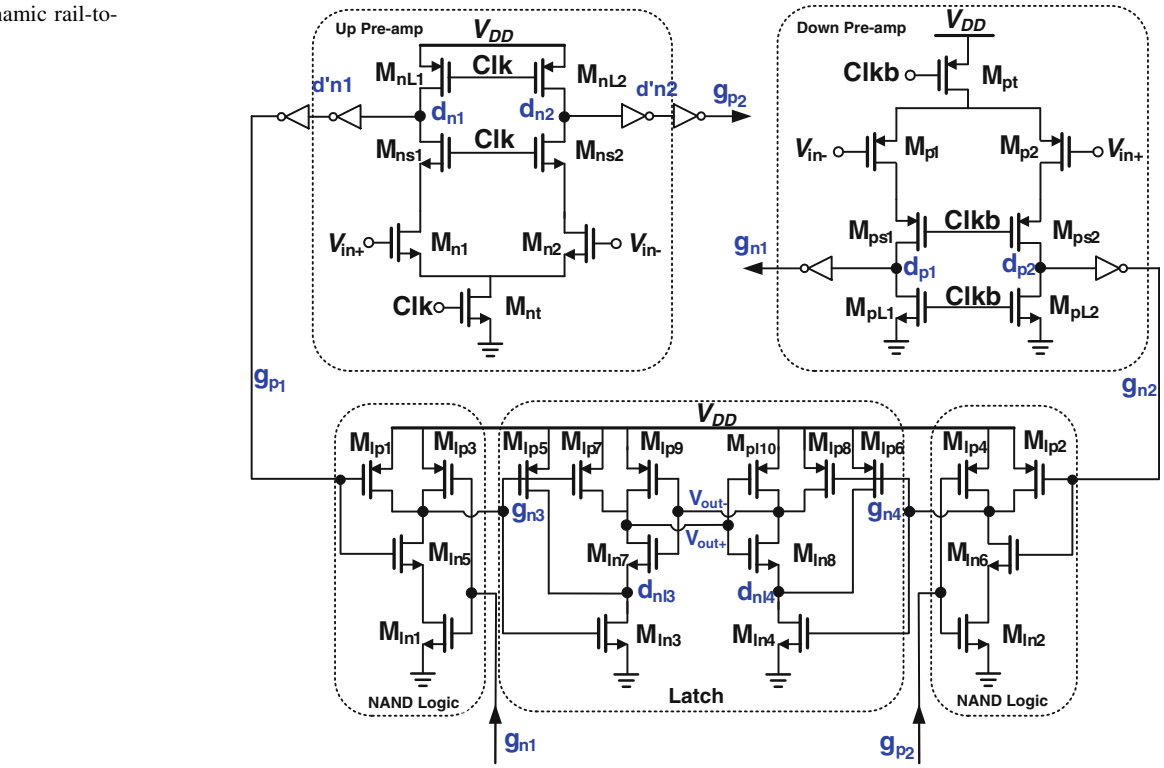

Fig. 9 Fully dynamic rail-to-rail comprator

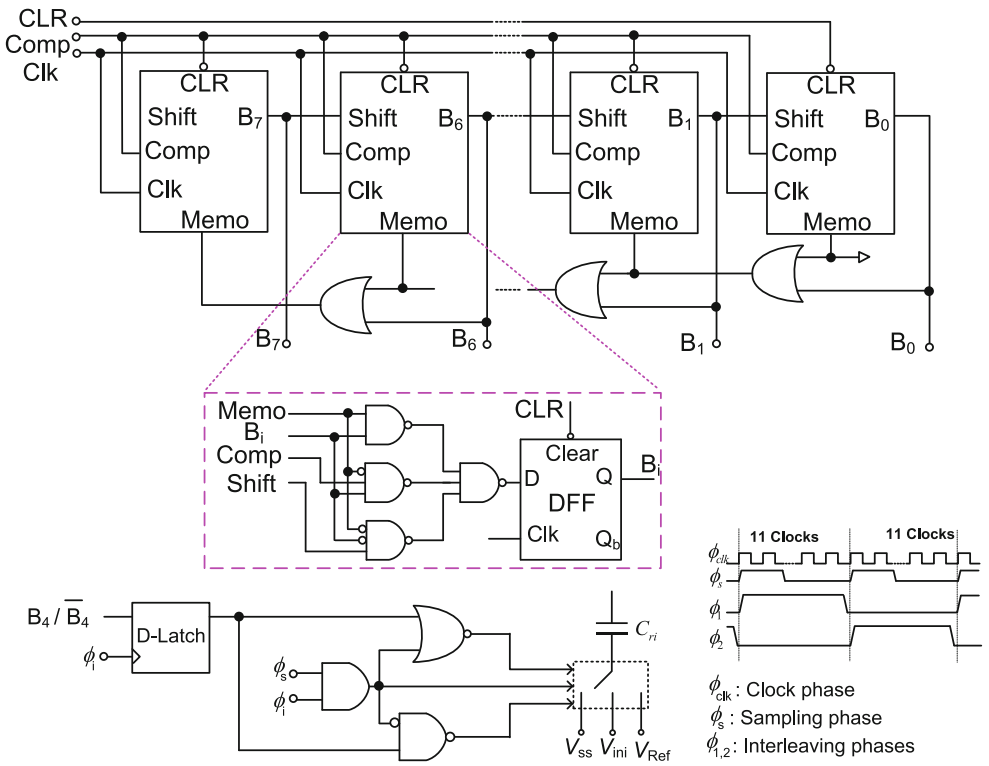

Fig. 10 SAR control logic

and then applied to the latch. Due to the positive feedback in the back-to-back inverter, one of the output nodes is forced to the ground and the other to V_{DD}.

Although the noise-shaping property relaxes the comparator requirement, to estimate the equivalent input-referred offset voltage, a Monte-Carlo simulation is

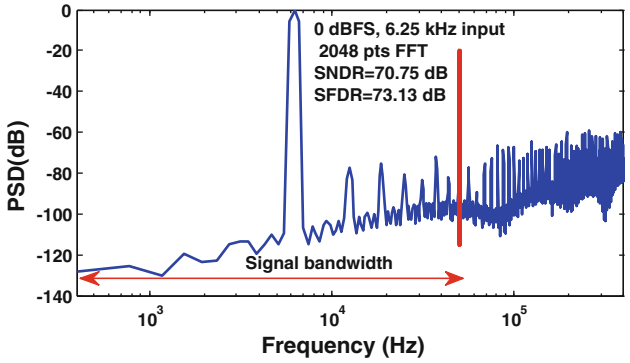

Fig. 11 Simulated ADC output spectrum excluding the circuit noise (TT @ 27 °C)

performed. The offset voltage standard deviation (σ_{Voff}) and the mean offset of the simulated comparator are about 7.1 mV and 851 μV, respectively. Therefore, the total offset voltage is about 22 mV. Regardless the noise-shaping property, the SNR degradation is 0.39 dB corresponding to the 0.065-LSB loss in ADC accuracy.

3.5 SAR control logic

The non-redundant structure introduced in [22] is used to generate the necessary controlling signals of the comparator and DAC switches. In order to control the DAC residue capacitors, a few modifications have been performed in the main structure. The schematic diagram of the 8-bit SAR control logic is illustrated in Fig. 10 which is comprised of 8 multiple input shift registers and an additional logic gate with D-type latch to maintain the bottom-plate voltage of the residue capacitors during the interleaving operation at the conversion phase. As mentioned before, each residue capacitor acts as the DAC unit capacitor only in one interleaving phase (Φ_1 or Φ_2) and in other phase it transfers the quantization error of the previous sample. Therefore, the bottom-plate voltage of the residue capacitor, C_{ri}, will be changed if only the voltage of Φ_i is high. Each shift register comprises of the decoder-multiplexer and the D flip-flop where all were implemented by NAND gates.

4 Simulation results

To verify the usefulness of the proposed noise-shaping SAR ADC, a 0.5-V 100 kS/s Nyquist-rate ADC with OSR = 8 and 8-bit charge redistribution capacitor DAC is designed and simulated in a 90 nm CMOS process. The simulated ADC output spectrum is shown in Fig. 11 where a 6.25 kHz, 0-dBFS sinusoidal input is applied to the ADC and 2048 points FFT with a Hann window is utilized for spectral estimation. In this simulation, the circuit noise was not considered but the overall kT/C noise of the ADC was calculated according to the relations (8) and (9) yielding the in-band fully differential noise with a mean-square value of about 21×10^{-9} V^2, whereas the signal power is 125×10^{-3} V^2 and the quantization noise power is 10.5×10^{-9} V^2. Therefore, by considering the circuit noise, the SNDR of the simulated ADC is obtained about 66.1 dB. According to Fig. 11, the simulated SFDR is about 73.1 dB indicating the high linearity performance of the proposed ADC. The average power consumption of the simulated ADC is about 4.53 μW.

The simulated ADC performance in different process corner cases and temperature variations is summarized in Table 2 where the power consumption of the ADC building blocks are separately reported. As is seen, the ADC analog section consumes more power than the digital section such that the FIR filter has the highest contribution in the overall power dissipation. The following figure-of-merit (FoM) is

Table 2 Performance summary of the simulated noise-shaping SAR ADC

Parameter	TT @ 27 °C	FF @ −40 °C	SS @ 85 °C
SNDR	66.08 dB	67.8 dB	64.4 dB
SFDR	73.13 dB	74 dB	71.43 dB
ENOB	10.68 bit	10.98 bit	10.42 bit
ADC power dissipation			
Comparator	320 nW	345 nW	295 nW
DAC + decoder	920 nW	935 nW	845 nW
FIR filter	3.1 μW	3.1 μW	3.3 μW
SAR logic	190 nW	225 nW	165 nW
Total power consumption	4.53 μW	4.61 μW	4.6 μW
Nyquist rate	100 kHz		
Oversampling ratio	8		
Signal bandwidth	50 kHz		
Supply voltage	0.5 V		
Technology	90 nm CMOS		

Table 3 Performance comparison of the simulated ADC with several recently reported low-power SAR ADCs

Reference	Process	Resolution of DAC (bit)	Sampling rate	Supply (V)	Input range	Power consumption	SNDR (dB)	ENOB (bit)	FoM (fJ/c-s)
JSSC'07 [2]	0.18 μm	12	100 kS/s	1	1 V p–p	25 μW	65.3	10.55	165
JSSC'12 [3]	0.13 μm	10	1 kS/s	0.4,1	1 V p–p	53 nW	57	9.1	94.5
JSSC'07 [4]	0.18 μm	8	200 kS/s	0.9	Rail-to-rail	2.47 μW	47.4	7.58	65
JSSC'12 [5]	0.18 μm	10	200 kS/s	0.6	1.13 V p–p	1.041 μW	57.64	9.34	8.03
AICSP'10 [6]	0.18 μm	12	100 kS/s	1	–	3.8 μW	58	9.4	56
AICSP'11 [7]	0.5 μm	10	100 kS/s	1.2	0.7 V	12 μW	58.9	9.49	166.3
JSSC'11 [8]	0.18 μm	10	100 kS/s	0.6	Rail-to-rail	1.3 μW	57.7	9.3	21
JSSC'12 [9]	65 nm	8	90 MS/s	1	1 V p–p	806 μW	62	10	35.7
CTA'12 [16]	0.35 μm	10	2 kS/s	1	Rail-to-rail	130 nW	58.40	9.4	96
ISSCC'11 [23]	65 nm	10	20 kS/s	0.55	–	206 nW	55	8.85	22.4
ISCAS'09 [24][a]	0.13 μm	10	100 kS/s	1	1 V p–p	1 μW	57	9.17	17
ISCAS'11 [25][a]	90 nm	10	1 MS/s	1	1 V p–p	7 μW	57.14	9.2	11.9
ISCAS'12 [26][a,b]	0.18 μm	8	16 kS/s	1.2	–	450 nW	49.9	8	132
JCSC'11 [27][a,b]	0.18 μm	8	1.23 MS/s	1.2	25.6 μA	73.19 μW	46.23	7.38	357
NEWCAS'12 [28][a]	0.18 μm	9	25 kS/s	1	–	160 nW	53	8.57	17
MWSCAS'12 [29][a]	0.18 μm	11	200 kS/s	1.2	–	6.7 μW	67.6	10.93	18.8
MWSCAS'12 [30]	0.13 μm	11	32 kS/s	1.02	–	857 nW	59	9.51	36.8
ESSCIRC'11 [31]	0.25 μm	8	31.25 kS/s	0.5	Rail-to-rail	87.41 nW	45.14	7.2	20
AICSP'13 [32]	0.18 μm	12	100 kS/s	1.8	2.4 V p–p	579.6 μW	68.74	11.13	2590
AICSP'13 [33][a]	0.18 μm	10	100 kS/s	0.9	Rail-to-rail	6.21 μW	58.9	9.55	82.8
This work[a]	90 nm	8	800 kS/s	0.5	Rail-to-rail	4.53 μW	66.08	10.68	27.6

[a] Simulation results

[b] Current mode

used to compare the simulated ADC performance with several recently reported low-power SAR ADCs and the results are shown in Table 3.

$$FoM = \frac{Power}{2 \times BW \times 2^{ENOB}} \quad (10)$$

This FoM is calculated excluding the power consumption of the decimation filter similar to [9]. As is seen, the simulated ADC achieves a good FoM among the published ones verifying the usefulness of the proposed noise-shaping SAR ADC, and hence, it can be a good candidate for low power and high resolution SAR ADCs. Moreover, due to the reduced DAC capacitance, the proposed structure has a relaxed anti-aliasing filter in comparison to the other high resolution SAR ADCs.

5 Conclusions

In this paper, a new noise-shaping SAR ADC was presented. The proposed ADC uses a simple technique to extract the quantization error by using the DAC dummy capacitor. It is then employed in an error feedback structure to provide a first-order noise-shaping. A low-gain and low-swing OTA was used to realize the buffer in order to extract the quantization noise and also to implement the unit delay in the sigma-delta modulator's feedback loop. A design example with 11-bit resolution and 100 kHz Nyquist rate was implemented in a 90 nm CMOS technology and simulated with Spectre to verity the usefulness of the proposed ADC scheme. The simulation results achieve 66.1 dB maximum SNDR and 73.1 dB SFDR while consuming 4.53 μW average power from a single 0.5 V supply resulting in a FoM of 27.6 fJ/conversion-step.

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